盛微先進科技
SAVITECH.COM

BRAVO-DSD
SA9302L

Stereo In/Out
DSD64/DSD128/DSD256
PCM 32Bit/384KHz
USB Audio Streaming Controller
WLCSP-49 Package

Datasheet v1.0

SAVITECH Corporation

BRAVO-DSD/PCM
SA9302L
USB Audio Streaming Controller

Overview

The SA9302L is a high performance up to 32bit, 384KHz PCM and DSD64/128/256 streaming USB High-Speed compliant audio steaming controller. It features one IEC60958 S/PDIF transmit streaming output. The SA9302L is ideal for both one stereo-in and one stereo-out professional digital audio interface applications. Its PCM resolution and sampling rate can be configurable with 16/24/32 bit and 32/ 44.1/ 48/ 88.2/ 96/ 176.4/ 192/ 352.8/ 384KHz respectively.

Features

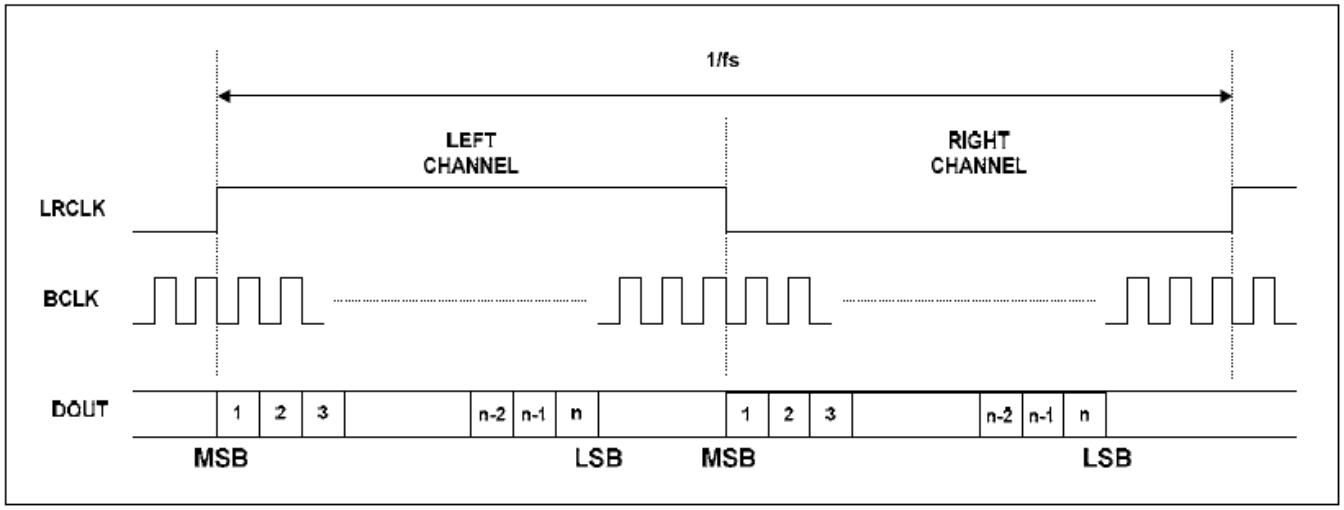
- Support iAP2
- USB 2.0 High-Speed Compliant
- USB Audio Class v1.0 and v2.0 supported
- Incredible Bravo sound quality supported by Savitech innovative Bravo Tech*1
  - Bravo Tech*1 supporting Jitter-less outputs using local clock in Async-mode
- Isochronous input and output endpoints for recording and playback
- Support Dynamic Consumption Adjustment
- One interrupt endpoint for HID
- One DSD interface for connect with external DSD DAC
- Support DSD64 / DSD128 / DSD256 both of native and DoP in Async mode
- Support DSD L/R data line swap feature
- Support resolutions up to 32-bit and sampling rates up to 384KHz
- One I2S input and one I2S output pairs for PCM
  - Independent sample rates for each pairs
  - 32/ 44.1/ 48/ 88.2/ 96/ 176.4/ 192/ 352.8/ 384 KHz sampling rates
  - 16/24/32 bit resolution
- Built in IEC60958 professional S/PDIF TX
  - AES/EBU supported
  - SCMS for copyright supported
  - Stereo S/PDIF Output
  - 32/ 44.1/ 48/ 88.2/ 96/ 176.4/ 192/ 352.8/ 384 KHz sampling rates
  - 16/24 bit resolution
  - DSD with S/PDIF TX
- Control and I/O
  - I2C bus
  - FWIOs
- 49-pin WLCSP packages

For iDevice, it is necessary to become a licensee of Apple Inc.

Serial Audio Interfaces Formats

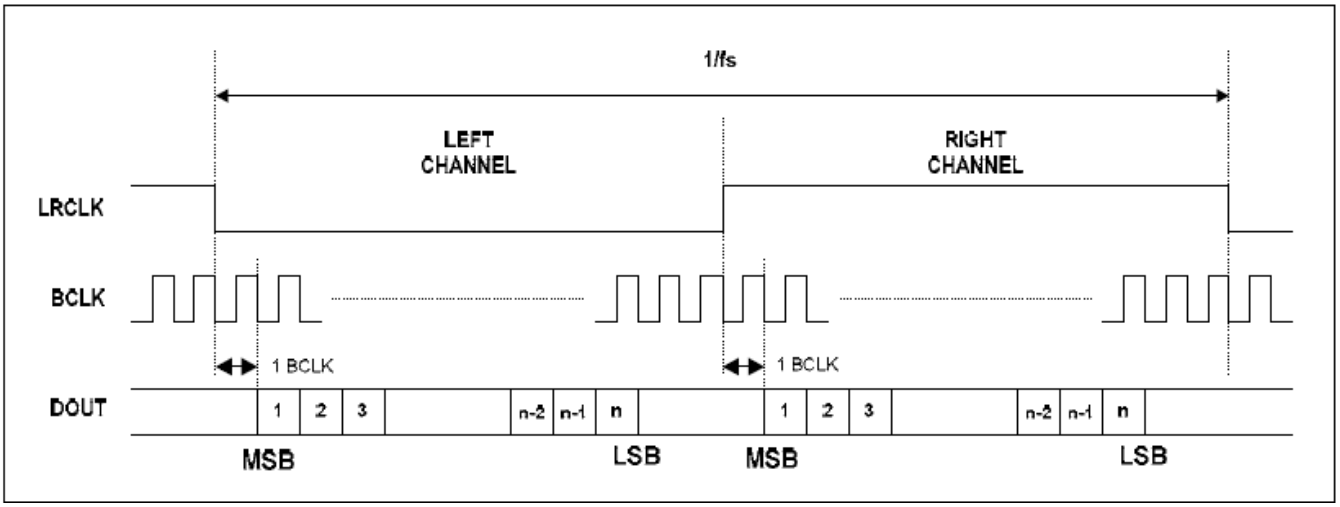
■ L-justified format:

In Left Justified mode, the MSB is available on the first rising edge of BCLK following an LRCLK transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles before each LRCLK transition.



■ I2S format

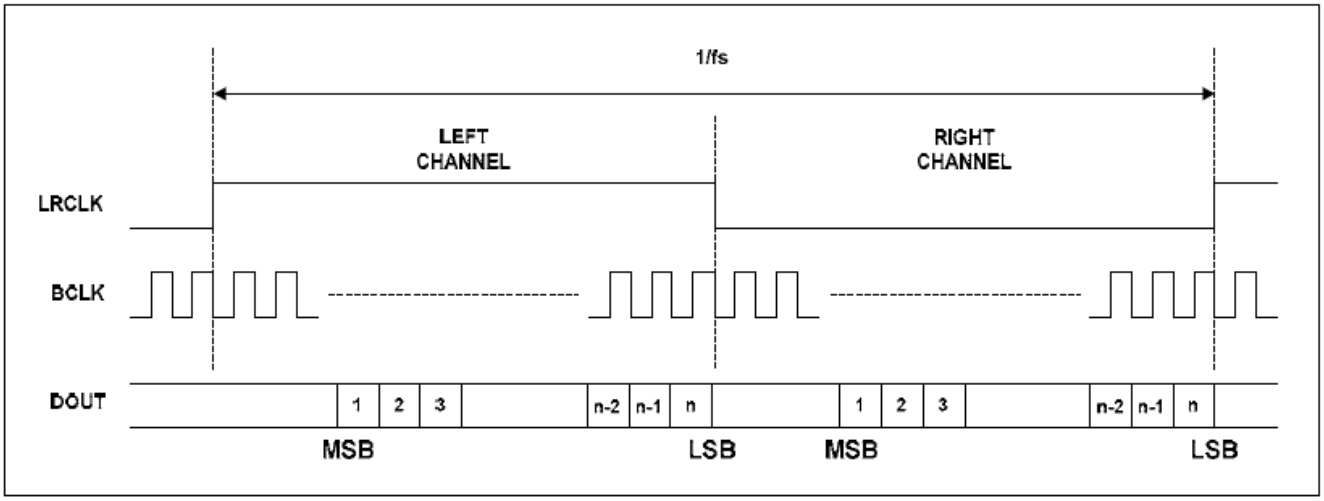
In I2S mode, the MSB is available on the second rising edge of BCLK following an LRCLK transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles between the LSB of one sample and the MSB of the next.



Serial Audio Interfaces Formats

■ R-justified format

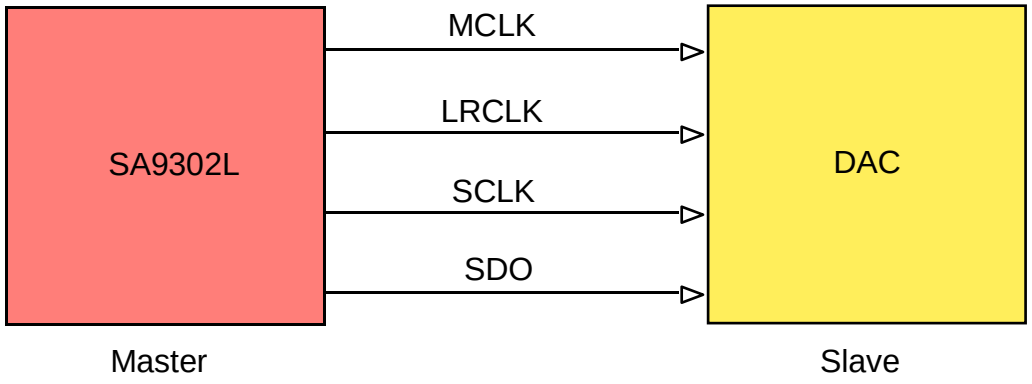
In Right Justified mode, the LSB is available on the last rising edge of BCLK before an LRCLK transition. All other bits are transmitted before (MSB first). Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles after each LRCLK transition. In Right Justified mode, the LSB is available on the last rising edge of BCLK before an LRCLK transition. All other bits are transmitted before (MSB first). Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles after each LRCLK transition.



Serial Audio Interfaces Configuration-DAC

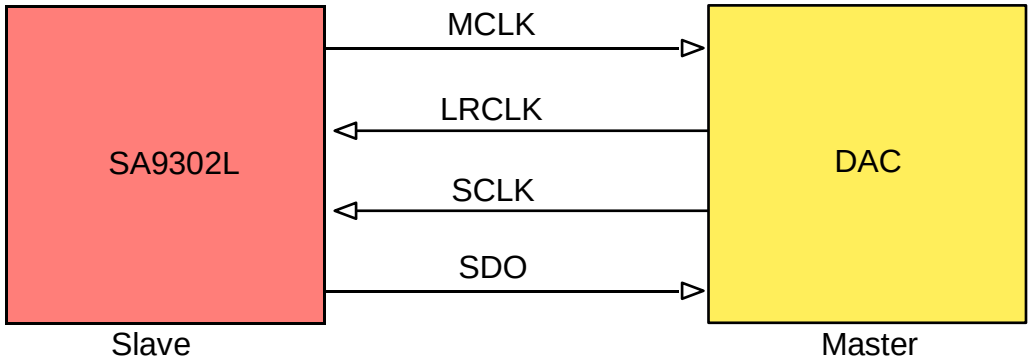
■ SA9302L supports both master mode and slave mode for following configurations.

■ **Master Mode**



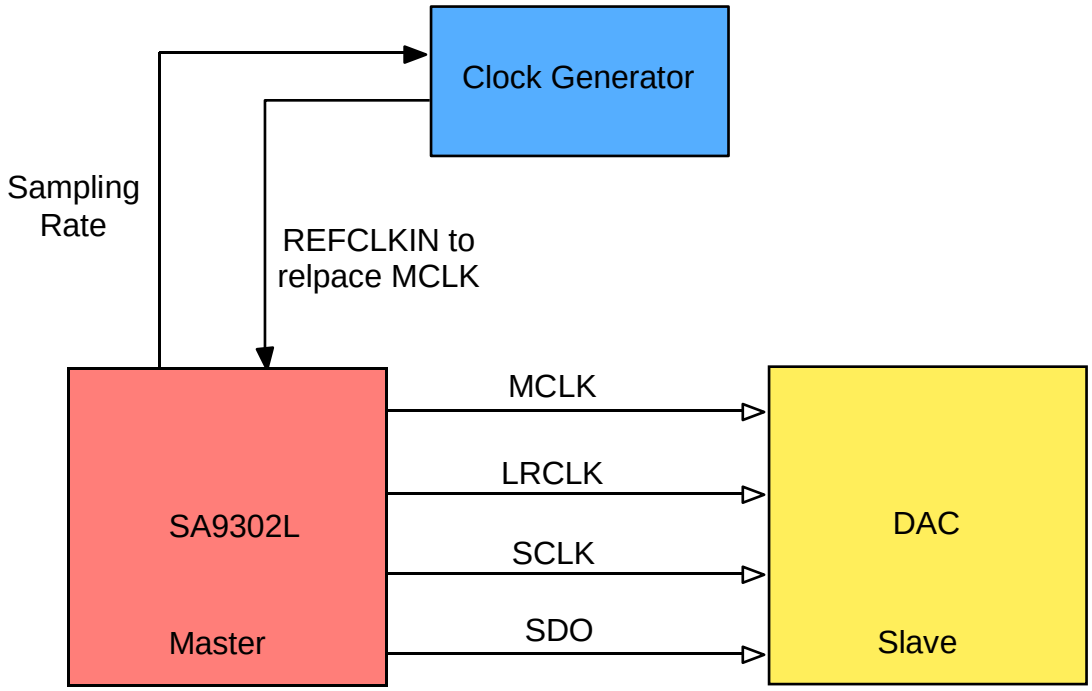
SA9302L I2S Master Mode connection

■ **Slave Mode**

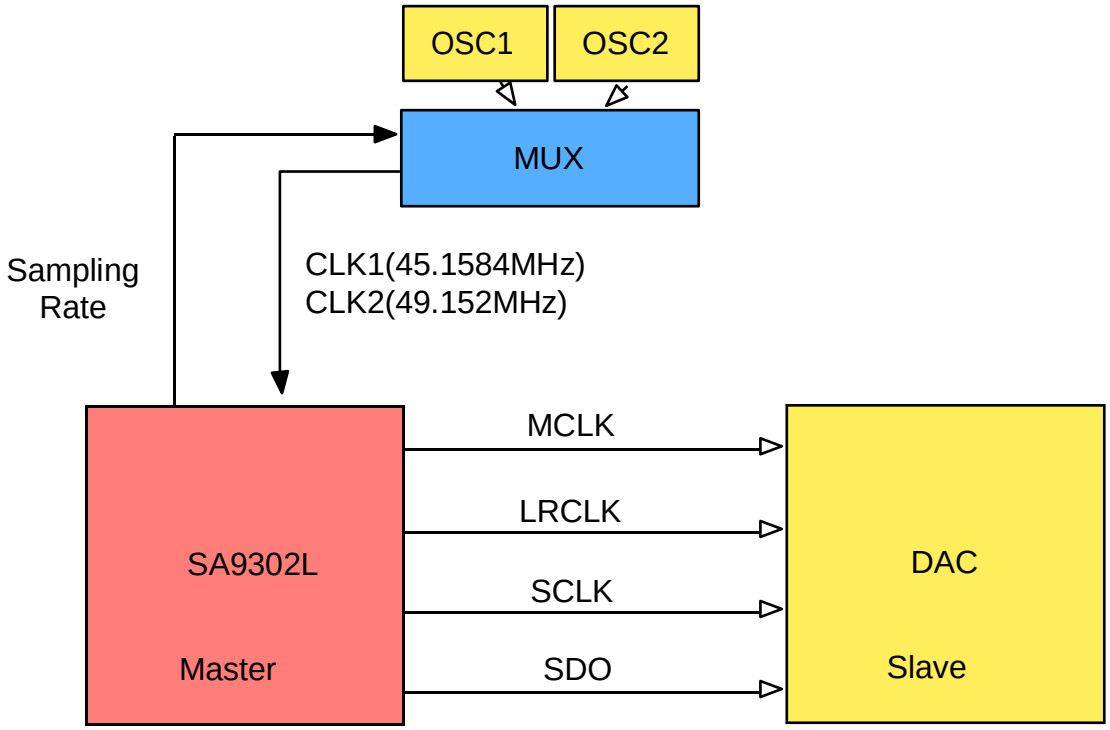


SA9302L I2S Slave Mode connection

Serial Audio Interfaces Configuration-DAC

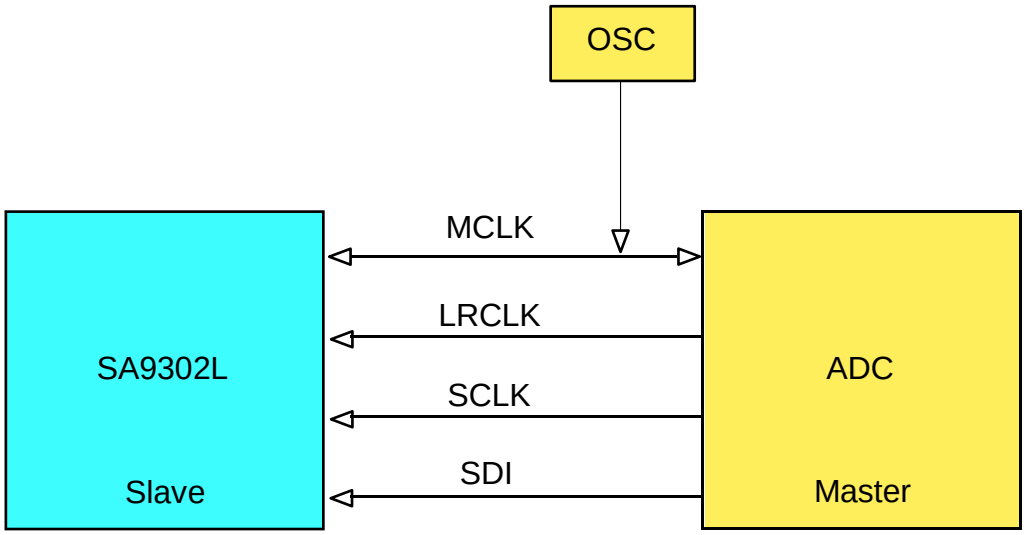


Master Mode (with external REFCLKIN), Mode 0



Master Mode (with external REFCLKIN), Mode 1

Serial Audio Interfaces Configuration-ADC



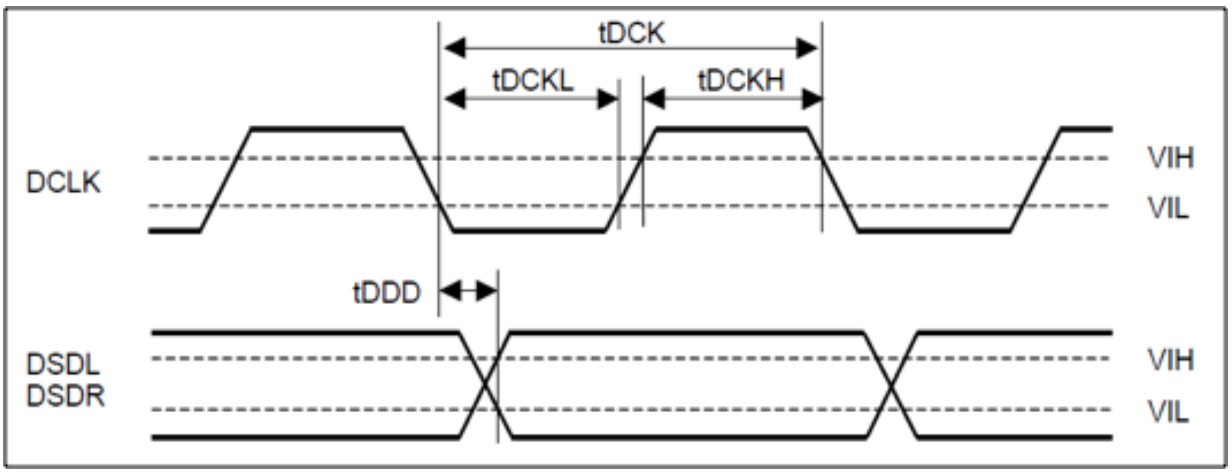
DSD Audio Data Interfaces

Playback:

SA9302L supports five modes for playback DSD data over USB Audio stream

Supported DSD formats:

■ DSD 64 for 88.2K 32-bit	DCLK(@2.8224MHz)	Direct-DSD
■ DSD 128 for 176.4K 32-bit	DCLK(@5.6448MHz)	Direct-DSD
■ DSD 256 for 352.8K 32-bit	DCLK(@11.2896MHz)	Direct-DSD
■ DSD 64 for 176.4K 24-bit	DCLK(@5.6448MHz)	DoP/dCS
■ DSD 128 for 352.8K 24-bit	DCLK(@11.2896MHz)	DoP/dCS



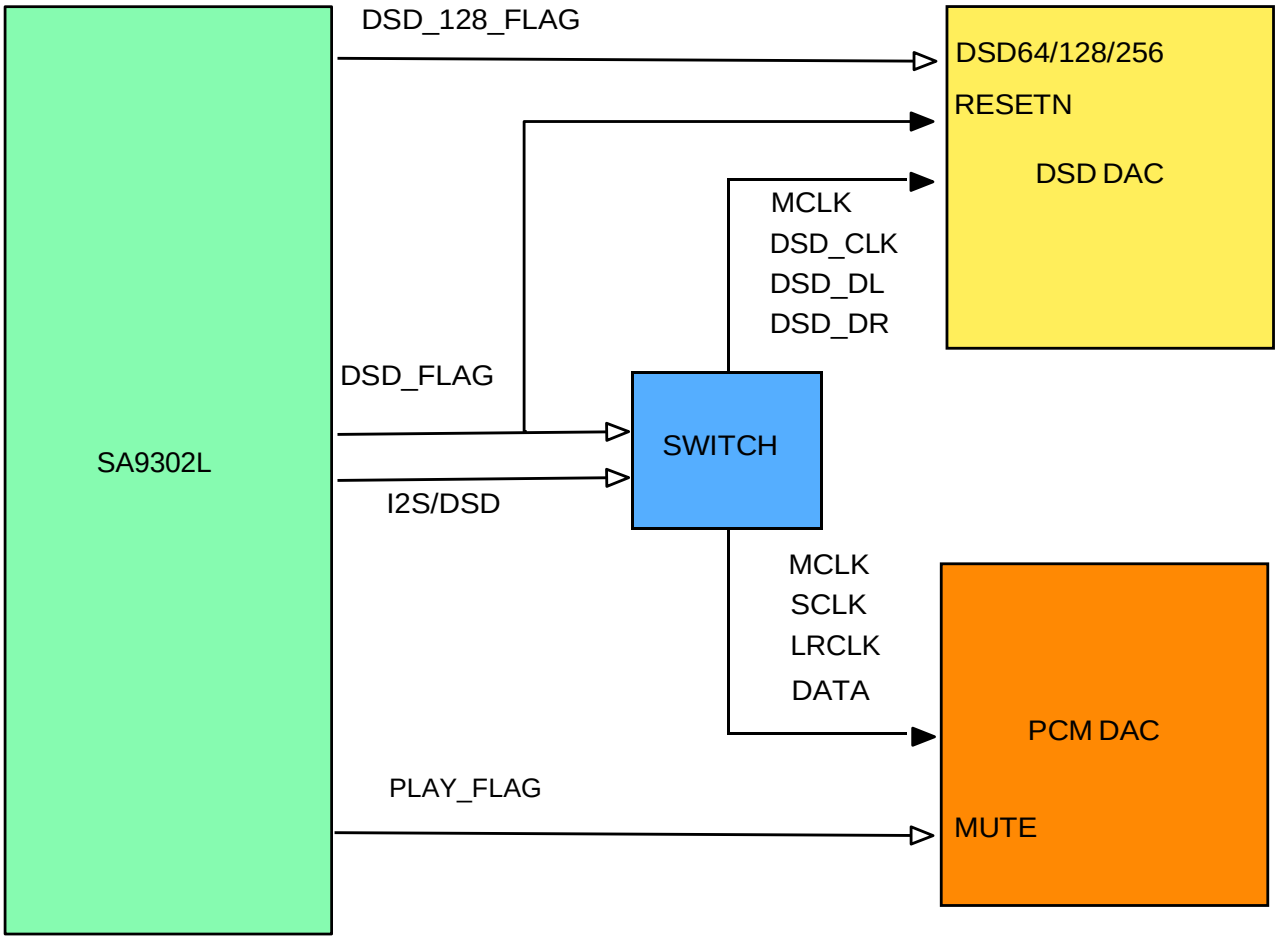
The DSDL and DSDR are all output by negative edge of DCLK. And DSD DAC will sample them by post edge of DCLK.

DSD External Control Signals

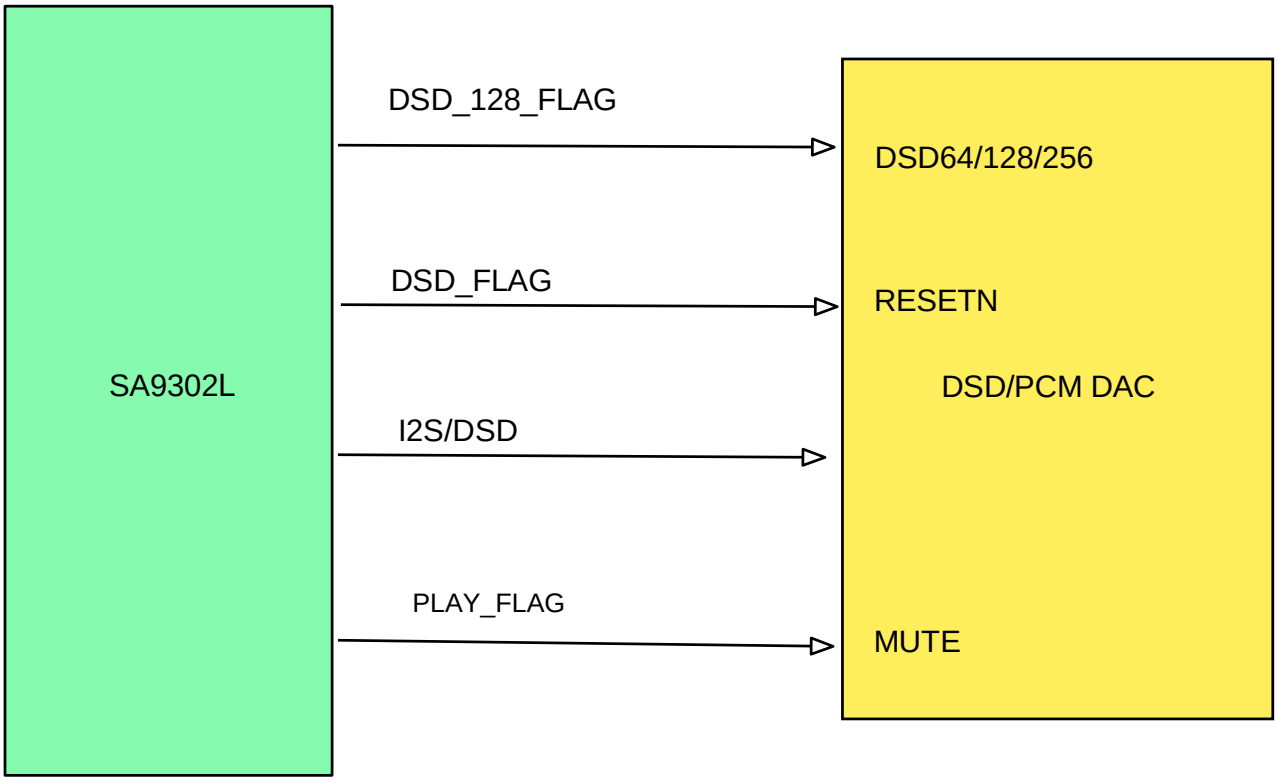
- DSD_FLAG : (0 : RESET, 1: Normal Operation in DSD format):
  Used to RESETN DSD DAC.

- DSD_FLAG : (0 : in PCM mode, 1: in DSD mode):
  used to switch DSD or PCM DAC.

- DSD_128 : (0 : in DSD 64 mode, 1: in DSD 128 mode):
  used to switch DSD64 and DSD128 format for DSD DAC.



Application with PCM DAC and DSD DAC

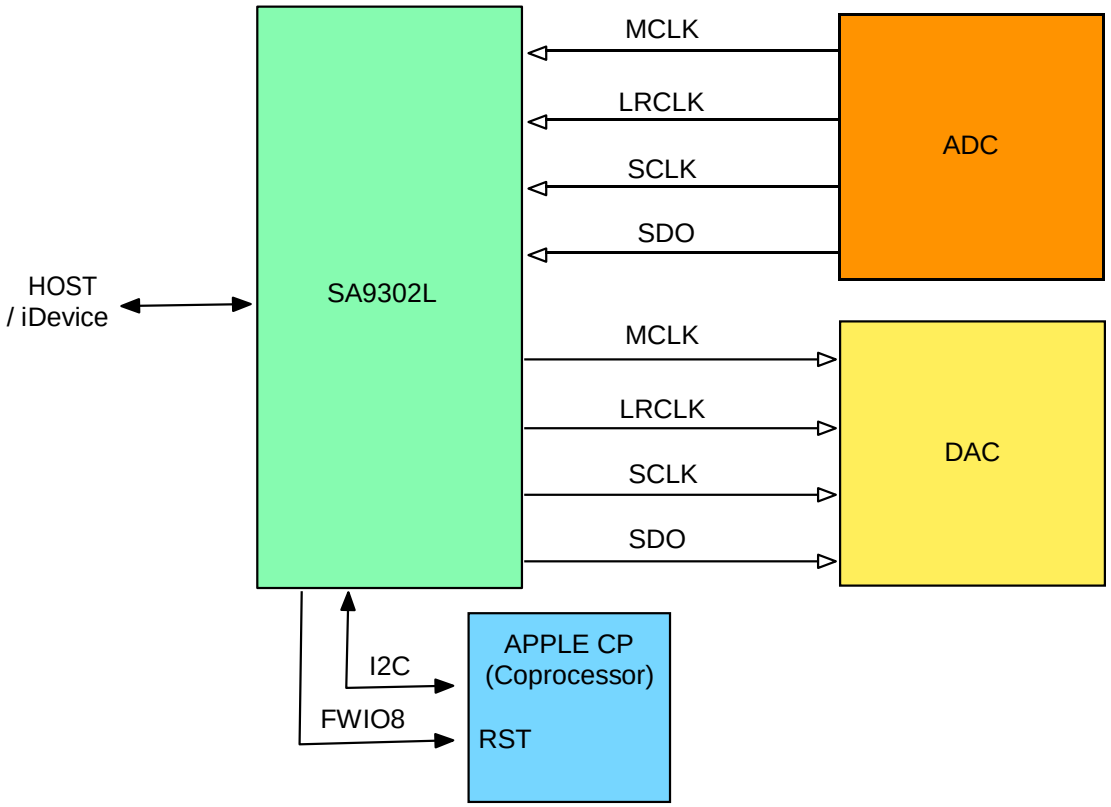


Application with PCM/DSD multi function DAC

iDevice support

Apple strongly recommends the use of digital audio paths to and from accessories. Apple device in USB Host Mode audio is the recommended approach. SA9302L will authenticate and identify itself to Apple device using iAP1/iAP2 CP before the iDevice will enumerate and start using USB Audio interface.

- Support 16 /24-bit linear PCM
- Support 44.1 / 48KHz sampling rate and up to 384KHz for future.
- Support input and output audio interface
- Support Volume Control Feature Unit
- Support iAP1 and iAP2 by CP2.0B and CP2.0C.



Digital USB Audio Application for iDevice

For using of SA9302L on iDevice, It is necessary to become a licensee of Apple Inc. regarding "Made for iPod/iPhone/iPad License".

S/PDIF TX Interfaces

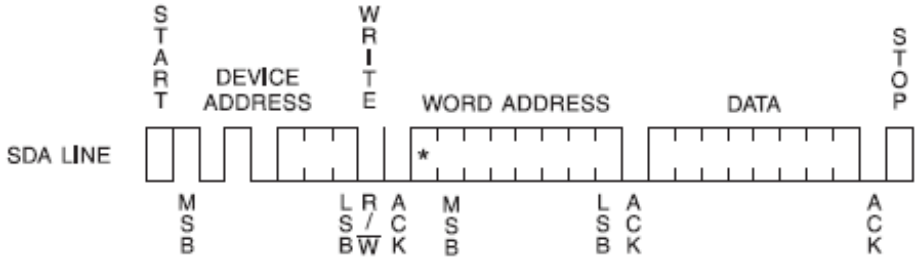
SA9302L support one S/PDIF TX interfaces, each can support up to 24-bit 384K sampling rate. Built in IEC60958 professional S/PDIF TX

- AES/EBU supported
- DSD stream output on S/PDIF TX
- 32/ 44.1/ 48/ 88.2/ 96/ 176.4/ 192/ 325.8/ 384KHz sampling rates
- 16/24 bit resolution

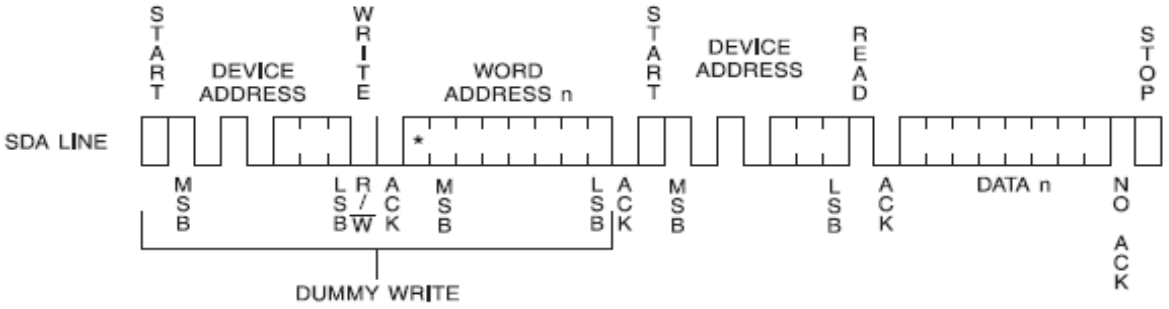
I²C Master Interfaces

One serial I²C master is supported in SA9302L to control external peripheral devices (EEPROM). SA9302L need an EEPROM to load Firmware code from it to SA9302L support use I²C Master Interfaces to read/write CP to support Apple MFi.

Byte Write



Random Read



Chip Status Flags

SA9302L provide these pins for display chip status flag

FLAGs	Definition
SOF_FLAG	User can check this pin to understand USB is in suspend or not 0: USB is in suspend 1: USB is in normal mode
DSD_FLAG	User can check this pin to understand DSD mode is detected or not 0: PCM mode 1: DSD mode
DSD_128_FLAG	User can check this pin to understand which DSD mode is played now (DSD64 or DSD128 mode) 0: DSD 64 mode 1: DSD 128 mode
USB_HS_FLAG	User can check this pin to understand which USB mode is running now 0: Full Speed 1: High Speed
PLAY_FLAG	User can check this pin to understand which playback status 0: Stop 1: Play

Pin Assignment - Ball Side Up View

7	6	5	4	3	2	1	
VDD_LDO	TEST0	NC3	REFCLKIN	ADATA	SPDIFTX	DLRCK	A
VDD18	GND	NC1	ALRCK	ABCLK	DDATA	GND	B
VDD33	TEST1	NC4	AMCLK	DMCLK	DBCLK	SDA_M	C
SOF_FLAG	DSD_FLAG	VDD18	FWIO8	RESET	SCL_M	VDD33	D
USB_HS_FLAG	DSD_128_FLAG	GND	VDD18	FWIO5	FWIO6	FWIO7	E
VDD33P	REXT	XI	VDD18U	PLAY_FLAG	REFCLKSEL	FWIO4	F
DP	DM	XO	VDD33PLL	FWIO0	GND	FWIO2	G

Pin Description

Pin	Name	I / O	Description
A7	VDD_LDO	P	LDO 3.3V input
B7	VDD18	P	Connect to 1.8V or connect 1uF capacitor to GND
D7	SOF_FLAG	O	USB Start-Of-Frame indicator
D6	DSD_FLAG	O	DSD/PCM indicator
E6	DSD_128_FLAG	O	DSD64/DSD128 indicator
E7	USB_HS_FLAG	O	USB speed indicator
F3	PLAY_FLAG	OD	Playback indicator
F6	REXT	I	Connect 270ohm resistor to ground
F7	VDD33P	P	USB2.0 PHY 3.3V power
F4	VDD18U	P	USB2.0 PHY 1.8V power
E5	GND	P	USB2.0 PHY ground
G7	DP	I/O	USB2.0 signals
G6	DM	I/O	USB2.0 signals
F5	XI	I	12MHz X'stal input
G5	XO	O	12MHz X'stal output
G3	FWIO0	OD	Firmware assign function I/O port *1
G1	FWIO2	OD	Firmware assign function I/O port *1
F1	FWIO4	OD	Firmware assign function I/O port *1
E3	FWIO5	OD	Firmware assign function I/O port *1
E2	FWIO6	OD	Firmware assign function I/O port *1
E1	FWIO7	OD	Firmware assign function I/O port *1
D4	FWIO8	OD	Firmware assign function I/O port *1
D3	RESET	I	Power-on reset signal (Active low)
D2	SCL_M	O	Master I2C clock
C1	SDA_M	I/O	Master I2C data

*1 All FWIOs are firmware assign function input/output, contact FAE to customize.

Pin	Name	I / O	Description
C3	DMCLK	I/O	I2S output MCLK
C2	DBCLK / DSD_CLK	I/O	I2S output BCLK / DSD_CLK
A1	DLRCK / DSD_LEFT	I/O	I2S output LRCLK / DSD_LEFT
B2	DDATA / DSD_RIGHT	O	I2S ouput DATA / DSD_RIGHT
A2	SPDIFTX	O	S/PDIF TX output
C4	AMCLK	I/O	I2S input MCLK
B3	ABCLK	I/O	I2S input BCLK
B4	ALRCK	I/O	I2S input LRCK
A3	ADATA	I	I2S input DATA
A4	REFCLKIN	I	External reference clock input
F2	REFCLKSEL	OD	External reference clock select
B5	NC1	I	Normal Operation. Needs pull-high
A5	NC3	I	Normal Operation. Needs pull-low
C5	NC4	I	Normal Operation. Needs pull-low
A6	TEST0	I	Normal Operation. Needs pull-low
C6	TEST1	I	Normal Operation. Needs pull-low
C7	VDD33	P	3.3V Power
D1	VDD33	P	3.3V Power
G4	VDD33PLL	P	3.3V PLL Power
D5	VDD18	P	1.8V Core power
E4	VDD18	P	1.8V Core power
B1	GND	P	Ground
B6	GND	P	Ground
G2	GND	P	Ground

DC Characteristics

Test Conditions: Ta = 25°C; VDD33 = +3.0 ~ +3.6V; fs = 48 kHz-32bit sine wave

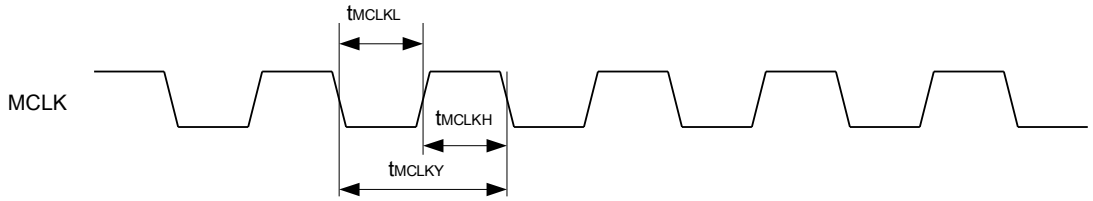
Parameter	Symbol	Test Condition	Min.	Max.	Unit
Input Low Voltage	VIL	VD33 = 3.3V		0.3*VDD33	V
Input High Voltage	VIH	VDD33 = 3.3V	0.7*VDD33		V
Output Low Voltage	VOL	IOL = 2mA		0.2	V
Output High Voltage	VOH	IOH = ---2mA	VDD33---0.2		V
Input Low Leakage Current	IIL	VIN = 0V VDD33 = 3.6V	---10	10	uA
Input High Leakage Current	IIH	VIN = 3.6V VDD33 = 3.6V	---10	10	uA
Operation Current	Idle*1	VDD33 = 3.3V VDD18 = Ext. DC-DC		30	mA
Operation Current	up to 192KHz *1 Playback	VDD33 = 3.3V VDD18 = Ext. DC-DC		45	mA
Operation Current	up to 384KHz & DSD *2 Playback	VDD33 = 3.3V VDD18 = Ext. DC-DC		109	mA
Suspend Current	Suspend	Total 3.3V rail	2	3	mA
		Total 1.8V rail	2	3	

*1 The power mode is controlled by F/W. This mode can not support DSD.
*2 Support DSD up to DSD128 by DoP and DSD256 by native DSD.

AC Timing Characteristics

Test Conditions: Ta = 25°C; VDD33 = +3.0 ~ +3.6V; fs = 48 kHz-32bit sine wave

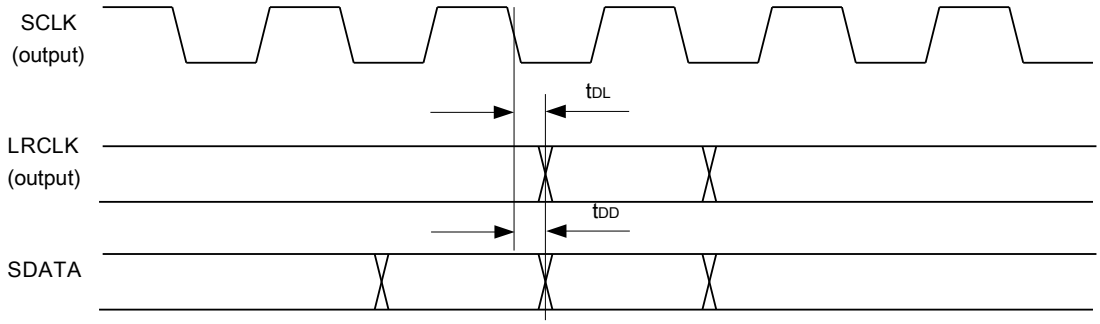
1. System Clock Timing



Test Conditions: VDD = 3.3V, VSS = 0V, TA = +25°C, Master Mode fs = 48kHz, MCLK = 256fs, 24---bit data.

Parameter	Symbol	Min	Typ.	Max	Unit
MCLK System clock pulse width high	tMCLKL		41.13		ns
MCLK System clock pulse width low	tMCLKH		40.23		ns
MCLK System clock cycle time	tMCLKY		81.36		ns

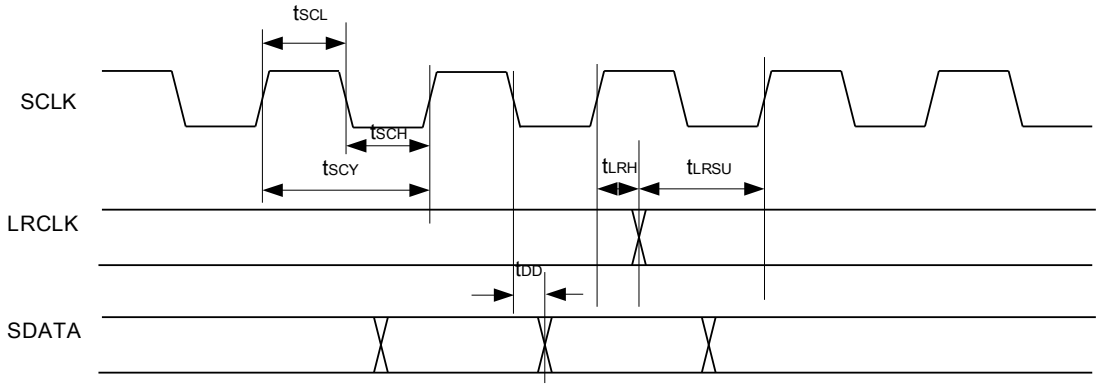
2. Audio Interface Timing – Master Mode



Test Conditions: VDD = V, VSS = 0V, TA = +25°C, Master Mode, fs = 48kHz, MCLK = 256fs, 24---bit data.

Parameter	Symbol	Min	Typ.	Max	Unit
LRCLK propagation delay from SCLK falling edge	tDL	5			ns
SDATA propagation delay from SCLK falling edge	tDDA	5			ns

3. Audio Interface Timing – Slave Mode



Test Conditions: VDD = V, VSS = 0V, TA = +25°C, Master Mode, fs = 48kHz, MCLK = 256fs, 24---bit data.

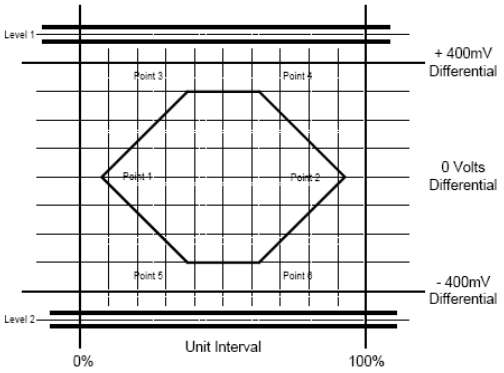
Parameter	Symbol	Min	Typ.	Max	Unit
SCLK cycle time	tSCY	293	325	358	ns
LRCLK pulse width high	tSCH	144	163	179	ns
SCLK pulse width low	tSCL	144	163	179	ns
LRCLK set---up time to SCLK rising edge	tLRSU	10			ns
LRCLK hold time from SCLK rising edge	tLRH	10			ns
SDATA propagation delay from SCLK falling edge	tDD	5			ns

Dynamic Electrical Characteristics: (DP/DM)

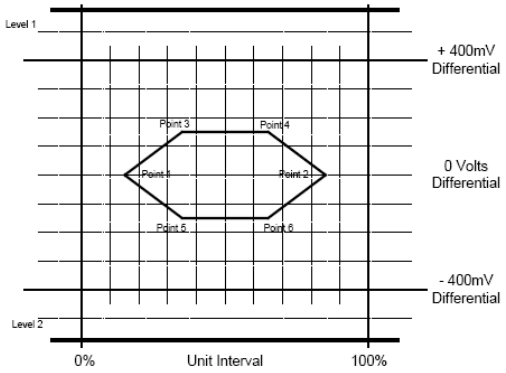
Driver Characteristics:

Symbol	Parameter	Min	Max	Unit
High---speed Mode				
t_{HSR}	High---speed differential rise time (10%---90%)	500	---	ps
t_{HSF}	High---speed differential fall time (10%---90%)	500	---	ps
Full---speed Mode				
t_{FR}	Rise Time for DP/DM	4	20	ns
t_{FF}	Fall Time for DP/DM	4	20	ns
t_{FRFM}	Differential rise/fall Time Matching (t_{FR} / t_{FF})	90	110	%
V_{CRS}	Output Signal Crossover Voltage	1.3	2.0	V

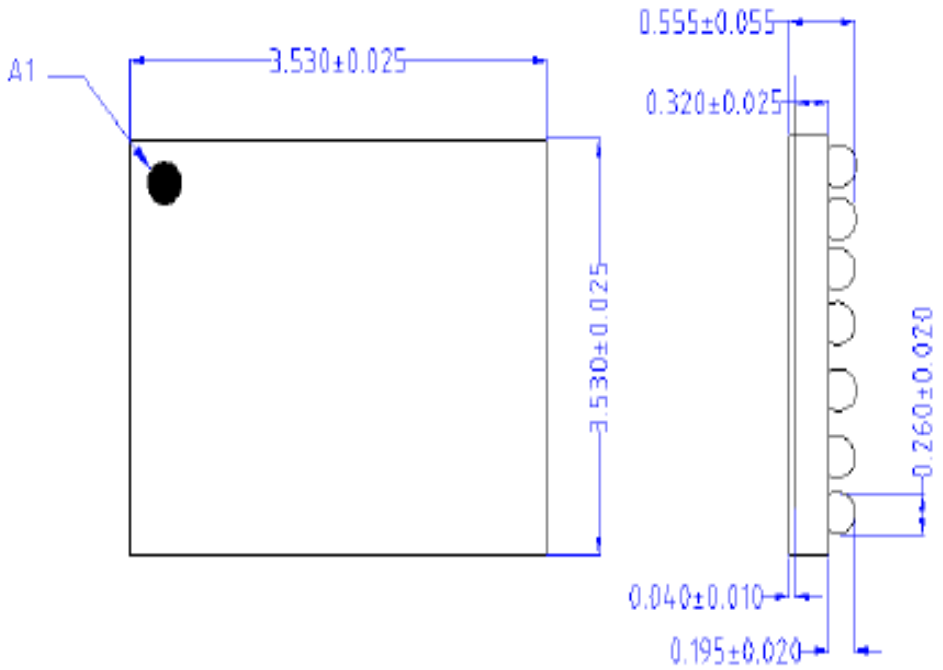
Driver Timing/Receiver timing:

Symbol	**Description**	**Condition**	**Min.**	**Typ.**	**Max.**	**Unit**
Driver timing						
High---speed mode						
Driver waveform requirement	See the eye pattern of template 1 (described in the USB 2.0 spec.) 					
	Follow template 1 described in USB specification Rev 2.0.					
Full---speed mode						

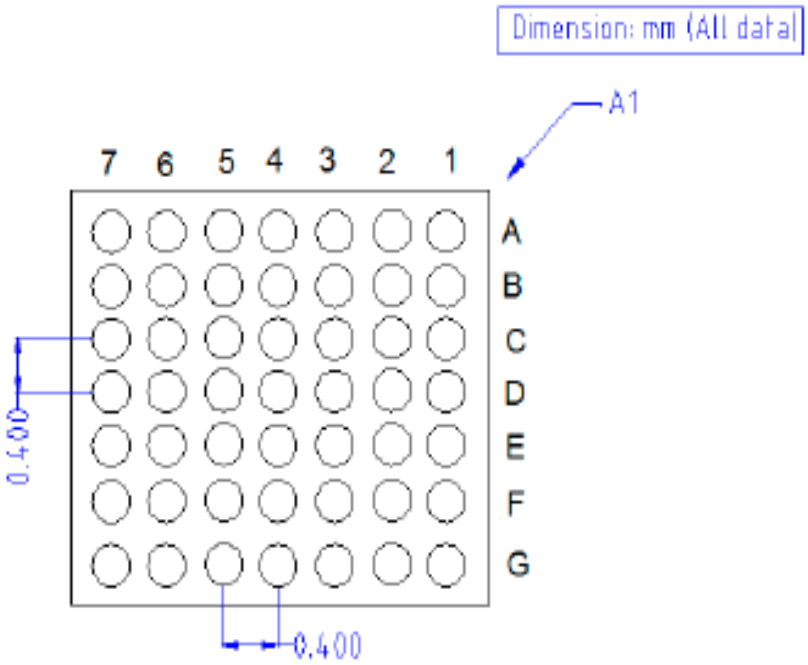
	Voltage Level (D+ - D-)	Time (% of Unit Interval)
Level 1	525 mV in UI following a transition, 475 mV in all others	N/A
Level 2	-525 mV in UI following a transition, -475 in all others	N/A
Point 1	0 V	7.5% UI
Point 2	0 V	92.5% UI
Point 3	300 mV	37.5% UI
Point 4	300 mV	62.5% UI
Point 5	-300 mV	37.5% UI
Point 6	-300 mV	62.5% UI

<table>
<tr><td>Propagation delay (VI, FSE 0, OE to DP, DM)</td><td>For the detailed description of VI, FSE 0, and OE, (please refer to the USB 1.1 spec.)</td><td colspan="2">…</td><td>…</td><td>15</td><td>ns</td></tr>
<tr><td colspan="7">Receiver timing</td></tr>
<tr><td colspan="7">High---speed mode (template 4, USB 2.0 spec.)</td></tr>
<tr><td>Data source jitter and receiver jitter tolerance</td><td colspan="2">See the eye pattern of template 4 (described in the USB 2.0 spec.)
 
</td><td colspan="4">Follow template 4 described in USB specification Rev 2.0.
<table><tr><th></th><th>Voltage Level (D+ - D-)</th><th>Time (% of Unit Interval)</th></tr><tr><td>Level 1</td><td>575 mV</td><td>N/A</td></tr><tr><td>Level 2</td><td>-575 mV</td><td>N/A</td></tr><tr><td>Point 1</td><td>0 V</td><td>15% UI</td></tr><tr><td>Point 2</td><td>0 V</td><td>85% UI</td></tr><tr><td>Point 3</td><td>150 mV</td><td>35% UI</td></tr><tr><td>Point 4</td><td>150 mV</td><td>65% UI</td></tr><tr><td>Point 5</td><td>-150 mV</td><td>35% UI</td></tr><tr><td>Point 6</td><td>-150 mV</td><td>65% UI</td></tr></table></td></tr>
<tr><td colspan="7">Full---speed mode</td></tr>
<tr><td>$t_{PLH(rcv)}$
$t_{PHL(rcv)}$</td><td>Receiver propagation delay (DP; DM to RX_RCV)</td><td>For the detailed description of RCV, (please refer to the USB 1.1 spec.)</td><td>…</td><td>…</td><td>15</td><td>ns</td></tr>
<tr><td>$t_{PLH(single)}$
$t_{PHL(single)}$</td><td>Receiver propagation delay (DP; DM to VOP, VON)</td><td>…</td><td>…</td><td>…</td><td>15</td><td>ns</td></tr>
</table>

WLCSP-49 Mechanical Data



Bottom View
Ball Side Down



TOP VIEW
Ball Side Up