Discrete Opamps Revisited 2019 – Comparing Topologies

XEN Audio

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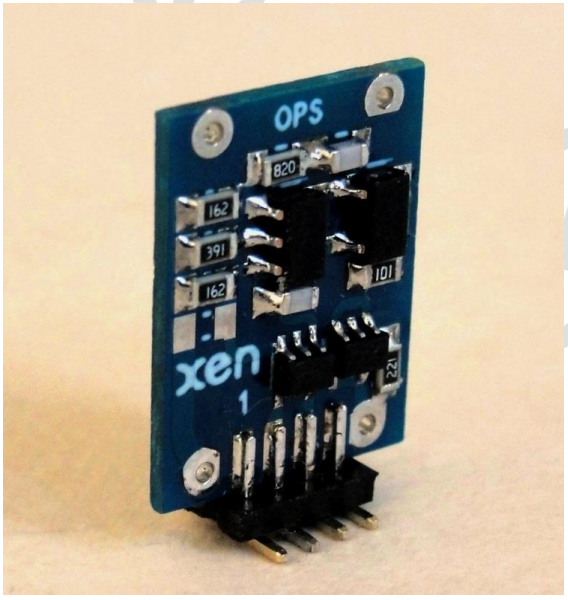

Background

As early as 2008, we have been making various attempts to build a discrete opamp in DIP8 package, with varying degrees of success. Our first attempt was an all FET design published by Nelson Pass [1].

While it did what it was supposed to, it did have a few problems preventing it from a wide field of application. The most obvious problem was DC thermal drift, especially during warm up. The next was its marginal stability for gain close to unity.

We had another attempt in 2012 in the discrete opamp open design thread still active till today [2]. Many circuits were discussed, but few were built, and almost none fits into a 10x10mm footprint. And not much was known about the thermal stability of those designs.

There are actually many discrete opamp's being offered on the market, even in dual versions. And some of them have excellent specs, using up to 30 transistors per opamp. But it is not only about specs, since commercial opamp's from TI, AD or LT are really difficult to beat in those terms, especially for what you get for the price. So why bother, you would say. Perhaps just for the challenge ?

We do believe that simple circuits, when properly done and especially operating in pure Class A, can sound better than those relying on high NFB to mask cross-over distortions. And yes, we like the challenge.

Design Requirements

During the year 2018, we went through the thinking again and again about what it should look like, what topology, and how to implement. First of all, a list of design requirements were defined :

1) Should fit a 10x10mm maximum footprint on standard DIL pin-out, ideally for both single and dual versions. Height can be up to 20mm including heat sinking. Working temperature should not exceed 60°C even for dual.

2) Stable at all gains from 1 to 10, both positive and negative. Gain margin should not be less than 20dB, and phase margin not less than 50°.
3) Open loop gain 50dB minimum at 1kHz, so that one can still get 30dB NFB at a gain of 10. Slew rate not less than 4V/µs.
4) Distortion < -85dB at gain = +10, 2Vrms out, 1kHz and 1k load. Distortion at 5kHz should not be more than 10dB higher than that at 1kHz, and relatively independent on load.
5) Total current consumption per channel < 20mA.
6) Max. Class A output current 8mA.
7) Output DC drift at gain of 10 should not exceed 10mV from cold (20°C) to steady state.
8) Input impedance > 1G.
9) Input noise < 4nV/√Hz at 1kHz.
10) Supply voltage +/-7V to +/-20V.

These specifications already dictate certain design choices, such as all SMD devices, JFET inputs, low component count, the need of a follower after the gain stage, and a thermally stable design, with lowish bias currents. For example, the minimum bias for the output stage has to be 8mA to satisfy requirement (6), leaving 12mA for the rest of the circuit.

Especially in symmetrical design topologies, dual devices should be used wherever possible to ensure good thermal tracking. That already puts a large constraint on the choice of components. When using SOT23 devices, the maximum dissipation should not be more than 80mW per device to ensure good reliability. That in turn means maximum 4mA bias with 20V rails.

Circuit Topology

A number of circuit topologies were considered and studied in detail with simulations :

A) MOX DOA (6 transistors, of which 2 duals, total 6mA bias)

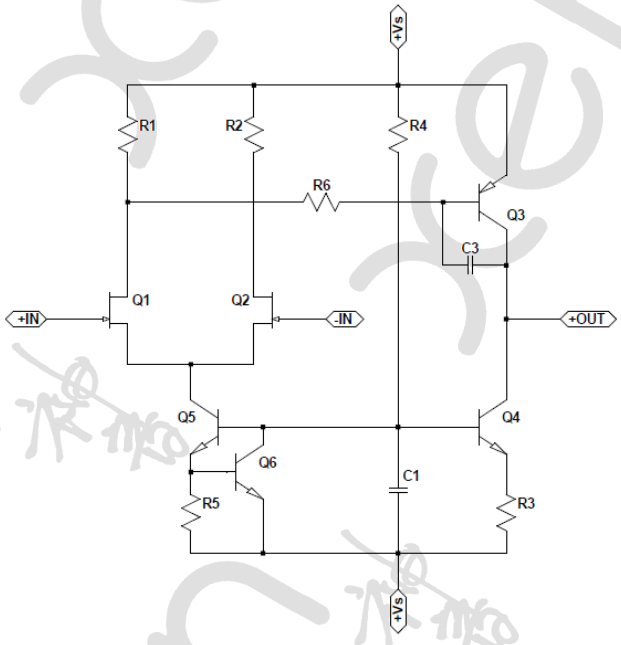

Fig. 1 MOX DOA Schematics

One of the well-known discrete opamp is that published at the MOX active crossover thread [3]. The same topology can also be found in many other publications. An example assembled in Spice using

exclusively active SMD devices and models indicates that it has good frequency characteristics and stability when not loaded. With 12mA bias, open loop gain is 65dB with a 10k load, with -3dB bandwidth at 800Hz. Close loop bandwidth at unity gain is 1MHz; phase margin is 60°, and gain margin is 40dB. Slew rate though is a bit low at 1V/µs, and can only be raised by increasing bias further.

The biggest drawback is, however, that the OL Gain drops by 20dB to only 45dB with a 1k load. Furthermore, the second stage is not a thermally symmetrical design. And warming of 2nd stage PNP can cause an estimated DC offset of 0.2V at a gain of 10.

B) XEN SOPA (9 transistors, of which 3 duals, total 11mA bias)

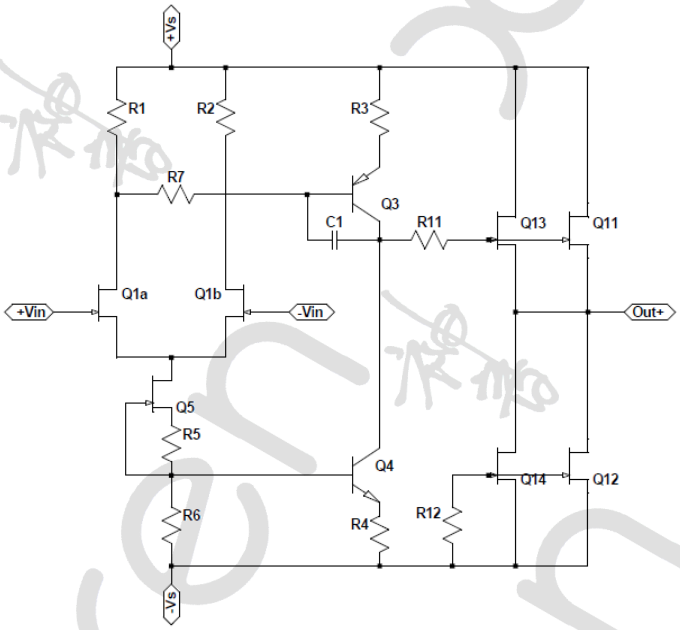

Fig. 2 XEN SOPA Schematics

The well proven practice to reduce load dependency is to add a follower stage after the gain stage. One can use a pair of complementary BJTs as emitter followers. But this would require a biasing circuit and also thermal coupling to avoid thermal run-away. In that respect, a dual N-JFET source follower is a better choice unless there is a necessity to drive heavy load.

To solve the thermal drift issue, a symmetrical 2nd stage and a ratio-metric 1st stage is implemented for both top & bottom halves. In the first stage, the drain resistor of each leg of the LTP is nominally 2x of that below the CCS (R6). The former biases the 2nd stage PNP, and the latter the 2nd stage NPN. Both 2nd stage degeneration resistors are of the same value. As such, the gain stage is thermally symmetrical by design.

With reduced bias at the gain stages, a 12mA-bias gives an open loop gain is 75dB with a 10k load, with -3dB bandwidth at 900Hz. Close loop bandwidth at unity gain is now at 3MHz; phase margin is 60°, and gain margin is 20dB. Slew rate is greatly improved to 4V/µs. There is now essentially no drop in OLG with a 1k load. A much-improved design compared to the MOX.

C) EB602 + Follower (11 transistors, of which 4 duals, total 10mA bias)

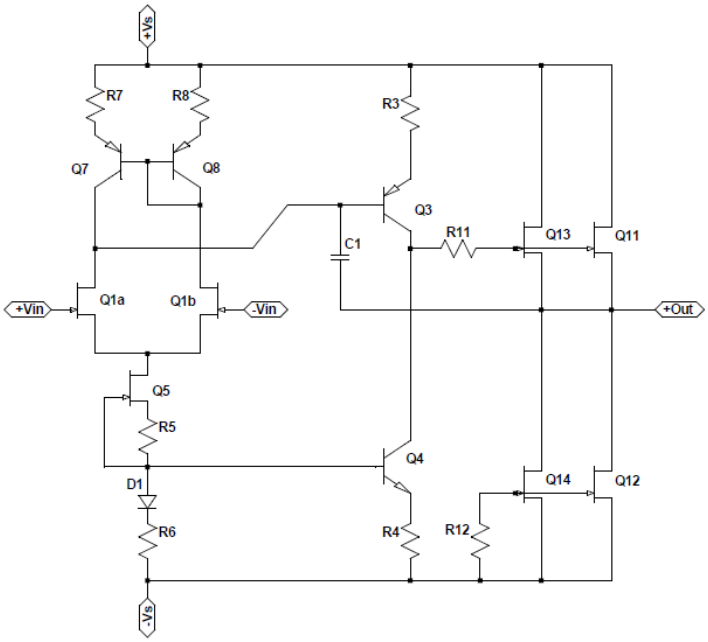

Fig. 3 EB602+F Schematics

A variant of the MOX topology is the Borbely EB602 [4]. Similar but different to MOX, this uses a current mirror for 1st stage for additional open-loop gain. We modified this by incorporating an additional output follower, as well as thermal symmetry in the XEN SOPA. With the current mirror, open loop gain is as high as 110dB OLG, requiring heavy compensation for unity gain stability, at only 12Hz OL bandwidth. Unity gain bandwidth is at 2MHz, with a phase margin 40°, and gain margin -15dB. It is similar to many commercial opamps with “low distortion”, relying on very high OLG but low OL bandwidth to ensure stability.

D) Kaneda Quasi-Push-Pull (8~10 transistors, of which 3 or 4 duals, total 10~14mA bias)

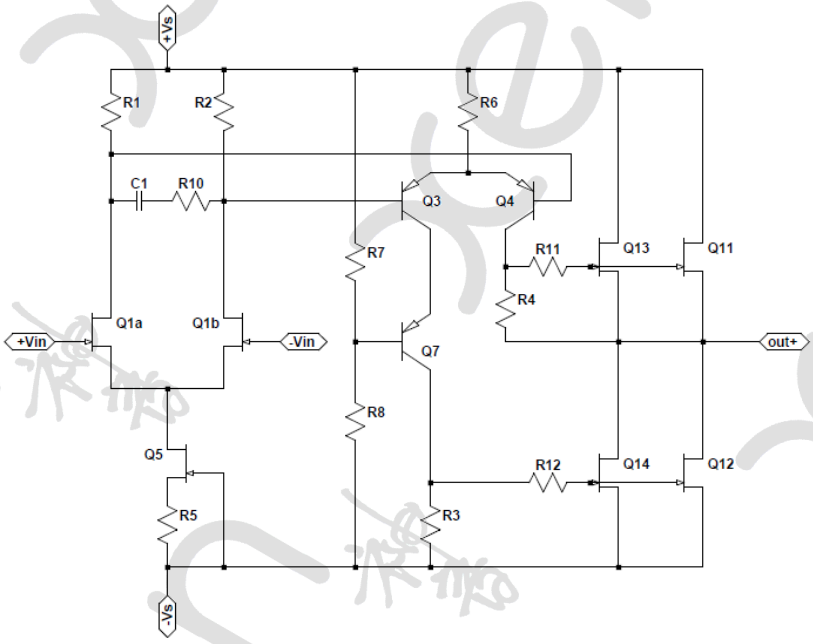

Fig. 4 Kaneda OPA Schematics

Very popular in Japan, and attempted by us in 2012 [5], is the Kaneda quasi-push-pull topology. By using quasi-push-pull at the output stage, the Class A output current can be 2x that of bias. So one can actually save one pair of output devices. An additional cascode transistor on 2nd stage greatly improves thermal symmetry of Q3 & Q4, but at the expense of PSRR.

When compensated for unity gain stability, open loop gain is 80dB, with -3dB bandwidth at 500Hz. Unity gain is at 2.2MHz, phase margin 45°, and gain margin 25dB. Slew rate is somewhat low at 2.4V/µs.

E) JC Pro-1 (11 transistors, of which 5 duals, total 16mA bias)

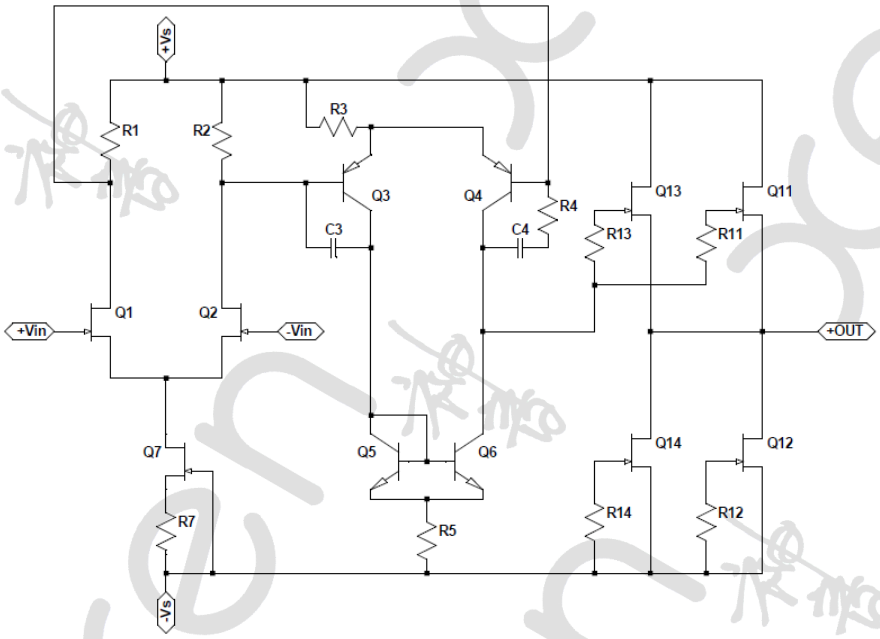

Fig. 5 JC Pro-1 OPA Schematics

This topology follows that of the LH0032 IC, or the discrete JC Pro-1 opamp module [6]. Unfortunately, both of them were not unity gain stable. In order to have enough compensation for unity gain stability, open loop bandwidth has to be reduced somewhat to 300Hz. But this is made up by the open loop gain of 87dB. Unity gain bandwidth is 4MHz, with 63° phase margin, 25dB gain margin. Slew rate is at 4.5V/µs.

F) AD797-JFET (9 transistors + 1 LED, of which 4 duals, total 18mA bias)

A similar but different topology to the JC Pro-1 is also widely discussed and used in some commercial offerings. This differs from the JC topology in that instead of using a resistor-loaded diff pair first stage to drive a current-mirror-loaded diff pair second stage, a folded cascode is used instead. This topology was also used in various commercial products, such as Marantz HDAM, Luxman C-02 & M-02 [7]. But in actual fact, this is essentially the same topology as the famous AD797, but with JFET inputs. One can also find such cascoded opamp topology in almost any university lecture notes for analogue electronics.

The original circuit is not unity gain stable. And the circuit does not offer much choice for compensation locations. When uncompensated, open loop bandwidth can be very high (> 10kHz), but is unstable for gain below 100x. Internal compensation can bring this down to unity gain stable, at the

expense of OLG bandwidth. Open loop gain is 73dB with 1.1kHz bandwidth, unity gain 3MHz, with phase margin at 80°, and gain margin at 28dB. Slew Rate is 4V/µs. A slight disadvantage compared to the JC is slightly earlier voltage clipping.

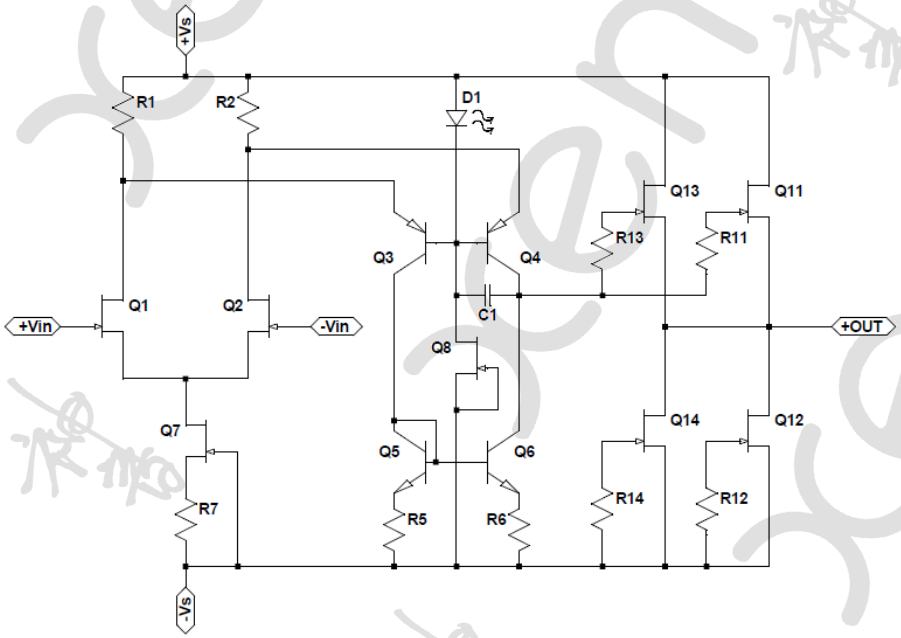

Fig. 6 J-797 OPA Schematics

Summary

Without claim that all the sweet spots were hit in terms of device choice, bias, and compensation, the best overall performance are to be had from the JC Pro-1, J-797 and the XEN SOPA topologies. So these were chosen for hardware implementation and tests.

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