AV RECEIVER/AV AMPLIFIER

RX-V459/HTR-5940/DSP-AX459
HTR-5935

SERVICE MANUAL

IMPORTANT NOTICE

This manual has been provided for the use of authorized YAMAHA Retailers and their service personnel.
It has been assumed that basic service procedures inherent to the industry, and more specifically YAMAHA Products, are already known and understood by the users, and have therefore not been restated.

WARNING: Failure to follow appropriate service and safety procedures when servicing this product may result in personal injury, destruction of expensive components, and failure of the product to perform as specified. For these reasons, we advise all YAMAHA product owners that any service required should be performed by an authorized YAMAHA Retailer or the appointed service representative.

IMPORTANT: The presentation or sale of this manual to any individual or firm does not constitute authorization, certification or recognition of any applicable technical capabilities, or establish a principle-agent relationship of any form.

The data provided is believed to be accurate and applicable to the unit(s) indicated on the cover. The research, engineering, and service departments of YAMAHA are continually striving to improve YAMAHA products. Modifications are, therefore, inevitable and specifications are subject to change without notice or obligation to retrofit. Should any discrepancy appear to exist, please contact the distributor's Service Division.

WARNING: Static discharges can destroy expensive components. Discharge any static electricity your body may have accumulated by grounding yourself to the ground buss in the unit (heavy gauge black wires connect to this buss).

IMPORTANT: Turn the unit OFF during disassembly and part replacement. Recheck all work before you apply power to the unit.

■ CONTENTS

■ SELF DIAGNOSIS FUNCTION (DIAG)／自己診断機能（ダイアグ）

This unit has self diagnosis functions that are intended for inspection, measurement and location of faulty point.
There are 23 DIAG menu items, each of which has sub-menu items.
Listed in the table below are menu items and sub-menu items.
Note that not all menu items listed will apply to the models covered in this service manual.

本機には、検査、測定、不良個所の発見を目的にした自己診断機能（ダイアグ）があります。
ダイアグメニューは23個あり、そのそれぞれにサブメニューがあります。（ダイアグのメニュー操作は本体で行います。） 下表はメニュー一覧です。
下表の全メニュー項目が、このサービスマニュアル記載のモデルに適用されるとは限りません。

No.	MAIN MENU	SUB MENU
1	BYPASS	1. ANALOG BYPASS
		2. DSP BYPASS
2	RAM THR	1. RAM MARGIN
		2. RAM FULL BIT
3	PRO LOGIC	1. Pro Logic
4	SPEAKERS SET	1. FRONT : SMALL 0dB
		2. CENTER : NONE
		3. LFE/B : FRNT
		4. Pres Mix : 5ch
		5. Front GAIN 1
		6. Front GAIN 2
		7. SURR B Check
5	XCH-INPUT	1. XCH_INPUT_6
		2. XCH_INPUT_8
		3. LIMIT SET (Not applied to these models / このモデルには適用されません)
6	MIC CHECK (Not applied to these models / このモデルには適用されません)	1. MIC CHECK --dB
7	DISPLAY CHECK	1. STRAIGHT (Initial display)
		2. VFD DISP OFF
		3. VFD DISP ALL
		4. VFD DIMMER
		5. CHECK PATTERN
8	MANUAL TEST	1. TEST ALL
		2. TEST FRNT L
		3. TEST CENTER
		4. TEST FRNT R
		5. TEST SURR R
		6. TEST SB R (Not applied to these models / このモデルには適用されません)
		7. TEST SB L
		8. TEST SURR L
		9. TEST PRES L (Not applied to these models / このモデルには適用されません)
		10. TEST PRES R (Not applied to these models / このモデルには適用されません)
		11. TEST LFE
9	FACTORY PRESET	1. PRESET INHI (memory initialization inhibited)
		2. PRESET RSRV (memory initialized)
10	AD DATA CHECK	1. PS1/PS2
		2. DC/TH
		3. IMP SW/POWER LIMITER DISP
		4. PANEL KEY
11	VIDEO (Not applied to these models / このモデルには適用されません)	1. I2C Read Check
		2. DIGITAL THR CVBS
		3. DIGITAL THR Y/C
		4. ANALOG BYPASS
		5. TEST PATTERN
		6. LOOP BACK CVBS
		7. LOOP BACK Y/C
12	XM STATUS (U,C models)	1. 1k -1dB / 44.1k
		2. 1k -61dB / 44.1k
		3. Mute / 44.1k
		4. XM Tone / 44.1k
		5. ISO Tone / 44.1k
		6. 1k -1dB / 32k
		7. 1k -61dB / 32k
		8. Mute / 32k
		9. XM Tone / 32k
		10. ISO Tone / 32k
		11. XM / DT Bus Power : OFF
13	iPod	1. DOCK : OK/NG
16	IF STATUS	1. DSP STATUS (5Byte)
		2. DECODE MODE (2Byte) (Not applied to these models / このモデルには適用されません)
		3. DIR INFO (5Byte) (Not applied to these models / このモデルには適用されません)
		4. Pc (2Byte) (Not applied to these models / このモデルには適用されません)
		5. CHS 1 (5Byte) (Not applied to these models / このモデルには適用されません)
		6. CHS 2 (1Byte) (Not applied to these models / このモデルには適用されません)
		7. DEC INFO (5Byte) (Not applied to these models / このモデルには適用されません)
		8. BSI 1 (5Byte) (Not applied to these models / このモデルには適用されません)
		9. BSI 2 (5Byte) (Not applied to these models / このモデルには適用されません)
		10. BSI 3 (5Byte) (Not applied to these models / このモデルには適用されません)
		11. BSI 4 (5Byte) (Not applied to these models / このモデルには適用されません)
		12. BSI 5 (5Byte) (Not applied to these models / このモデルには適用されません)
		13. BSI 6 (5Byte) (Not applied to these models / このモデルには適用されません)
		14. BSI 7 (5Byte) (Not applied to these models / このモデルには適用されません)
		15. BSI 8 (1Byte) (Not applied to these models / このモデルには適用されません)
		16. Mute Trigger (5Byte) (Not applied to these models / このモデルには適用されません)
		17. Digital Info (5Byte) (Not applied to these models / このモデルには適用されません)
17	DSP BUS CHECK	1. TI (DSP) BUS CHECK
		2. RDS IC CHECK
18	SWFR CUT OFF (HTR-5935 model)	1. L CUT OFF
		2. H CUT OFF
19	PROTECTION SETTING (Not applied to these models / このモデルには適用されません)	1. PS L
		2. PS H
		3. DC L
		4. DC H
		5. TEMP
		6. PL_J_8_L
		7. PL_J_8_H
		8. PL_U_8_L
		9. PL_U_8_H
		10. PL_U_N_L
		11. PL_U_N_H
		12. PL_G_8_L
		13. PL_G_8_H
		14. PL_G_N_L
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20	PROTECTION HISTORY	1. HISTORY 1
		2. HISTORY 2
		3. HISTORY 3
		4. HISTORY 4
21	SOFT SW	1. SW MODE : PCB/MODEL/FNC
		2. MODEL : 759SE-5935
		3. DEST. : J/UC/R/T/K/A/BGE/L
		4. TUNER DEST : J/UC/ATKBG/RL
		5. TUNER TYPE : NRM/RDS/XM
		6. VIDEO FORMAT : NTSC/PAL
		7. ZONE2 EXIST : EXIST/NOT
		8. AAC EXIST : EXIST/NOT
		9. TUNER EXIST : EXIST/NOT
		10. ZONE2 AMP EXIST : EXIST/NOT
		11. OSD EXIST : EXIST/NOT
		12. YPAO EXIST : EXIST/NOT
22	ROM VER / SUM / PORT	1. MICROPROCESSOR VERSION
		2. SUM ALL / PROGRAM
		3. OPE / DSP / XM VERSION
		4. PORT
		5. TI (DSP) FLASH VERSION
		6. TI (DSP) FLASH SUM
		7. EEPROM SUM
23	TI (DSP) BOOT (Not applied to these models / このモデルには適用されません)	1. TI (DSP) FLASH BOOT

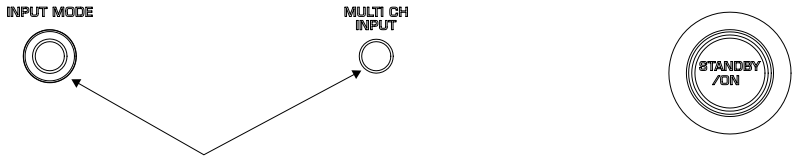
• Starting DIAG

Press the “STANDBY/ON” key while simultaneously pressing those two keys of the main unit as indicated in the figure below.

● ダイアグの起動

本体の下図に示すキーを同時に押しながら“STANDBY/ON”キーを押すと、ダイアグが起動します。

Keys of main unit / 本体キー



Turn on the power while pressing these keys.
これらのキーを同時に押しながら、パワーオンする。

• Starting DIAG in the protection cancel mode

If the protection function works and causes hindrance to trouble diagnosis, cancel the protection function as described below, and it will be possible to enter the DIAG mode. (The protection functions other than the excess current detect function will be disabled.)

Press the “STANDBY/ON” key while simultaneously pressing those two keys indicated in the figure above. At this time, keep pressing those two keys for 3 seconds or longer.

In this mode, the “SLEEP” segment of the FL display of the main unit flashes to indicate that the mode is DIAG mode with the protection functions disabled.

CAUTION!
Using this product with the protection function disabled may cause damage to itself. Use special care for this point when using this mode.

● プロテクション解除モードでの起動

プロテクションが動作することにより、故障箇所の診断に支障をきたすような場合は、次の方法によりプロテクションを解除した状態でダイアグモードに入ることができます。（過電流検出以外のプロテクション動作を解除する）

上図のキーを同時に押しながら“STANDBY/ON”キーを押します。このとき、上図のキーを3秒以上押し続けてください。
このモードでは本体FLの“SLEEP”セグメントが点滅し、プロテクションを解除した状態でのダイアグモードであることを知らせます。

注意！
プロテクションを解除した状態でのダイアグモードは、危険な状態でもプロテクションが作動しないため、動作させると、機器を破壊することがあります。このモードを使用する場合は十分注意してください。

• Canceling DIAG

① Before canceling DIAG, execute setting for FACTORY PRESET of DIAG menu No.9 (Memory initialization inhibited or Memory initialized).
   * In order to keep the user memory stored, be sure to select PRESET INHIBITED (Memory initialization inhibited).
② Turn off the power by pressing the “STANDBY/ON” key of the main unit.

● ダイアグの解除

① ダイアグを解除する前に、ダイアグメニューＮｏ.９のFACTORY PRESET（メモリーの初期化禁止/またはメモリーの初期化）の設定をします。
   ※ ユーザーメモリーを保持したい場合は、必ずPRESET INHIBITED（メモリー初期化禁止）を選択してください。
② 本体の“STANDBY/ON”キーを押し、パワーオフにします。

• Display provided when DIAG started

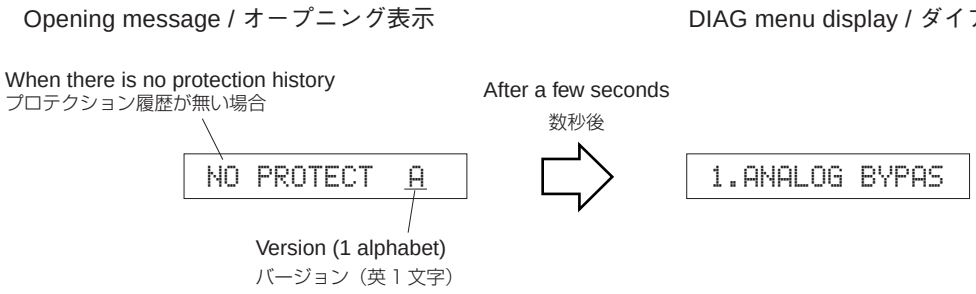
On the FL display of the main unit, an opening message (including the version and the protection history) appears for a few seconds followed by the diagnostic menu display (1. ANALOG BYPASS).

● ダイアグ起動時の表示

本体FLディスプレイには、オープニング(プロテクション履歴／バージョン)が表示され、数秒後にダイアグメニュー表示(1. ANALOG BYPASS)となります。

When there is no history of protection function:

プロテクション履歴が無い場合：



When there is a history of protection function:

The FL display appears as shown below depending on the type of the protection function.

プロテクション履歴がある場合：

プロテクションの種類によって下記の表示が現れます。

The protection function worked due to excessive current through the amplifier. Causes could be a short at the speaker terminal or a defect in the amplifier. The protection function activates immediately to turn off the power, with no history display at turn-on, if the amplifier is defective.

`I PROTECT A`

スピーカーをショートさせた時などが原因で、プロテクションが働いたことを示します。

The protection function worked due to a defect or overload in the power supply. If the power is turned on with the abnormality unsolved, the protection function works in about 1 second to turn off the power.

`PS1 PRT:000 A`
or
`PS2 PRT:000 A`

電源電圧による原因で、プロテクションが働いたことを示します。異常状態のままパワーオンすると、約1秒後にプロテクションが掛かり、電源が切れます。

The protection function worked due to a DC voltage appearing at the speaker terminal. A cause could be a defect in the amplifier. If the power is turned on with the abnormality unsolved, the protection function works in about 3 seconds to turn off the power.

`DC PRT:000 A`

アンプの故障でスピーカーに直流電圧が掛かるなどが原因で、プロテクションが働いたことを示します。異常状態のままパワーオンすると、約3秒後にプロテクションが掛かり、電源が切れます。

The protection function worked due to the temperature limit being exceeded. Causes could be poor ventilation or a defect related to the thermal sensor. If the power is turned on with the abnormality unsolved, the protection function works in about 1 second to turn off the power.

TMP PRT:000 A

温度制限を越えた原因で、プロテクションが働いたことを示します。異常状態のままパワーオンすると、約1秒後にプロテクションが掛かり、電源が切れます。

For detection of each protection function (except I-PROTECT) , refer to DIAG MENU No.10 AD DATA.

各プロクテクションの検出に関しては、後述のダイアグメニューNo. 10 AD DATAを参照してください。

History of protection function

When the protection function has worked, its history is stored in memory with a backup. Even if no abnormality is noted while servicing the unit, an abnormality which has occurred previously can be defined as long as the backup data has been stored.
The history of the protection function is cleared when DIAG is cancelled by selecting PRESET RESERVED (Memory initialized) of DIAG menu No.9 or when the backup data is erased.

プロテクションの履歴

プロテクションが働いた場合、履歴をバックアップして記憶しています。サービスのときに異常が認められなくても、バックアップが残っていれば、お客様のところで起きた異常を区別できます。
ダイアグメニューNo.9 で PRESET RESERVED（メモリーの初期化）を選んでダイアグを解除した場合、またはバックアップが消えた場合に、プロテクションの履歴はクリアされます。

• Display during menu operation

During the DIAG operation, the menu list described in the section of the startup screen appears on the monitor screen and the function at work is indicated on the FL indicator. The contents displayed during the function operation are described later in the “Details of DIAG menu” section.

● メニュー動作中の表示

ダイアグ中、モニター画面には起動画面の項で説明したメニュー一覧が表示されます。本体のFL ディスプレイには動作中の機能が表示されます。機能動作中の表示内容については、後述の機能詳細で記述します。

• Operation procedure of DIAG menu and SUB-MENU

There are 23 MENU items, each of which has some SUB-MENU items.

DIAG menu selection

Main unit: Select the menu using ▷ (Forward) and ◁ (Reverse) keys of PROGRAM.

SUB-MENU selection

Main unit: Select the sub-menu using ▷ (Forward) and ◁ (Reverse) keys of PRESET/TUNING.

● ダイアグメニューとサブメニューの操作

ダイアグにはNo.1～23のメニューがあり、そのそれぞれにサブメニューがあります。

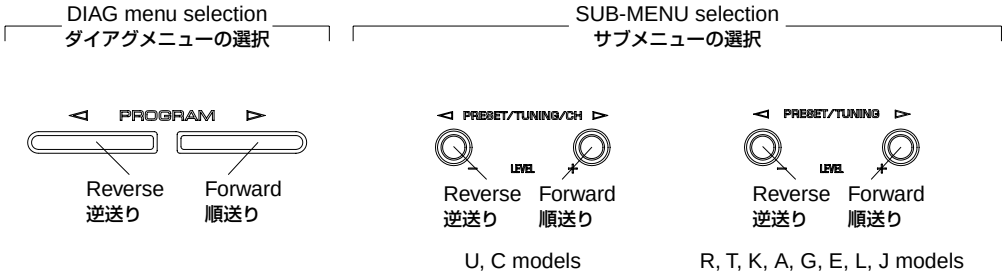
ダイアグメニューの選択

本体キーでの操作：PROGRAM ▷（順送り）、◁（逆送り）キーで選択します。

サブメニューの選択

本体キーでの操作：PRESET/TUNING ▷（順送り）、◁（逆送り）キーで選択します。

Keys of main unit / 本体キー



• Functions in DIAG mode

In addition to the DIAG menu items, functions as listed below are available.

- Input selection
- Center/Rear/Rear Center/Sub-woofer level adjustment
- Speaker relay control of A and B
- Muting
- Power on/off
- Master volume

* Functions related to the tuner and the set menu are not available.

* It is possible to confirm Menu No.16 IF STATUS while keeping the signal process (operation status) of each DIAG menu by using the INPUT MODE key of the main unit.

● ダイアグ中の機能

ダイアグメニューの他に、以下の機能が動作します。

・ インプット切り換え
・ センター、リア、リアセンター、サブウーファーレベル調整
・ スピーカーリレーA/B
・ ミューティング
・ パワーオン/オフ
・ マスターボリューム

※ チューナー関連、セットメニュー関連は機能しません。

※ 本体のINPUT MODEキーにより、各ダイアグメニューの信号処理(動作状態)を維持したままメニューNo.16 "IF STATUS"の確認ができます。

• Initial settings used to start DIAG

The following settings are used when starting DIAG. When DIAG is canceled, these settings are restored to those before starting DIAG.

- Master volume: -20 dB
- Input: DVD (MULTI CH INPUT OFF)
- Effect level: 0 dB
- Audio mute: OFF
- Speaker relay of A and B: ON
- Speaker setting: LARGE / BASS OUT = SWFR
- DIAG menu: BYPASS (1. ANALOG BYPASS)

● ダイアグ開始時の初期設定

ダイアグ開始時に以下のような設定になります。ダイアグ解除時にはダイアグ開始前の状態に戻ります。

・ マスターボリューム：-20 dB
・ インプット：DVD（MULTI CH INPUT オフ）
・ エフェクトレベル：0 dB
・ オーディオミュート：オフ
・ スピーカーリレーA/B：ON
・ スピーカー設定：LARGE / BASS OUT = SWFR
・ ダイアグメニュー：BYPASS (1. ANALOG BYPASS)

• Details of DIAG menu

1. BYPASS

Using the sub-menu, it is possible to select analog bypass output or DSP bypass output.

ANALOG BYPASS

1.ANALOG BYPAS

Reference data
INPUT: DVD ANALOG
SUBWOOFER OUTPUT: 50 Hz, Others: 1 kHz

Input level	Volume	SPEAKERS OUT				SUBWOOFER OUTPUT
		FRONT L/R	CENTER	SURROUND L/R	SURROUND BACK L/R	
Both ch, -20 dBm	+6.0 dB	+13.0 dBm	- ∞	- ∞	- ∞	- ∞

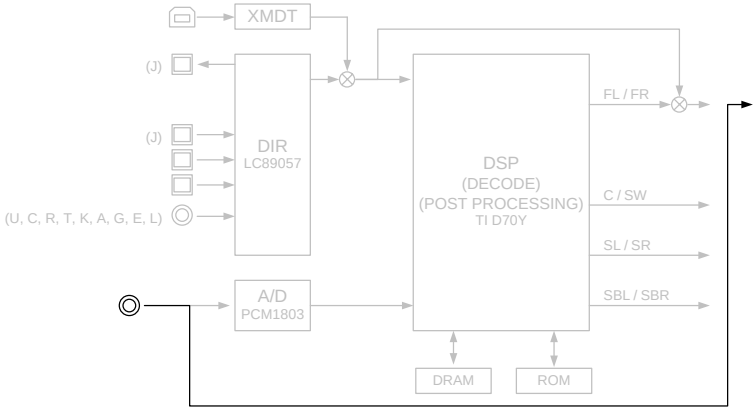
DSP BYPASS

1.DSP BYPASS

Reference data
INPUT: DVD ANALOG
SUBWOOFER OUTPUT: 50 Hz, Others: 1 kHz

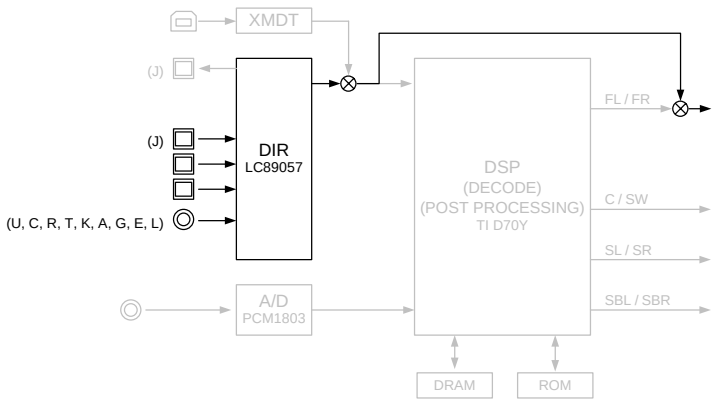
Input level	Volume	SPEAKERS OUT				SUBWOOFER OUTPUT
		FRONT L/R	CENTER	SURROUND L/R	SURROUND BACK L/R	
Both ch, -20 dBm	+6.0 dB	+13.5 dBm	- ∞	- ∞	- ∞	- ∞

ANALOG BYPASS



(Shaded items not used in this example)

DSP BYPASS



(Shaded items not used in this example)

● ダイアグメニュー詳細

1. BYPASS

サブメニューによりANALOG BYPASS/DSP BYPASSが選択可能です。

ANALOG BYPASS

1.ANALOG BYPAS

Reference data
INPUT: DVD ANALOG
SUBWOOFER OUTPUT: 50 Hz, Others: 1 kHz

Input level	Volume	SPEAKERS OUT				SUBWOOFER OUTPUT
		FRONT L/R	CENTER	SURROUND L/R	SURROUND BACK L/R	
Both ch, -20 dBm	+6.0 dB	+13.0 dBm	- ∞	- ∞	- ∞	- ∞

DSP BYPASS

1.DSP BYPASS

Reference data
INPUT: DVD ANALOG
SUBWOOFER OUTPUT: 50 Hz, Others: 1 kHz

Input level	Volume	SPEAKERS OUT				SUBWOOFER OUTPUT
		FRONT L/R	CENTER	SURROUND L/R	SURROUND BACK L/R	
Both ch, -20 dBm	+6.0 dB	+13.5 dBm	- ∞	- ∞	- ∞	- ∞

2. RAM THROUGH

Using the sub-menu, it is possible to select margin output or full-bit output.

2. RAM THROUGH

サブメニューによりMARGIN/Full Bitが選択可能です。

RAM MARGIN

Following head margin is reserved.

RAM MARGIN

以下のヘッドマージンを取ります。

FRONT	CENTER	SURROUND	SURROUND BACK	SUBWOOFER
+15.0 dB	+13.5 dB	+9.0 dB	+7.5 dB	+21.0 dB

2.RAM MARGIN

Reference data
INPUT: DVD ANALOG
SUBWOOFER OUTPUT: 50 Hz, Others: 1 kHz

Input level	Volume	SPEAKERS OUT				SUBWOOFER
		FRONT L/R	CENTER	SURROUND L/R	SURROUND BACK L/R	OUTPUT
Both ch, -20 dBm	+6.0 dB	+13.5 dBm	+13.5 dBm	+13.5 dBm	+13.5 dBm	+2.0 dBm

RAM FULL BIT

No head margin is reserved except SW.

RAM FULL BIT

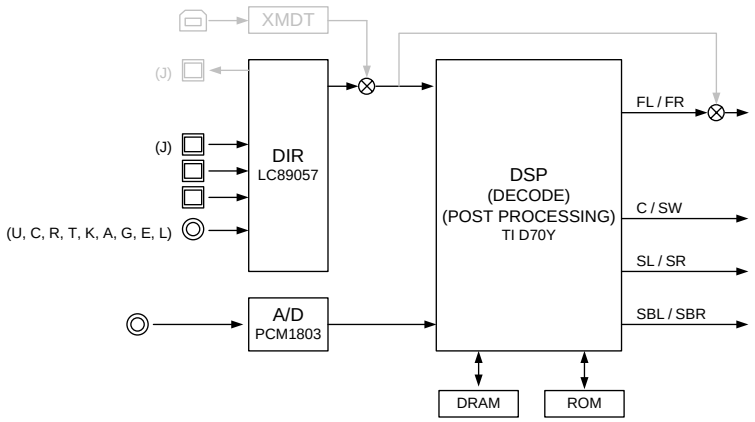
SW以外のヘッドマージンを取りません。

FRONT	CENTER	SURROUND	SURROUND BACK	SUBWOOFER
0 dB	0 dB	0 dB	0 dB	+21 dB

2.RAM FULL BIT

Reference data
INPUT: DVD ANALOG
SUBWOOFER OUTPUT: 50 Hz, Others: 1 kHz

Input level	Volume	SPEAKERS OUT				SUBWOOFER
		FRONT L/R	CENTER	SURROUND L/R	SURROUND BACK L/R	OUTPUT
Both ch, -20 dBm	+6.0 dB	+13.5 dBm	+13.5 dBm	+13.5 dBm	+13.5 dBm	+2.0 dBm



(Shaded items not used in this example)

When input source is stereo, signal is assigned as below.
2ch信号入力時、以下のように信号を振り分けて出力します。

Front L → Center / Surround L / Surround Back L, R
Front R → Surround R
Front L +10 dB → SWFR

3. PRO LOGIC

Dolby PRO LOGIC is applied to input stereo source.

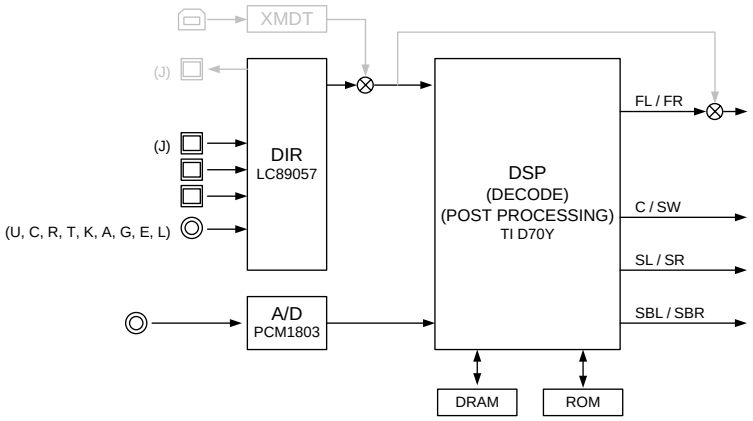
3. PRO LOGIC

入力2ch信号にDolby PRO LOGIC処理を行います。

3.PRO LOGIC

Reference data
INPUT: DVD ANALOG
SUBWOOFER OUTPUT: 50 Hz, Others: 1 kHz

Input level	Volume	SPEAKERS OUT				SUBWOOFER OUTPUT
		FRONT L/R	CENTER	SURROUND L/R	SURROUND BACK L/R	
Each ch, -20 dBm	+6.0 dB	+13.5 dBm	- ∞	- ∞	- ∞	- ∞
Both ch, -20 dBm	+6.0 dB	-20.0 dBm	+16.5 dBm	- ∞	- ∞	- ∞



(Shaded items not used in this example)

4. SPEAKERS SET

The analog switch settings for each sub-menu are as shown in the table below.

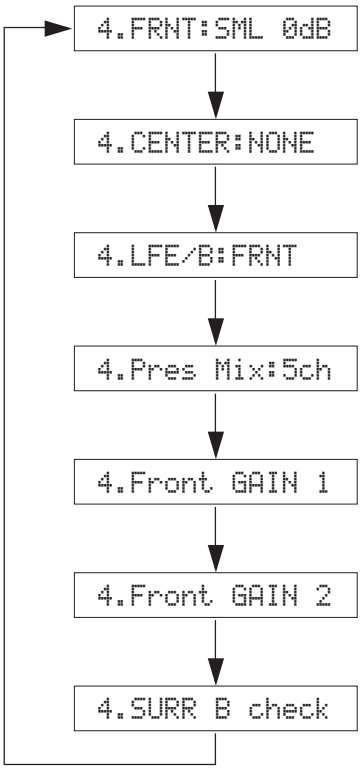
4. SPEAKERS SET

各サブメニューにおけるアナログスイッチの設定は以下の通りです。

Sub-menu		FRONT L/R	CENTER	SUR. L/R	SUR.B L/R	LFE/BASS
1	FRNT: SML 0 dB	SMALL	LARGE	LARGE	LARGE	SWFR
2	CENTER: NONE	LARGE	NONE	LARGE	LARGE	SWFR
3	LFE/B: FRNT	LARGE	SMALL	SMALL	SMALL	FRONT
4	Pre Mix: 5ch	–	–	–	–	–
5	Front GAIN 1	–	–	–	–	–
6	Front GAIN 2	–	–	–	–	–
7	SURR B Check	–	–	–	–	–

LARGE: This mode is used with a speaker with high bass reproduction performance (a large unit). Full bandwidth signals are output.
SMALL: This mode is used with a speaker with low bass reproduction performance (a small unit). The signals of 80 Hz or less are mixed into the channel specified by LFE/BASS.
NONE: This mode is used with no center speaker. The center content is reduced by 3 dB and distributed to FRONT L/R.
SWFR: LFE of 5.1ch signal or LFE/BASS lower than 90Hz is output through SUBWOOFER OUT.
FRONT: LFE of 5.1ch signal or LFE/BASS lower than 90Hz is distributed to FRONT L/R.

LARGE： 低音再生能力の高い(ユニットの大きい)スピーカーを使用するモードです。全帯域が出力されます。
SMALL： 低音再生能力の低い(ユニットの小さい)スピーカーを使用するモードです。80 Hz以下がLFE/BASSで指定したチャンネルにミックスされます。
NONE： スピーカーを使用しないモードです。センター成分は-3 dBされて、FRONT L/R に振り分けられます。
SWFR： 5.1ch信号のLFEまたは90Hz以下のLFE/BASSがSUBWOOFER OUTに出力されます。
FRONT： 5.1ch信号のLFEまたは90Hz以下のLFE/BASSをFRONT L/Rに振り分けます。



Reference data
INPUT: DVD ANALOG (Both ch)
SUBWOOFER OUTPUT: 50 Hz, Others: 1 kHz

	Sub-menu	Input level	Volume	SPEAKER OUT				SUBWOOFER
				FRONT L/R	CENTER	SURROUND L/R	SURROUND BACK L/R	OUTPUT
1	FRONT: SML 0dB	Both ch, -20 dBm	+6.0 dB	+13.5 dBm	+13.5 dBm	+13.5 dBm	+13.5 dBm	+5.5 dBm
2	CENTER: NONE	Both ch, -20 dBm	+6.0 dB	+10.5 dBm	- ∞	+13.5 dBm	+13.5 dBm	+2.0 dBm
3	LFE/B: FRNT (1 kHz)	Both ch, -20 dBm	+6.0 dB	- ∞	+13.5 dBm	+13.5 dBm	+13.5 dBm	- ∞
	LFE/B: FRNT (50 Hz)	Both ch, -20 dBm	+6.0 dB	+20.5 dBm	+13.5 dBm	+13.5 dBm	+13.5 dBm	- ∞
4	Pres Mix: 5ch	Both ch, -20 dBm	+6.0 dB	- ∞	+13.5 dBm	+18.5 dBm	- ∞	-0.5 dBm
5	Front Gain 1	Both ch, -20 dBm	+6.0 dB	+20.5 dBm	+13.5 dBm	+13.5 dBm	+13.5 dBm	+2.0 dBm
6	Front Gain 2	Both ch, -20 dBm	+6.0 dB	+20.5 dBm	+13.5 dBm	+13.5 dBm	+13.5 dBm	+2.0 dBm
7	SURR B check	Both ch, -20 dBm	+6.0 dB	- ∞	- ∞	- ∞	+13.5 dBm	- ∞

5. XCH INPUT

The signal input through the multi ch input is output.
The speaker impedance can be selected.

5. XCH INPUT

マルチCH入力された信号が出力されます。
6オーム、8オームが選択されます。

XCH INPUT_6 (ohms)

XCH INPUT_6(ohms)

```
5.XCH INPUT_6
```

Reference data
INPUT: MULTI CH INPUT
SUBWOOFER OUTPUT: 50 Hz, Others: 1 kHz

Input level	Volume	SPEAKERS OUT				SUBWOOFER OUTPUT
		FRONT L/R	CENTER	SURROUND L/R	SURROUND BACK L/R	
Both ch, -20 dBm	+6.0 dB	+13.5 dBm	+13.5 dBm	+13.5 dBm	- ∞	-10.0 dBm

XCH INPUT_8 (ohms)

XCH INPUT_8(ohms)

```
5.XCH INPUT_8
```

Reference data
INPUT: MULTI CH INPUT
SUBWOOFER OUTPUT: 50 Hz, Others: 1 kHz

Input level	Volume	SPEAKERS OUT				SUBWOOFER OUTPUT
		FRONT L/R	CENTER	SURROUND L/R	SURROUND BACK L/R	
Both ch, -20 dBm	+6.0 dB	+13.5 dBm	+13.5 dBm	+13.5 dBm	- ∞	-10.0 dBm

LIMIT SET

Not applied to these models.

LIMIT SET

このモデルには適用されません。

```
XXXXXXXXXXXX__
```

6. MIC CHECK

Not applied to these models.

6. MIC CHECK

このモデルには適用されません。

```
6.MIC CHK --dB
```

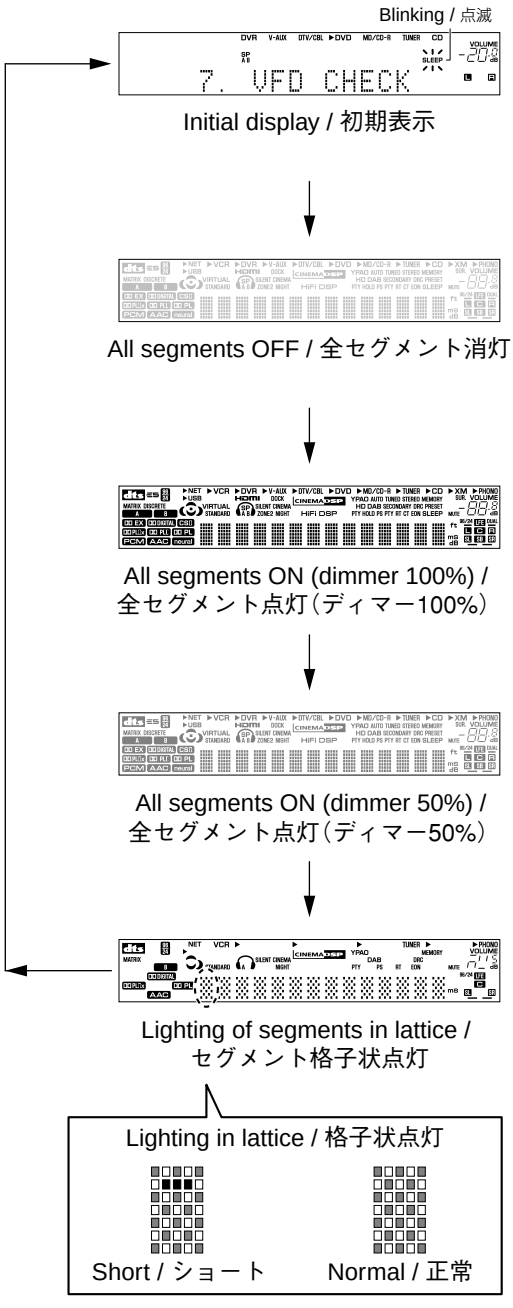
7. DISPLAY CHECK

This program is used to check the FL display section. The display condition varies as shown below according to the sub-menu operation.
The signal route is STRAIGHT.

7. DISPLAY CHECK

FL表示部のチェックプログラムです。サブメニュー操作により、表示状態が以下のように変わります。
信号処理はSTRAIGHTです。

Checking FL display section /
FL表示部のチェック



Segment conditions of the FL driver and the FL tube are checked by turning ON and OFF all segments. Next, the operation of the FL driver is checked by using the dimmer control. Then a short between segments next to each other is checked by turning ON and OFF all segments alternately (in lattice). (In the above example, the segments in the second row from the top are shorted.)

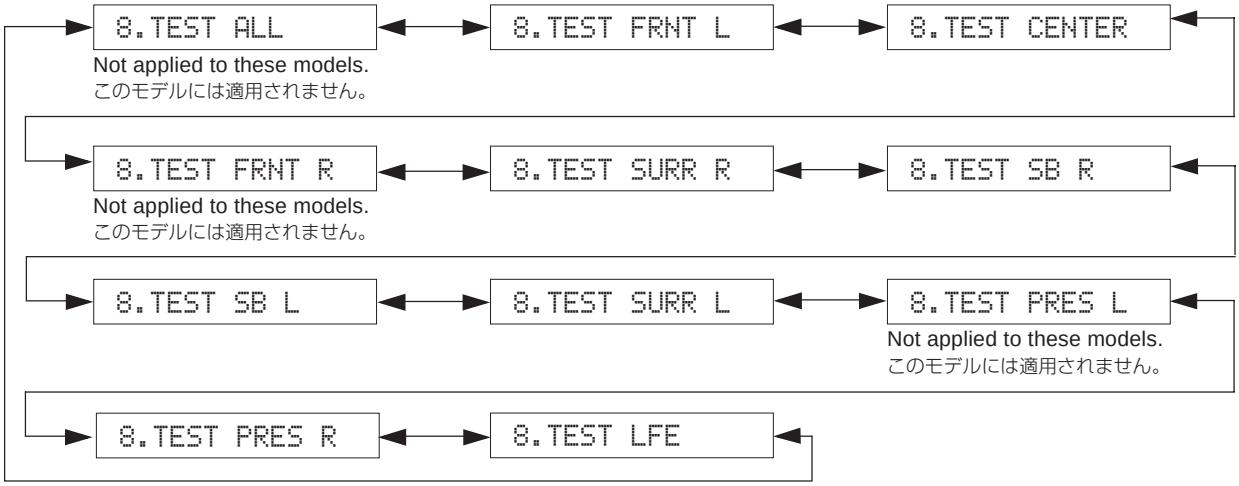
全セグメント消灯・全セグメント点灯によりFLドライバー、FL管のセグメントの不良を確認します。
次に、ディマーコントロールによってFLドライバーの動作チェックを行います。
さらに全セグメントを交互（格子状）に点灯/消灯することで、隣り合うセグメントのショートをチェックします。
（上図の例では、上から2行目のセグメントがショートしています。）

8. MANUAL TEST

The test noise based THX is output to the channel specified by the sub-menu from the DSP.
The noise frequency for LFE is 35 to 250 Hz. Other than that, the center frequency is 800 Hz.

8. MANUAL TEST

DSPからサブメニューで指定したチャンネルへTHX準拠のテストノイズを出力します。
LFE用のノイズ周波数は35～250 Hz、それ以外は中心周波数800 Hzとなります。

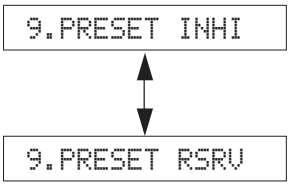


9. FACTORY PRESET

This menu is used to reserve/inhibit initialization of the backup RAM (Parameters and set menu contents, etc. of the sound field program).

9. FACTORY PRESET

バックアップ用RAM（音場プログラムのパラメーターやセットメニュー内容など）の初期化を予約/禁止します。



PRESET INHIBIT (Initialization inhibited) / **PRESET INHIBIT**（初期化禁止）
RAM initialization is not executed. Select this sub-menu to protect the values set by the user.
Note: The protection history will not be erased using PRESET INHIBIT.
RAMの初期化は行われません。ユーザーの設定値を保護するときは、こちらを選択してください。

PRESET RESERVED (Initialization reserved) / **PRESET RESERVED**（初期化予約）
Initialization of the back-up RAM is reserved. (Actually, initialization is executed the next time that the power is turned on.) Select this sub-menu to reset to the original factory settings or to reset the RAM. Use PRESET RESERVED to erase the protection history.
バックアップRAMの初期化が予約されます。（実際に初期化されるのは、次回の電源投入時です。）工場出荷時やRAMをリセットしたいときは、こちらを選択してください。

CAUTION: Before setting to the PRESET RESERVED, write down the existing preset memory. Content of the Tuner in a table as shown below. (This is because setting to the PRESET RESERVED will cause ALL user memory contents to be erased.)

注意： PRESET RESERVEDを選んで初期化をする前に、チューナーのユーザーメモリー内容を下表に書き写してください。（初期化をすると、ユーザーメモリーの内容は消えてしまいます。）

Preset group	P1	P2	P3	P4	P5	P6	P7	P8
A								
B								
C								
D								
E								

• **PRESET STATIONS / プリセット局**

STATION		FM FACTORY PRESET DATA (MHz)		
PAGE	NO.	U, C	R, T, K, A, G, E, L	J
A/C/E	1	87.5	87.50	76.0
	2	90.1	90.10	83.0
	3	95.1	95.10	84.0
	4	98.1	98.10	86.0
	5	107.9	108.00	90.0
	6	88.1	88.10	78.0
	7	106.1	106.10	88.0
	8	107.9	108.00	82.1

STATION		AM FACTORY PRESET DATA (kHz)		
PAGE	NO.	U, C, R, T, K	A, G, E, L	J
B/D	1	630	630	630
	2	1080	1080	1080
	3	1440	1440	1440
	4	530	531	531
	5	1710	1611	1611
	6	900	900	900
	7	1350	1350	1350
	8	1400	1404	1404

10. AD DATA CHECK

This menu is used to display the A/D conversion value of the Microprocessor which detects panel keys of the main unit and protection functions in using the sub-menu. During audio signal processing, the condition before execution is maintained.
When K0/K1 menu is selected, keys become non-operable due to detection of the values of all keys. However, it is possible to advance to the next sub-menu by turning the VOLUME of the main unit. When using this function, note that turning the VOLUME more than 1 click would cause the volume value to change.

* The figures in the diagram are given as reference only.

PS1/PS2 (Power supply voltage protection detection)
Power supply voltage protection value (Normal value: PS1: 17 to 66, PS2: 25 to 46)
PS1: Detects +5S and +5.3X (U, C models).
PS2: Detects ±12V, ±5V, +5D, +3.3D and +5i.
* If PS is out of the normal value range, the protection function works to turn off the power.
(Reference voltage: 5 V=100 %)

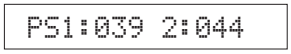
DC/TH (protection detection/temperature detection)
DC: DC detect protection value (Normal value: 5 to 36)
* If DC is out of the normal value range, the protection function works to turn off the power.
(Reference voltage: 5 V=100 %)
TH: Detects the temperatur of the heat sink.
Temperature detected value
(Normal value: 9 to 177) U, C, T, K, A, G, E, J models
(Normal value: 9 to 167) R, L models
(Reference voltage: 5 V=255)

10. AD DATA CHECK

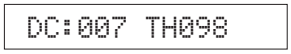
本機パネルキー、プロテクションなどを検出しているMicroprocessorのA/D変換の値を、サブメニューで表示します。オーディオ信号処理は実行前の状態を維持します。
K0/K1のメニューにすると、全キーの値を検出するためキー操作はできなくなりますが、本機のVOLUMEを回すことにより、次のサブメニューに進めることができます。このとき1クリック以上回すと、ボリューム値が変化するので注意してください。

※ 図中の数値は参考例です。

PS1/PS2（電源電圧プロテクションの検出）
プロテクションの値(正常値 PS1: 17～66、PS2: 25～46)
PS1：+5Sを検出しています。
PS2：±12V、±5V、+5D、+3.3D、+5iを検出しています。
※ PSは正常値を外れるとプロテクションが働き、電源オフされます。
(基準電圧：5V=100%)



DC/TH（プロテクションの検出/温度検出）
DC： DC検出プロテクションの値(正常値5～36)
※ DCは正常値を外れるとプロテクションが働き、電源オフされます。
(基準電圧：5V=100%)
TH： ヒートシンクの温度を検出しています。
温度検出値
(正常値: 9～177)
(基準電圧：5V=255)



IMP SW/POWER LIMIT (impedance/power limiter detection)
IMP: Not applied to these models.
PL: Power limiter detection value
The voltage value of pin No. 92 of IC451 is displayed, using 5V/256 as standard.
The port (No. 3) output is controlled by using the input voltage value of pin No. 92 of IC451.

IMP SW/POWER LIMIT（インピーダンス/パワーリミッターの検出）
IMP：このモデルには適用されません。
PL： パワーリミッター検出の値
IC451　92ピンの入力電圧値を5V/256を基準にして表示します。IC451　92ピンの入力電圧値により、ポート（3ピン）を制御します。

```
IMP:8 PL:245
```

PANEL KEY (K0/K1)
(Panel key of main unit) [Remote control code: –]
A/D of the key fails to function properly when the standard value is deviated by ±8. In this case, check the constant of partial pressure resistor, solder condition, etc. Refer to table.
(Reference voltage: 5 V=100 %)

PANEL KEY (K0/K1)
（本機パネルキー）
キーのA/Dは基準値から±8を外れると、正常な動きをしません。下表をご覧になり、各キーの分圧抵抗の定数、ハンダ不良等の確認をしてください。
（基準電圧：5V=100%）

```
K0:100 K1:100
```

Display (%)	K0	K1
0 - 6	◁ PROGRAM	—
7 - 13	PROGRAM ▷	—
14 - 21	BASS/TREBLE -	—
22 - 31	BASS/TREBLE +	—
32 - 41	INPUT MODE	MULTI CH INPUT
42 - 53	STRAIGHT	FM/AM
54 - 63	TONE CONTROL	A/B/C/D/E
64 - 72	PRESET/TUNING	◁ PRESET
73 - 80	SPEAKERS B	PRESET ▷
81 - 88	SPEAKERS A	MEMORY
89 - 95	—	TUNING MODE
96 - 100	KEY OFF	KEY OFF

11. VIDEO
Not applied to these models.

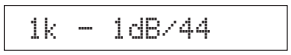
11. VIDEO
このモデルには適用されません。

12. XM STATUS (U, C models)
Perform the output check of XM Radio Antenna connected to the XM terminal.

1k -1dB/44.1k
The test tone (1kHz, -1dB/44.1kHz) is output.

12. XM STATUS(U、C models)
XM端子に接続された、XM Radio Antennaの出力チェックを行います。

1k -1dB/44.1k
テストトーン(1kHz、-1dB/44.1kHz)を出力します。



1k -61dB/44.1k
The test tone (1kHz, -61dB/44.1kHz) is output.

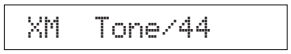
1k -61dB/44.1k
テストトーン(1kHz、-61dB/44.1kHz)を出力します。

Mute /44.1k
Nothing is output.

Mute /44.1k
何も出力されません。

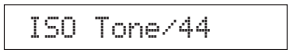
XM Tone/44.1k
The XM tone (44.1kHz) is output.

XM Tone/44.1k
XMトーン(44.1kHz)を出力します。



ISO Tone/44.1k
The ISO tone (44.1kHz) is output.

ISO Tone/44.1k
ISOトーン(44.1kHz)を出力します。



1k -1dB/32k
The test tone (1kHz, -1dB/32kHz) is output.

1k -1dB/32k
テストトーン(1kHz、-1dB/32kHz)を出力します。

1k -61dB/32k
The test tone (1kHz, -61dB/32kHz) is output.

1k -61dB/32k
テストトーン(1kHz、-61dB/32kHz)を出力します。

Mute /32k
Nothing is output.

Mute /32k
何も出力されません。

XM Tone/32k
The XM tone (32kHz) is output.

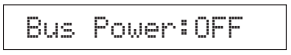
XM Tone/32k
XMトーン(32kHz)を出力します。

ISO Tone/32k
The ISO tone (32kHz) is output.

ISO Tone/32k
ISOトーン(32kHz)を出力します。

XM/DT Bus Power: OFF
The power of XM module is turned off.

XM/DT Bus Power: OFF
XMモジュールの電源をOFFします。



13. iPod
Not applied to these models.

13. iPod
このモデルには適用されません。

16. IF STATUS (Input function status)

Using the sub-menu, the status data is displayed one after another in the hexadecimal notation.
During signal processing, the status before execution of this menu is maintained.

* Numeric values in the figure example are for reference.

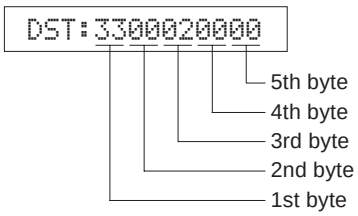
16. IF STATUS

サブメニュー操作により、以下のステータス情報を順次16進数で表示します。信号処理は、本メニュー実行前の状態を維持します。

※図中の数値は参考例です。

DST: DSP status

DST：DSPステータス



<1st byte>　Digital input/output setting value
Upper 4 bits: REC OUT selected /
lower 4 bits: INPUT selected

＜第1バイト＞デジタル入出力設定値
上位4 bit REC OUT選択 /
下位4 bit INPUT選択

Value	Choice	Preset name	
0	NONE	–	
1	OPT FRONT	–	
2	OPT 1	MD/CD-R	DSP-AX459 model
3	OPT 2	DVD	
4	OPT 3	DTV/CBL	
8	COAX 1	CD	RX-V459/HTR-5940/HTR-5935 models
9	COAX 2	–	

<2nd byte> / ＜第2バイト＞
Fs information of reproduction signal /
再生信号のFs情報

Display	Fs (kHz)
00	Analog
01	32 kHz
02	44.1 kHz
03	48 kHz
04	64 kHz
05	88.2 kHz
06	96 kHz
07	128 kHz
08	176.4 kHz
09	192 kHz
0A	Unknown NRM
0B	Unknown DBL
0C	Unknown QUAD
0D	Unknown
0E	Undefined

<3rd byte> / ＜第3バイト＞
Audio code mode information of reproduction signal /
再生信号のオーディオコードモード情報

Display	Audio code
00	1+1
01	1/0
02	2/0
03	3/0
04	2/1
05	3/1
06	2/2
07	3/2
08	2/3
09	3/3
0A	3/4
0B	over 6.1
0C	Milti-Mono
0D	Milti-PCE
0E	Unknown
0F	Undefined

<4th byte> / ＜第4バイト＞
Format information of reproduction signal /
再生信号のフォーマット情報

Display	Signal format
00	Analog
01	Err
10	PCM Audio
20	Digital Data
21	IEC1937
22	None PCM
23	Unknown
50	dts
51	dts-CD
52	dts 96/24
54	dts-ES (Matrix)
58	dts-ES (Discrete)
5C	dts-ES (Both)
60	AAC
C0	Dolby Digital
C1	Dolby Digital Karaoke
C4	Dolby Digital EX
FF	Undefined

<5th byte> / <第5バイト>
Signal processing status information /
信号処理ステータス情報

bit	Fs (kHz)
bit 7	Digital mute
bit 6	–
bit 5	6.1 (7.1) processing
bit 4	Analog mute
bit 3	–
bit 2	PCM through
bit 1	–
bit 0	dts analog mute

DMD: Decoder mode information
Not applied to these models.

DMD：デコーダー情報
このモデルには適用されません。

DMD:03C00000

DIF: DIR information
Not applied to these models.

DIF：DIR情報
このモデルには適用されません。

DIF:0001000600

PC: Preamble C information
Not applied to these models.

PC：Preamble C情報
このモデルには適用されません。

PC :0000

CS1, 2: Channel status information
Not applied to these models.

CS1、2：チャンネルステータス情報
このモデルには適用されません。

CS1:00000000000 ——— CS2:00

DEI: Decoder information
Not applied to these models.

DEI：デコーダー情報
このモデルには適用されません。

DEI:08080000600

BS1-8: Bit stream information
Not applied to these models.

BS1-8：ビットストリーム情報
このモデルには適用されません。

BS1:00000000000 ——— BS8:00

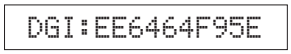
MTT: Mute Trigger
Not applied to these models.

MTT：Mute Trigger
このモデルには適用されません。

MTT:0018001820

DGI: Digital information
Not applied to these models.

DGI：DIGITAL系情報
このモデルには適用されません。

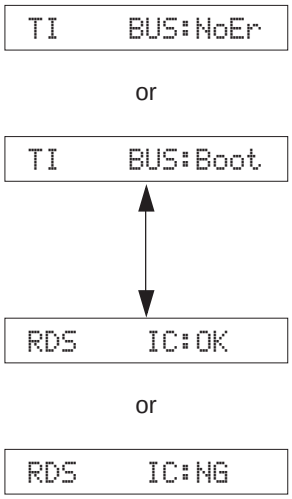


17. DSP BUS CHECK

This menu is used to self-diagnose whether or not the bus connection for the TI (DA70Y) and the external ROM/RAM is made properly.
When no error is detected, "NoEr" appears on display.

17. DSP BUS CHECK

TI(DA70Y)と外付けROM/RAMとのバス接続の正否を自己診断します。
エラーが検出されなかった場合は、“NoEr”と表示されます。



No error detected.
不良検出なし

When this indication is displayed with in seconds or displayed alternately “NoEr” and “Boot”, it is highly possible that there are errors.
数秒間この状態、またはNoErと交互に表示される場合、異常が発生している可能性があります。

No applied to these models.
このモデルは適用されません。

18. SWFR CUT OFF (HTR-5935 model)

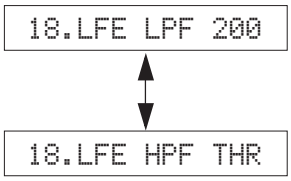
The cut off frequency setting of LFE.

Low-pass filter setting.
It can be selected 40 Hz to 200 Hz every 10 Hz by the STRAIGHT key.

High-pass filter setting.
It can be selected 40 Hz to 200 Hz every 10 Hz and through by the STRAIGHT key.

18. SWFR CUT OFF(HTR-5935 model)

LFE出力のカットオフ周波数を設定できます。



ローパスフィルタの設定です。
STRAIGHTキーにより、40 Hz～200 Hzまで10 Hz単位で変更できます。

ハイパスフィルタの設定です。
STRAIGHTキーにより、40 Hz～200 Hzまで10 Hz単位とスルーに変更できます。

19. PROTECTION SETTING

Not applied to these models.

19. PROTECTION SETTING

このモデルには適用されません。

20. PROTECTION HISTORY

Four protection histories are display.

20. PROTECTION HISTORY

過去のプロテクション履歴を4つまで表示します。

21. SOFT SW

Note) Changing the function setting may hinder the proper operation.

This menu is used to switch the function settings on P.C.B. through the software so as to activate the product.
The protection function follows the P.C.B. settings. When connected to AC or in the maker preset state, the unit is initialized to the P.C. B. setting. Display of each function after initialization varies depending on settings on P.C.B. The operation mode can be changed by selecting the sub-menu and then using the STRAIGHT key.

SW MODE: PCB, MODEL or FNC can be selected.

```
21.SW    :PCB
```

MODEL SETTING: 759SE, V659, H5960, V559, H5950, V459 or H5935 can be selected. (SW MODE: Selectable when MODEL has been selected.)

```
21.MODEL:V459
```

DESTINATION: J, U, C, R, T, K, A, B, G (E) or L can be selected. (SW MODE: Selectable when MODEL has been selected.)

```
21.DEST  :G
```

TUNER DESTINATION: J, UC, ABG or RL can be selected. (SW MODE: Selectable when FNC has been selected.)

```
21.TuDst:ABG
```

TUNER TYPE: NRM, RDS or XM can be selected. (SW MODE: Selectable when FNC has been selected.)

```
21.TuDyp:RDS
```

VIDEO FORMAT: NTSC or PAL can be selected. (SW MODE: Selectable when FNC has been selected.)

```
21.VIDEO:PAL
```

21. SOFT SW

注) 機能設定を変更した場合、正常に動作しないことがあります。

P.C.B.上の機能設定をソフト的に切り替えて、製品を動作させる機能です。
プロテクション機能は、P.C.B.の設定にしたがいます。AC接続またはメーカープリセットで、P.C.B.の設定に初期化されます。初期化後の各機能の表示は、P.C.B.上の設定によります。操作は、サブメニューを選んだ後、STRAIGHTキーで切り替えます。

SW MODE：PCB、MODELまたはFNCを選択できます。

```
21.SW    :PCB
```

MODEL SETTING：759SE、V659、H5960、V559、H5950、V459、H5935のいずれかを選択できます。（SW MODE：MODEL時選択できます。）

```
21.MODEL:V459
```

DESTINATION：J、U、C、R、T、K、A、B、G(E)、Lのいずれかを選択できます。（SW MODE：MODEL時選択できます。）

```
21.DEST  :G
```

TUNER DESTINATION：J、UC、ABG、RLのいずれかを選択できます。（SW MODE：FNC時選択できます。）

```
21.TuDst:ABG
```

TUNER TYPE：NRM、RDS、XMのいずれかを選択できます。（SW MODE：FNC時選択できます。）

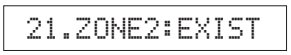
```
21.TuDyp:RDS
```

VIDEO FORMAT：NTSCまたはPALを選択できます。（SW MODE：FNC時選択できます。）

```
21.VIDEO:PAL
```

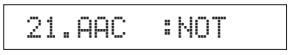
ZONE2: NOT or EXIST can be selected. (SW MODE: Selectable when FNC has been selected.)

ZONE2：NOTまたはEXISTを選択できます。(SW MODE：FNC時選択できます。)



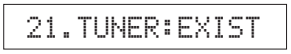
AAC: NOT or EXIST can be selected. (SW MODE: Selectable when FNC has been selected.)

AAC：NOTまたはEXISTを選択できます。(SW MODE：FNC時選択できます。)



TUNER: NOT or EXIST can be selected. (SW MODE: Selectable when FNC has been selected.)

TUNER：NOTまたはEXISTを選択できます。(SW MODE：FNC時選択できます。)



ZONE2 AMP: NOT or EXIST can be selected. (SW MODE: Selectable when FNC has been selected.)

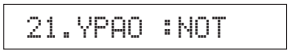
ZONE2 AMP：NOTまたはEXISTを選択できます。(SW MODE：FNC時選択できます。)

OSD: NOT or EXIST can be selected. (SW MODE: Selectable when FNC has been selected.)

OSD：NOTまたはEXISTを選択できます。(SW MODE：FNC時選択できます。)

YPAO: NOT or EXIST can be selected. (SW MODE: Selectable when FNC has been selected.)

YPAO：NOTまたはEXISTを選択できます。(SW MODE：FNC時選択できます。)



22. SOFTWARE VERSION

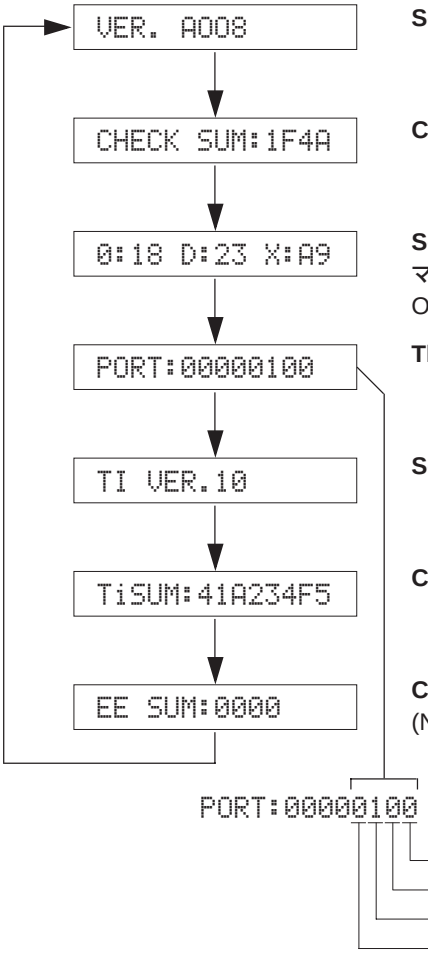
The version, checksum and the port specified by the microprocessor are displayed. The signal is processed using EFFECT OFF. The checksum is obtained by adding the data at every 16 bits for each program area and expressing the result as a 4-figure hexadecimal data.

* Numeric values in the figure example are for reference.

22. SOFTWARE VERSION

ソフトウェアのバージョン、チェックサム、マイコンの指定ポートを表示します。
信号はエフェクトOFFです。チェックサムは、プログラムエリア別にデータを16ビットごとに加算していき、4桁の16進データで現したものです。

※図中の数値は参考例です。



Software version of microprocessor / マイコンのソフトウェアバージョン

Checksum value of microprocessor / マイコンのチェックサム

Software modules version of microprocessor /
マイコンのモジュール別ソフトウェアバージョン
O: Operation D: DSP X: XM

The condition of ports for model detection / モデル判別ポートの状態

Software version of TI (DSP) / TI(DSP)のソフトウェアバージョン

Checksum value of TI (DSP) / TI(DSP)のチェックサム

Checksum value of EEPROM / EEPROMのチェックサム
(Not applied to these models. / このモデルには適用されません。)

Type3	Type2	Type1	Type0	Model
–	1	1	1	RX-V459 DSP-AX459 HTR-5940
–	1	1	0	HTR-5935

23. TI (DSP) BOOT

The rewriting mode of TI (DSP) software.
(Not applied to these models.)

23. TI(DSP)BOOT

TI(DSP)のソフトウェア書き換えモードです。
(このモデルには適用されません。)

■ AMP ADJUSTMENT / アンプ部調整

Confirmation of Idling Current of MAIN (1) P. C. B.

- Right after power is turned on, confirm that each measured voltage across the terminals of R1149 (FRONT Lch), R1150 (FRONT Rch), R1153 (CENTER), R1154 (SURROUND Lch), R1152 (SURROUND Rch), R1151 (SURROUND BACK) is between 0.1 mV and 10.0 mV.
- If it exceeds 10.0 mV, open (cutoff) R1104 (FRONT Lch), R1106 (FRONT Rch), R1112 (CENTER), R1114 (SURROUND Lch), R1110 (SURROUND Rch), R1108 (SURROUND BACK) and reconfirm the voltage.

  Attention
  If the measured voltage exceeds 10.0 mV. after an amplifier repair, first check for a defective component before cutting the bias resistor.
- Confirm that the voltage is 0.2 mV-15.0 mV. after 60 minutes.

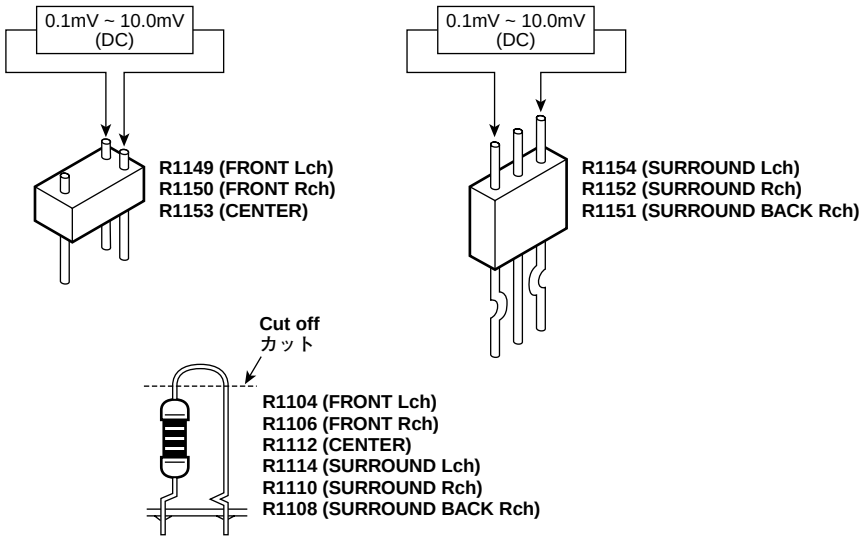
メイン(1)基板のアイドリング電流の確認

● 電源投入直後、R1149(FRONT Lch)、R1150(FRONT Rch)、R1153(CENTER)、R1154(SURROUND Lch)、R1152(SURROUND Rch)、R1151(SURROUND BACK)の端子間電圧を測定し、0.1 mVから10.0 mV.の間であることを確認してください。

● 電圧が10 mVを超えている場合は、R1104(FRONT Lch)、R1106(FRONT Rch)、R1112(CENTER)、R1114(SURROUND Lch)、R1110(SURROUND Rch)、R1108(SURROUND BACK)をカットし、電圧を再確認してください。

注意
パワーアンプ修理後に10.0 mV.を超えている場合は、抵抗をカットする前に故障箇所を調べてください。

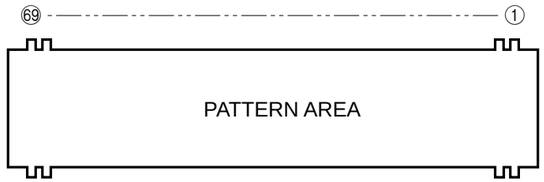
● 60分後、電圧が0.2 mV～15.0 mV.であることを確認してください。



RX-V459/HTR-5940/DSP-AX459

■ DISPLAY DATA

● V3000 : HNA-17MM03T (WG474000)



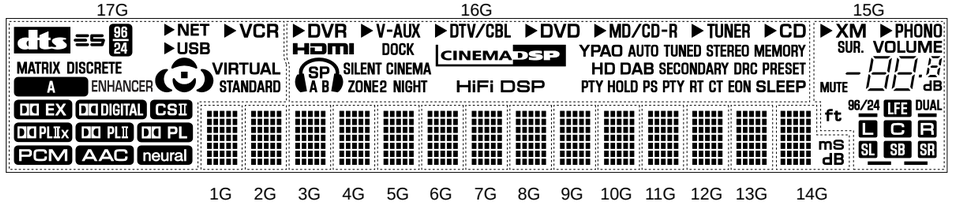
● PIN CONNECTION

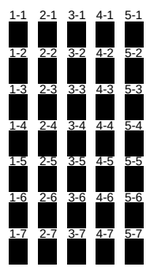
Pin No.	69	68	67	66	65	64	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35
Connection	F2	F2	NP	NP	P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	P12	P13	P14	P15	P16	P17	P18	P19	P20	P21	P22	P23	P24	P25	P26	P27	P28	P29	P30	P31

Pin No.	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
Connection	P32	P33	P34	P35	P36	P37	NX	NX	NX	NX	NX	NX	NX	17G	16G	15G	14G	13G	12G	11G	10G	9G	8G	7G	6G	5G	4G	3G	2G	1G	NP	NP	F1	F1

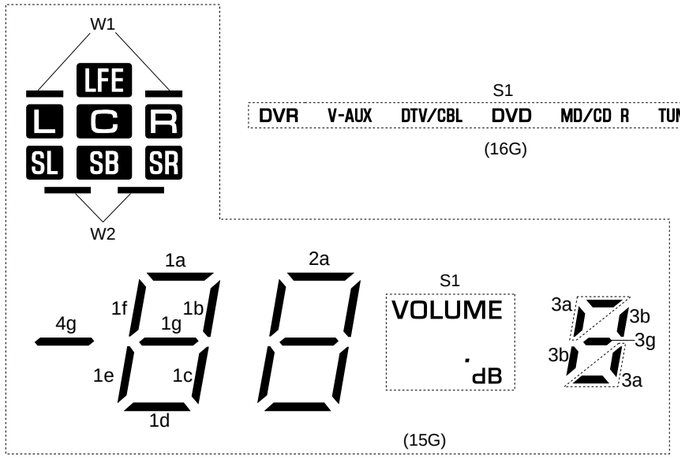
Note : 1) Fn ..... Filament pin 2) nG ..... Grid pin 3) Pn ..... Anode pin 4) NP ..... No pin 5) NX ..... No extended pin

● GRID ASSIGNMENT





(1G~14G)



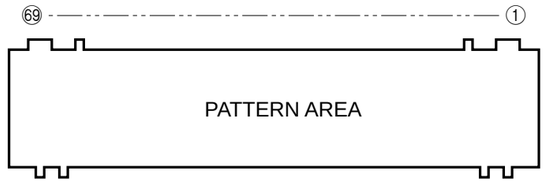
● ANODE CONNECTION

	17G	16G	15G	14G	13G~1G
P1	dts	S1	S1	1-1	1-1
P2	ES	DVR	W1	2-1	2-1
P3	MATRIX	V-AUX	W2	3-1	3-1
P4	DISCRETE	DTV/CBL	4g	4-1	4-1
P5	96/24	DVD	1a	5-1	5-1
P6	A	MD/CD-R	1b	1-2	1-2
P7	ENHANCER	TUNER	1c	2-2	2-2
P8	DD EX	CD	1d	3-2	3-2
P9	DD DIGITAL	HDMI	1e	4-2	4-2
P10	CSII	(headphone)	1f	5-2	5-2
P11	DD PLIIx	SP	1g	1-3	1-3
P12	DD PLII	A	2a	2-3	2-3
P13	DD PL	B	2b	3-3	3-3
P14	PCM	SILENT CINEMA	2c	4-3	4-3
P15	AAC	ZONE2	2d	5-3	5-3
P16	neural	NIGHT	2e	1-4	1-4
P17	NET	DOCK	2f	2-4	2-4
P18	USB	CINEMA DSP	2g	3-4	3-4
P19	VCR	HiFi DSP	3g	4-4	4-4
P20	NET	YPAO	3b	5-4	5-4
P21	USB	AUTO	3a	1-5	1-5
P22	VCR	TUNED	XM	2-5	2-5
P23	R1	STEREO	PHONO	3-5	3-5
P24	R2	MEMORY	XM	4-5	4-5
P25	R3	HD	PHONO	5-5	5-5
P26	R4	DAB	SUR.	1-6	1-6
P27	R5	SECONDARY	MUTE	2-6	2-6
P28	VIRTUAL	DRC	DUAL	3-6	3-6
P29	STANDARD	PRESET	96/24	4-6	4-6
P30	–	PTY HOLD	ft	5-6	5-6
P31	–	HOLD	LFE	1-7	1-7
P32	–	PS	L	2-7	2-7
P33	–	PTY	C	3-7	3-7
P34	–	RT	R	4-7	4-7
P35	–	CT	SL	5-7	5-7
P36	–	EON	SB	mS	–
P37	–	SLEEP	SR	dB	–

HTR-5935

■ DISPLAY DATA

● V3000 : 17-BT-26GNK (WG473900)



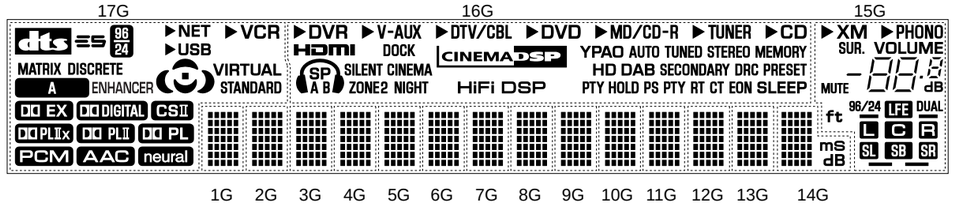
● PIN CONNECTION

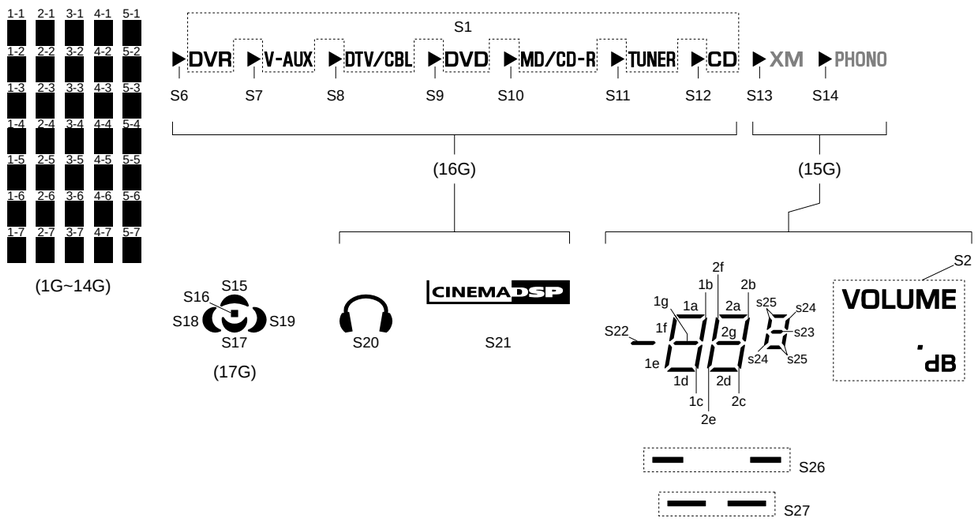
Pin No.	69	68	67	66	65	64	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35
Connection	F2	NX	NP	NP	P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	P12	P13	P14	P15	P16	P17	P18	P19	P20	P21	P22	P23	P24	P25	P26	P27	P28	P29	P30	P31

Pin No.	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
Connection	P32	P33	P34	P35	P36	P37	NX	NX	NX	NX	NX	NX	NX	17G	16G	15G	14G	13G	12G	11G	10G	9G	8G	7G	6G	5G	4G	3G	2G	1G	NP	NP	NX	F1

Note : 1) F1, F2 ..... Filament pin 2) NP ..... No pin 3) NX ..... No extend pin 4) 1G~17G ..... Grid pin

● GRID ASSIGNMENT



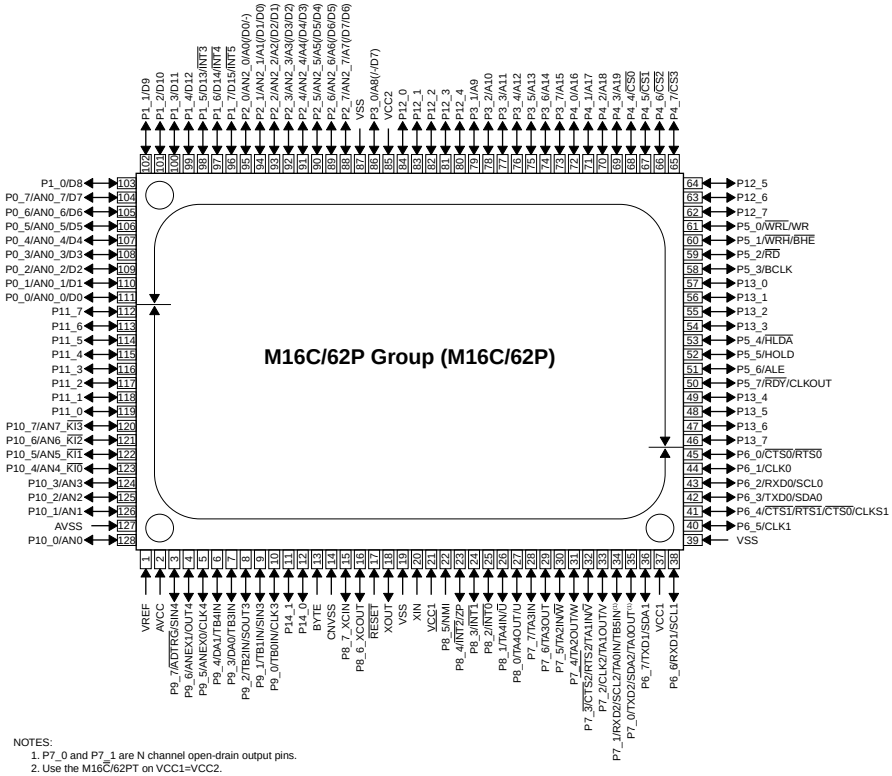


● ANODE CONNECTION

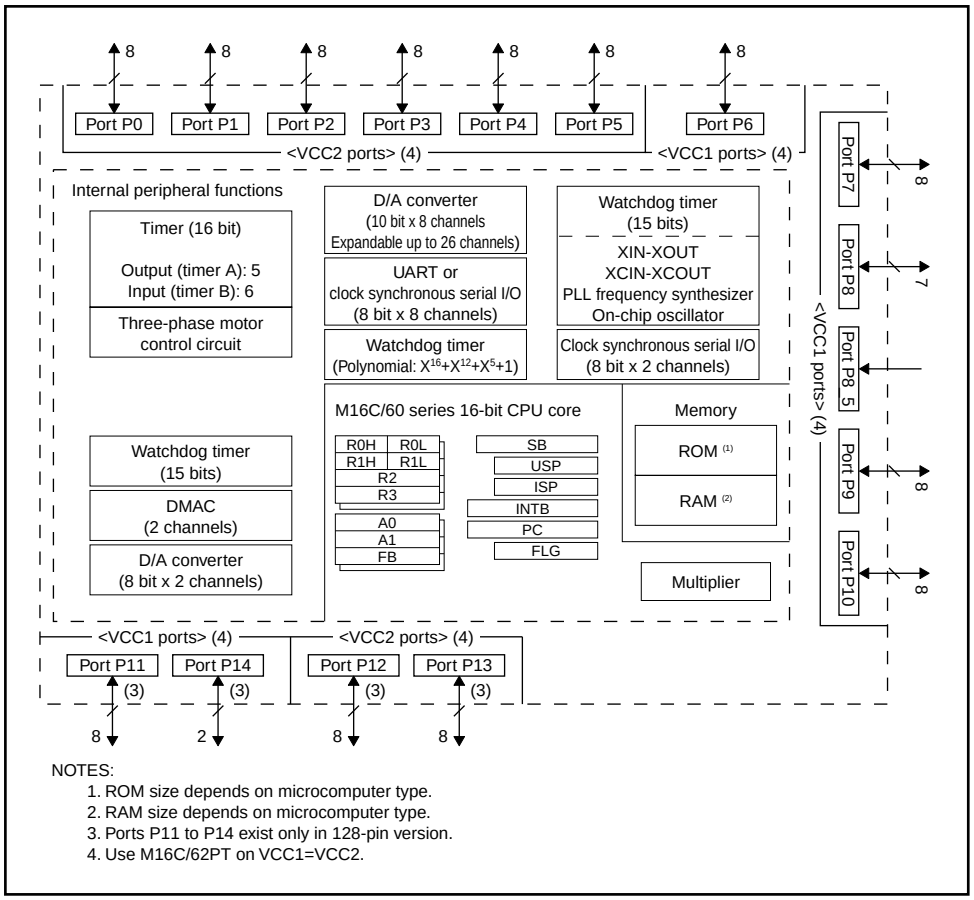
	1G~13G	14G	15G	16G	17G
1P	1-1	1-1	S2	S1	dts
2P	2-1	2-1	S26	S6	ES
3P	3-1	3-1	S27	S7	MATRIX
4P	4-1	4-1	S22	S8	DISCRETE
5P	5-1	5-1	1a	S9	96/24
6P	1-2	1-2	1b	S10	A
7P	2-2	2-2	1c	S11	ENHANCER
8P	3-2	3-2	1d	S12	DD EX
9P	4-2	4-2	1e	HDMI	DD DIGITAL
10P	5-2	5-2	1f	S20	CSII
11P	1-3	1-3	1g	SP	DD PLIIx
12P	2-3	2-3	2a	A	DD PLII
13P	3-3	3-3	2b	B	DD PL
14P	4-3	4-3	2c	SILENT CINEMA	PCM
15P	5-3	5-3	2d	ZONE2	AAC
16P	1-4	1-4	2e	NIGHT	neural
17P	2-4	2-4	2f	DOCK	NET
18P	3-4	3-4	2g	S21	USB
19P	4-4	4-4	S23	HiFi DSP	VCR
20P	5-4	5-4	S24	YPAO	S3
21P	1-5	1-5	S25	AUTO	S5
22P	2-5	2-5	XM	TUNED	S4
23P	3-5	3-5	PHONO	STEREO	S15
24P	4-5	4-5	S13	MEMORY	S16
25P	5-5	5-5	S14	HD	S17
26P	1-6	1-6	SUR.	DAB	S18
27P	2-6	2-6	MUTE	SECONDARY	S19
28P	3-6	3-6	DUAL	DRC	VIRTUAL
29P	4-6	4-6	96/24	PRESET	STANDARD
30P	5-6	5-6	ft	PTY HOLD	–
31P	1-7	1-7	LFE	HOLD	–
32P	2-7	2-7	L	PS	–
33P	3-7	3-7	C	PTY	–
34P	4-7	4-7	R	RT	–
35P	5-7	5-7	SL	CT	–
36P	–	mS	SB	EON	–
37P	–	dB	SR	SLEEP	–

■ IC DATA

IC2 : M30625MHP-A98GP (DSP P.C.B.)
Microprocessor



NOTES:
1. P7_0 and P7_1 are N channel open-drain output pins.
2. Use the M16C/62PT on VCC1=VCC2.



NOTES:
1. ROM size depends on microcomputer type.
2. RAM size depends on microcomputer type.
3. Ports P11 to P14 exist only in 128-pin version.
4. Use M16C/62PT on VCC1=VCC2.

IC2 : M30625MHP-A98GP (DSP P.C.B.)
Microprocessor

No.	Port Name	Terminal Name	I/O				Function
			PowerOn	Pure Direct	Standby	Sleep	
1	Vref	Vref	MCU		MCU	MCU	AD reference
2	Avcc	Avcc	MCU		MCU	MCU	AD power supply
3	P97/Adtrg/Sin4	CEFD	O		O	O	FL Driver CE
		MOD0			I		MODEL distinction 0
4	P96/ANEX1/SOUT4	DTFD	SO		O	O	FL Driver TxD
5	P95/ANEX0/CLK4	CKFD	SO		O	O	FL Driver CLOCK
6	P94/DA1/TB4in	LC	DA		O	O	Limiter control output
7	P93/DA0/TB3in	XMPWR	O		O	O	XM/DT BUS POWER CONTROL (U model)
8	P92/TB2in/SOUT3	SDM	SO		O	O	Serial data output to DIR, TI (DA70Y), DAC / DIR: 4M, LSBF/TI: 1M, MSBF
9	P91/TB1in/SIN3	SDD	SI		O	O	Serial data input from DIR, TI (DA70Y)
10	P90/TB0in/CLK3	SCK	SO		O	O	Serial clock output to DIR, TI (DA70Y) DAC
11	P141	/ICCNV	O	O	O	O	Reset I2C device of CONV
12	P140	NW_RST	O		O	O	Reset signal to Net-module
13	BYTE	BYTE	MCU		MCU	MCU	Vss : When single chip mode is used
14	CNVss	CNVss	MCU		MCU	MCU	Vss : When single chip mode is used, Vcc : When flash writing is used
15	P87/Xcin	MUTETI	O		O	O	MUTE of TI decoder DSP DA70Y (HI=MUTE)
16	P86/Xcout	/TIBUSY	I		O	O	TI BUSY detection / CDDA writing DATA input
17	/RESET	/RES	MCU		MCU	MCU	Reset
18	Xout	Xout	MCU		MCU	MCU	Oscillation output
19	Vss	Vss	MCU		MCU	MCU	Ground for microprocessor
20	Xin	Xin	MCU		MCU	MCU	Oscillation input
21	Vcc1	Vcc	MCU		MCU	MCU	Power supply +5V for microprocessor
22	P85/NMI	NMI	MCU		MCU	MCU	No used, connect Vss
23	P84/INT2	/INTTI	IRQ		O	O	Interrupt of TI decoder DSP DA70Y
24	P83/INT1	/INTDIR	IRQ		O	O	Interrupt of DIR
25	P82/INT0	/VSY	IRQ	O	O	O	
26	P81/TA4in/U	/CSDIR	O		O	O	Chip enable of DIR
27	P80/TA4out/U	/CSTI	O		O	O	Chip enable of TI decoder DSP DA70Y
28	P77/TA3in	/CSDAC	O		O	O	Chip enable of DAC (2ch/8ch common)
29	P76/TA3out	/ICDIR	O		O	O	DIR reset
30	P75/TA2in/W	/ICTI	O		O	O	Reset of TI decoder DSP DA70Y
31	P74/TA2out/W	/SPIRDY	I		O	O	TI DA601 Serial Ready / WCK input for CDDA writing
32	P73/CTS2/RTS2/TA1in/V	/CEEEP	O		O	O	EEPROM CE
33	P72/CLK2/TA1out/V	FET	O		O	O	Control of flash writing
34	P71/RXD2/SCL2/TA0in/TB5in	DRXM	SI		O	O	XMDT IC RxDU (U model)
35	P70/TXD2/SDA2/TA0out	DTXM	SO		O	O	XMDT IC TxDU
36	P67/TXD1/SDA1	SDA	SO	I	I	I	
		TXDF	SO				Data transmission terminal of AF220
37	Vcc1	Vcc	MCU		MCU	MCU	Power supply +5V for microprocessor
38	P66/RXD1/SCL1	SCL	SO	I	I	I	
		RXDF	SO				Flash ROM RxD
39	Vss	Vss	MCU		MCU	MCU	Ground for microprocessor
40	P65/CLK1	N.C.	O		O	O	
		CLKF	SO				Clock transmission terminal signal output for AF220
41	P64/CTS1/RTS1/CTS0/CLKS1	BSY	O				BUSY signal output for AF220
42	P63/TXD0/SDA0	TXDi	SO		O	O	serial data output for iPod
		TXDNW	SO		O	O	
43	P62/RXD0/SCL0	RXDi	SI		O	O	Serial data input for iPod
		RXDNW	SI		O	O	
44	P61/CLK0	iPDET	I		O	O	iPod detection
45	P60/CTS0/RTS0	iPAP	I		O	O	IPod accessories power detection
46	P137	Z2RY	O		O	O	
		YST	O		O	O	YST amp control (HTR-5935 model)
47	P136	/4ohm	O		O	O	IMPEDANCE control / ±B voltage control
48	P135	SBRY	O		O	O	SURROUND BACK SP relay output
49	P134	SPC	O		O	O	CENTER and SURROUND SP relay output
50	P57/RDY/CLKout	SPB	O		O	O	FRONT B SP relay output

IC2 : M30625MHP-A98GP (DSP P.C.B.)
Microprocessor

No.	Port Name	Terminal Name	I/O				Function
			PowerOn	Pure Direct	Standby	Sleep	
51	P56/ALE	SPA	O		O	O	FRONT A SP relay output
52	P55/HOLD	/EMP	I				For FLASH writing (LO)
53	P54/HLDA	PRI	I		O	O	Protection overcurrent detection
54	P133	PSV	O		O	O	Power Save
55	P132	PRY	O		O	O	Power relay output
56	P131	MASTER	I		O	O	MASTER ON/OFF
57	P130	/BLK	O		O	O	FL Driver turning off
58	P53/BCLK	ISA	I		O	O	INPUT Selector Rotary A
59	P52/RD	ISB	I		O	O	INPUT Selector Rotary B
60	P51/WRH/BHE	TONEA	I		O	O	Tone Control Rotary A
61	P50/WRL/WR	/CE	I				For FLASH writing (HI)
62	P127	TONEB	I		O	O	Tone Control Rotary B
63	P126	VRA	I		O	O	Volume Rotary A
64	P125	VRB	I		O	O	Volume Rotary B
65	P47/CS3	VIA	O	O	O	O	VIDEO Selector A
66	P46/CS2	VIB	O	O	O	O	VIDEO Selector B
67	P45/CS1	VIC	O	O	O	O	VIDEO Selector C
68	P44/CS0	S/V	O	O	O	O	
69	P43/A19	/CES	O	O	O	O	OSD Enable
		MOD1	I				MODEL distinction 1
70	P42/A18	SVIDD	I	O	O	O	S-Video Signal Detector
71	P41/A17	BYPASS	O	O	O	O	VIDEO Bypass/ conversion change
72	P40/A16	/INTCNV	I	O	O	O	
73	P37/A15	/VR1	O	O	O	O	VIDEO Rec Out 1 MUTE
74	P36/A14	/VR2	O	O	O	O	
75	P35/A13	/PURD	O		O	I	
76	P34/A12	/MON	O	O	O	O	VIDEO Mon Out MUTE
77	P33/A11	CPNTD	I	O	O	O	Component Signal Detector (DVD)
78	P32/A10	CMP0	O	O	O	O	Component Selector 0
79	P31/A9	CMP1	O	O	O	O	Component Selector 1
80	P124	CBYPASS	O	O	O	O	
81	P123	/CNONE	O	O	O	O	Component Mon Out MUTE
82	P122	TRIG	O		O	O	DC TRIGGER input
83	P121	TMT	O		O	O	TUNER MUTE
84	P120	SDRN	I		O	O	RDS RxDBG
85	Vcc2	Vcc	MCU		MCU	MCU	Power supply +5V for microprocessor
86	P30/A8	SCKN	O		O	O	RDS IC Clock (G model)
			O	O	O	O	
87	Vss	Vss	MCU		MCU	MCU	Ground for micro-processor
88	P27/A7	SDTN	O		O	O	RDS IC TxD (G model)
			O	O	O	O	
89	P26/A6	RDSE	O		O	O	RDS Enable (G model)
		/ICXM	O		O	O	DABIC IC reset (U model)
90	P25/A5	SCKP	O		O	O	PLL IC Clock
91	P24/A4	SDTP	O		O	O	PLL IC TxD
92	P23/A3	CEP	O		O	O	PLL IC Enable
93	P22/A2	SDRP	I+		O	O	PLL IC RxD
94	P21/A1	/ST	I+		O	O	TUNER /ST
95	P20/A0	TUNED	I+		O	O	TUNED
96	P17/D15/INT5	PDET	IRQ		IRQ	O	Power Down DETECT INT
97	P16/D14/INT4	/PSW	IRQ		IRQ	O	Interrupt MASTER / MAIN / Zone2 Power SW
98	P15/D13/INT3	REM	IRQ		IRQ	O	Remote Control input
99	P14/D12	/HP	I		O	O	HEAD PHONE detection
100	P13/D11	/MTHP	O		O	O	HEAD PHONE MUTE input
101	P12/D10	/MTFS	O		O	O	MUTE Front/Surround, PreOUT
102	P11/D9	/MTCT	O		O	O	MUTE Center
103	P10/D8	/MTSW	O		O	O	MUTE SW
104	P07/D7	/MTZ2	O		O	O	Zone 2 MUTER
105	P06/D6	CKEV	O		O	O	Electron volume IC Clock

IC2 : M30625MHP-A98GP (DSP P.C.B.)
Microprocessor

No.	Port Name	Terminal Name	I/O				Function
			PowerOn	Pure Direct	Standby	Sleep	
106	P05/D5	DTEV	O		O	O	Electron volume IC DATA
107	P04/D4	CKZ2	O		O	O	Zone2 Selector (BD3841) Clock (R model)
108	P03/D3	DTZ2	O		O	O	Zone2 Selector (BD3841) DATA (R model)
109	P02/D2	N.C.	O		O	O	
110	P01/D1	N.C.	O		O	O	
111	P00/D0	CKEX	O		O	O	EX. INPUT Selector Clock
112	P117	DTEX	O		O	O	EX. INPUT Selector DATA
113	P116	CKBD	O		O	O	
114	P115	DTBD	O		O	O	
		MOD2			I		MODEL distinction 2
115	P114	DTSEL	O		O	O	
116	P113	CKSEL	O		O	O	
117	P112	CESEL	O		O	O	
		MOD4			I		MODEL distinction
118	P111	ICEV	O		O	O	
119	P110	CEEV	O		O	O	
		MOD3			I		
120	P107/AN7/KI3	PRV2	AD		O	O	
121	P106/AN6/KI2	PRV1	AD		O	O	AD protection power-supply voltage detection
122	P105/AN5/KI1	PRD	AD		O	O	AD protection DC detection
123	P104/AN4/KI0	PLDET	AD		O	O	AD POWER LIMITTER detection
124	P103/AN3	THM	AD		O	O	AD temperature detection
125	P102/AN2	ADKEY0	AD		O	O	AD Key 0
126	P101/AN1	ADKEY1	AD		O	O	AD Key 1
127	Avss	Avss	MCU		MCU	MCU	Ground for AD
128	P100/AN0	DEST	AD		O	O	AD model detection

RX-V459/HTR-5940/DSP-AX459/HTR-5935
Key Input(A-D) Pull-Up Resistance 10 k-Ohms

Ohm	+0.0k	+1.0k	+1.0k	+1.5k	+2.2k	+3.3k	+4.7k	+4.7k	+6.8k	+10.0k	+22.0k
V	~0.3	~0.7	~1.0	~1.5	~2.0	~2.6	~3.1	~3.4	~3.7	~4.0	~4.4
ADKEY0 94pin/AN2	PROGRAM <	PROGRAM >	BASS/TREBLE +	BASS/TREBLE +	INPUT MODE	STRAIGHT	TONE CONTROL	PRESET/TUNING	SPEAKER B	SPEAKER A	PURE DIRECT
ADKEY1 95pin/AN1	–	–	–	–	MULTI CH INPUT	FM/AM	A/B/C/D/E	PRESET/TUNING <	PRESET/TUNING >	MEMORY	TUNING MODE

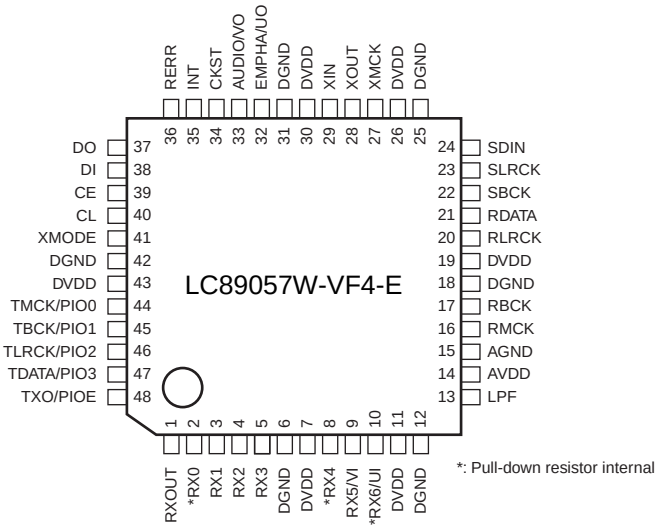
MODEL Distinction Port / モデル判別ポート

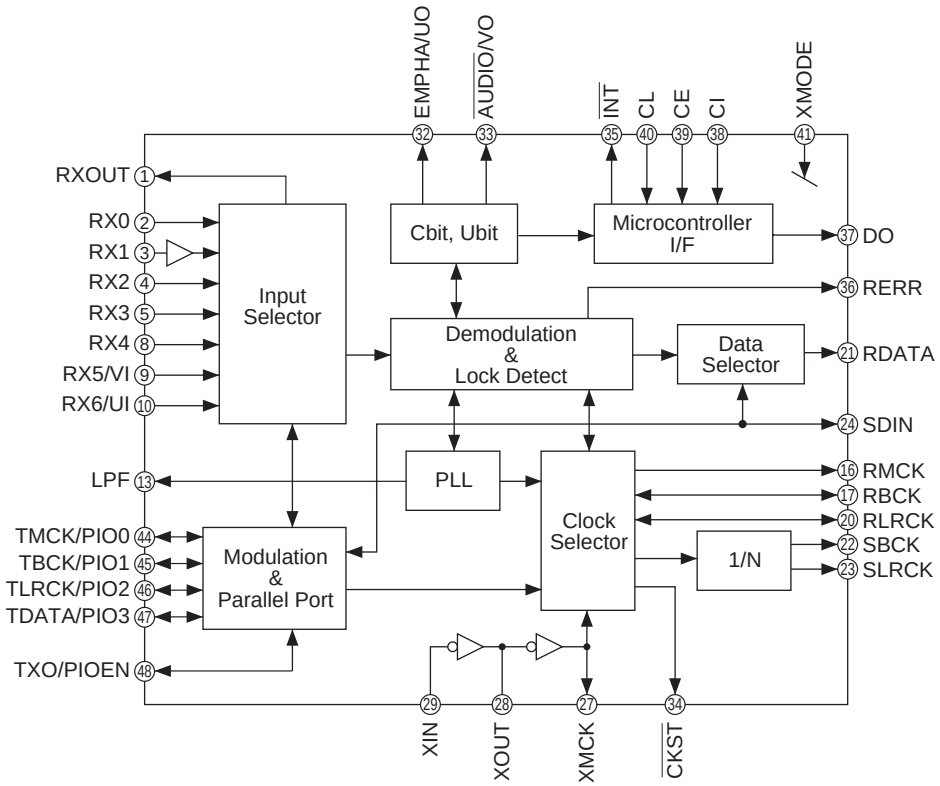
Pin	Function	Name	RX-V459/HTR-5940/DSP-AX459	HTR-5935
3	P97/Adtrg/Sin4	CEFD/MOD0	1	0
69	P43/A19	CES/MOD1	1	1
114	P115	DTBD/MOD2	1	1
119	P110	CEEV/MOD3	0	0
117	P112	CESEL/MOD4	0	0

Distinction for AD Port / 仕向け先判別ポート
Pull-Up Resistance 10 k-Ohms

Ohm	0.0k	1.2k	2.7k	4.7k	6.8k	10.0k	15.0k	27.0k	47.0k	100.0k	∞
V	0-0.2	0.3-0.8	0.9-1.3	1.4-1.8	1.8-2.2	2.3-2.7	2.8-3.3	3.4-3.8	3.9-4.3	4.4-4.7	4.8-5.0
A-D (5V=255)	0-13	14-40	41-68	69-92	93-115	116-140	141-170	171-198	199-221	222-244	245-255
DEST 129pin	J	U, C	–	R	T	K	A	–	G, E	L	–

IC56 : LC89057W-VF4-E (DSP P.C.B)
Digital Audio Interface Transceiver





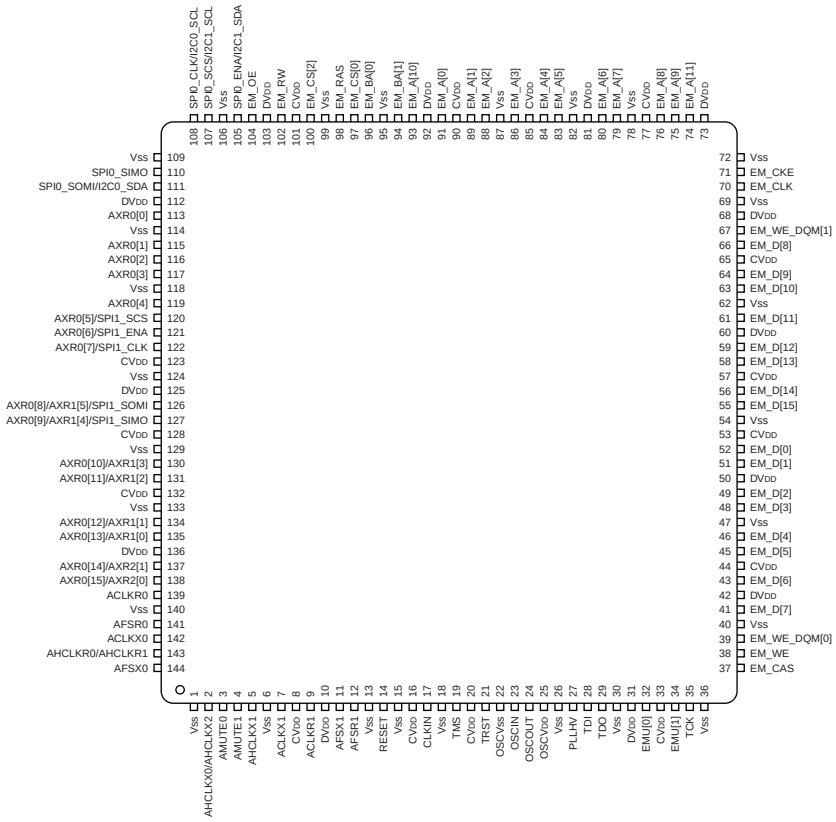
IC56 : LC89057W-VF4-E (DSP P.C.B)
Digital Audio Interface Transceiver

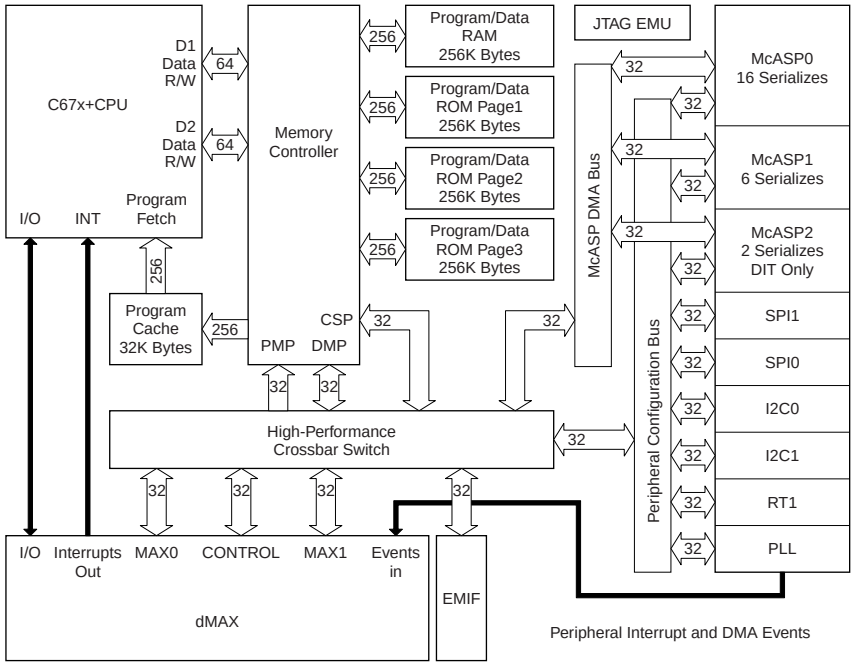
No.	Name	I/O	Function
1	RXOUT	O	Input bi-phase selection data output pin
2	RX0	Is	TTL-compatible digital data input pin
3	RX1	I	Coaxial-compatible digital data input pin with built-in amplifier
4	RX2	Is	TTL-compatible digital data input pin
5	RX3	Is	TTL-compatible digital data input pin
6	DGND		Digital GND
7	DVDD		Digital power supply
8	RX4	Is	TTL-compatible digital data input pin
9	RX5/VI	Is	TTL-compatible digital data / Validity flag input pin for modulation
10	RX6/UI	Is	TTL-compatible digital data / User data input pin for modulation
11	DVDD		PLL digital power supply
12	DGND		PLL digital GND
13	LPF	O	PLL loop filter connection pin
14	ACDD		PLL analog power supply
15	AGND		PLL analog GND
16	RMCK	O	R system clock output pin (256fs, 512fs, XIN, VCO)
17	RBCK	O/I	R bit clock input/output pin
18	DGND		Digital GND
19	DVDD		Digital power supply
20	RLRCK	O/I	R LR clock input/output pin (fs)
21	RDATA	O	Serial audio data input pin
22	SBCK	O	S bit clock output pin (32fs, 64fs, 128fs)
23	SLRCK	O	S LR clock output pin (fs/s, fs, 2fs)
24	SDIN	Is	Serial audio data input pin
25	DGND		Digital GND
26	DVDD		Digital power supply
27	XMCK	O	Oscillation amplifier output pin
28	XOUT	O	Crystal resonator connection output pin
29	XIN	I	Crystal resonator connection, external supply clock input pin (24.576 MHz or 12.288 MHz)
30	DVDD		Digital power supply
31	DGND		Digital GND
32	EMPHA/UO	I/O	Emphasis information / U data output / Chip address setting pin
33	AUDIO/VO	I/O	Non-PCM output / V flag output / Chip address setting pin
34	CKST	I/O	Clock switch transition period signal / Demodulation master or slave function switch pin
35	INT	I/O	Microcontroller interrupt output / Modulation or general-purpose I/O switch pin
36	RERR	O	PLL clock error, data error flag output
37	DO	O	Microcontroller I/F read data output pin (3-state)
38	DI	Is	Microcontroller I/F write data input pin
39	CE	Is	Microcontroller I/F chip enable input pin
40	CL	Is	Microcontroller I/F clock input pin
41	XMODE	Is	System reset input pin
42	DGND		Digital GND
43	DVDD		Digital power supply
44	TMCK/PIO0	I/O	Modulation 256fs system clock input / General-purpose I/O input/output pin
45	TMCK/PIO1	I/O	Modulation 64fs bit clock input / General-purpose I/O input/output pin
46	TLRCK/PIO2	I/O	Modulation fs clock input / General-purpose I/O input/output pin
47	TLRCK/PIO3	I/O	Modulation serial audio data input / General-purpose I/O input/output pin
48	TXO/PIOEN	O/I	Modulation data output / General-purpose I/O enable input pin

1) Input/output I or O = -0.3 to 3.6V, Is = -0.3 to 5.5V
2) Pins 32 and 33 are latch address setting input pins when pin 41 = "L".
3) Pin 34 is a demodulation function master or slave setting input pin when pin 41 = "L".
4) Pin 35 is a modulation function or general-purpose I/O function switch setting input pin when pin 41 = "L".
5) Perform ON/OFF for all power supplies with the same timing as a latch-up countermeasure.

IC60 : D70YE101RFP250 (DSP P.C.B)
Decoder/Post Processor

* No replacement part available. / サービス部品供給なし





IC60 : D70YE101RFP250 (DSP P.C.B)
Decoder/Post Processor

PIN NO.	SIGNAL NAME	TYPE(1)	PULL(2)	GPIO(3)	DESCRIPTION
1	Ground(Vss)				
2	AHCLKX0/AHCLKX2	IO	-	Y	McASP0 and McASP2 Transmit Master Clock
3	AMUTE0	IO	-	Y	McASP0 MUTE Output
4	AMUTE1	IO	-	Y	McASP1 MUTE Output
5	AHCLKX1	IO	-	Y	McASP1 Transmit Master Clock
6	Ground(Vss)				
7	ACLKX1	IO	-	Y	McASP1 Transmit Bit Clock
8	Core Supply (CVpp)				
9	ACLKR1	IO	-	Y	McASP1Receive Bit Clock
10	IO Supply (DVpp)				
11	AFSX1	IO	-	Y	McASP1 Transmit Frame Sync (L/R Clock)
12	AFSR1	IO	-	Y	McASP1Receive Frame Sync (L/R Clock)
13	Ground(Vss)				
14	RESET	IO	-	N	Device reset pin
15	Ground(Vss)				
16	Core Supply (CVpp)				
17	CLKIN	IO	-	N	Alternate clock input (3.3-V LVCMOS Input)
18	Ground(Vss)				
19	TMS	IO	IPU	N	Test mode Select
20	Core Supply (CVpp)				
21	TRST	IO	IPU	N	Test Reset
22	OSCVss	PWR	-	N	Oscillator Vss tap point (for filter only)
23	OSCIN	IO	-	N	1.2-V Oscillator Input
24	OSCOUT	O	-	N	1.2-V Oscillator Output
25	OSCVpp	PWR	-	N	Oscillator 1.2-V Vpp tap point (for filter only)
26	Ground(Vss)				
27	PLLHV	PWR	-	N	PLL 3.3-V Supply Input (requires external filter)
28	TDI	IO	IPU	N	Test Data In
29	TDO	OZ	IPU	N	Test Data Out
30	Ground(Vss)				
31	IO Supply (DVpp)				
32	EMU[0]	IO	IPU	N	Emulation Pin 0
33	Core Supply (CVpp)				
34	EMU[1]	IO	IPU	N	Emulation Pin 1
35	TCK	IO	IPU	N	Test Clock
36	Ground(Vss)				
37	EM_CAS	O	-	N	SDRAM Column Address Strobe
38	EM_WE	O	-	N	SDRAM Write Enable
39	EM_WE_DQM[0]	O	-	N	Write Enable or Byte Enable for EM_D[7:0]
40	Ground(Vss)				
41	EM_D[7]	IO	-	N	EMIF Data Bus [lower 16 Bits]
42	IO Supply (DVpp)				
43	EM_D[6]	IO	-	N	EMIF Data Bus [lower 16 Bits]
44	Core Supply (CVpp)				
45	EM_D[5]	IO	-	N	EMIF Data Bus [lower 16 Bits]
46	EM_D[4]	IO	-	N	EMIF Data Bus [lower 16 Bits]
47	Ground(Vss)				
48	EM_D[3]	IO	-	N	EMIF Data Bus [lower 16 Bits]
49	EM_D[2]	IO	-	N	EMIF Data Bus [lower 16 Bits]
50	IO Supply (DVpp)				
51	EM_D[1]	IO	-	N	EMIF Data Bus [lower 16 Bits]
52	EM_D[0]	IO	-	N	EMIF Data Bus [lower 16 Bits]
53	Core Supply (CVpp)				
54	Ground(Vss)				
55	EM_D[15]	IO	-	N	EMIF Data Bus [lower 16 Bits]

IC60 : D70YE101RFP250 (DSP P.C.B)
Decoder/Post Processor

PIN NO.	SIGNAL NAME	TYPE(1)	PULL(2)	GPIO(3)	DESCRIPTION
56	EM_D[14]	IO	-	N	EMIF Data Bus [lower 16 Bits]
57	Core Supply (CVpp)				
58	EM_D[13]	IO	-	N	EMIF Data Bus [lower 16 Bits]
59	EM_D[12]	IO	-	N	EMIF Data Bus [lower 16 Bits]
60	IO Supply (DVpp)				
61	EM_D[11]	IO	-	N	EMIF Data Bus [lower 16 Bits]
62	Ground(Vss)				
63	EM_D[10]	IO	-	N	EMIF Data Bus [lower 16 Bits]
64	EM_D[9]	IO	-	N	EMIF Data Bus [lower 16 Bits]
65	Core Supply (CVpp)				
66	EM_D[8]	IO	-	N	EMIF Data Bus [lower 16 Bits]
67	EM_WE_DQM[1]	O	-	N	Write Enable or Byte Enable for EM_D[15:8]
68	IO Supply (DVpp)				
69	Ground(Vss)				
70	EM_CLK	O	-	N	SDRAM Clock
71	EM_CKE	O	-	N	SDRAM Clock Enable
72	Ground(Vss)				
73	IO Supply (DVpp)				
74	EM_A[11]	O	-	N	EMIF Address Bus
75	EM_A[9]	O	-	N	EMIF Address Bus
76	EM_A[8]	O	-	N	EMIF Address Bus
77	Core Supply (CVpp)				
78	Ground(Vss)				
79	EM_A[7]	O	-	N	EMIF Address Bus
80	EM_A[6]	O	-	N	EMIF Address Bus
81	IO Supply (DVpp)				
82	Ground(Vss)				
83	EM_A[5]	O	-	N	EMIF Address Bus
84	EM_A[4]	O	-	N	EMIF Address Bus
85	Core Supply (CVpp)				
86	EM_A[3]	O	-	N	EMIF Address Bus
87	Ground(Vss)				
88	EM_A[2]	O	-	N	EMIF Address Bus
89	EM_A[1]	O	-	N	EMIF Address Bus
90	Core Supply (CVpp)				
91	EM_A[0]	O	-	N	EMIF Address Bus
92	IO Supply (DVpp)				
93	EM_A[10]	O	-	N	EMIF Address Bus
94	EM_BA[1]	O	-	N	SDRAM Bank Address and Asynchronous Memory LOW-Order Address
95	Ground(Vss)				
96	EM_BA[0]	O	-	N	SDRAM Bank Address and Asynchronous Memory LOW-Order Address
97	EM_CS[0]	O	-	N	SDRAM Chip Select
98	EM_RAS	O	-	N	SDRAM Row Address Strobe
99	Ground(Vss)				
100	EM_CS[2]	O	-	N	Asynchronous Memory Chip Select
101	Core Supply (CVpp)				
102	EM_RW	O	-	N	Asynchronous Memory Read/not Write
103	IO Supply (DVpp)				
104	EM_OE	O	-	N	SDRAM Output Enable
105	SPI0_ENA/I2C1_SDA	IO	-	Y	SPI0 Enable (Ready) or I2c1 Serial Data
106	Ground(Vss)				
107	SPI0_SCS/I2C1_SCL	IO	-	Y	SPI0 Slave Chip Select or I2c1 Serial Clock
108	SPI0_CLK/I2C0_SCL	IO	-	Y	SPI0 Serial Clock or I2c0 Serial Clock
109	Ground(Vss)				
110	SPI0_SIMO	IO	-	Y	SPI0 Data Pin Slave In Master Out

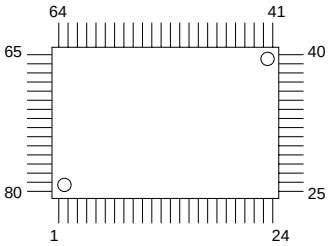
IC60 : D70YE101RFP250 (DSP P.C.B)
Decoder/Post Processor

PIN NO.	SIGNAL NAME	TYPE(1)	PULL(2)	GPIO(3)	DESCRIPTION
111	SPI0_SOMI/I2C0_SDA	IO	-	Y	SPI0 Data Pin Slave Out Master In or I2C0 Serial Data
112	IO Supply (DVpp)				
113	AXR0[0]	IO	-	Y	McASP0 Serial Data 0
114	Ground(Vss)				
115	AXR0[1]	IO	-	Y	McASP0 Serial Data 1
116	AXR0[2]	IO	-	Y	McASP0 Serial Data 2
117	AXR0[3]	IO	-	Y	McASP0 Serial Data 3
118	Ground(Vss)				
119	AXR0[4]	IO	-	Y	McASP0 Serial Data 4
120	AXR0[5]/SOI1_SCS	IO	-	Y	McASP0 Serial Data 5 or SPI1 Slave Chip Select
121	AXR0[6]/SPI1_ENA	IO	-	Y	McASP0 Serial Data 6 or SPI1 Enable (Ready)
122	AXR0[7]/SPI1_CLK	IO	-	Y	McASP0 Serial Data 7 or SPI1 Serial Clock
123	Core Supply (CVpp)				
124	Ground(Vss)				
125	IO Supply (DVpp)				
126	AXR0[8]/AXR1[5]/SPI1_SOMI	IO	-	Y	McASP0 Serial Data 8 or McASP1 Serial Data 5 or SPI1 Data Pin Slave Out Master In
127	AXR0[9]/AXR1[4]/SPI1_SIMO	IO	-	Y	McASP0 Serial Data 9 or McASP1 Serial Data 4 or SPI1 Data Pin Slave In Master Out
128	Core Supply (CVpp)				
129	Ground(Vss)	IO	-	Y	
130	AXR0[10]/AXR1[3]	IO	-	Y	McASP0 Serial Data 10 or McASP1 Serial Data 3
131	AXR0[11]/AXR1[2]				McASP0 Serial Data 11 or McASP1 Serial Data 2
132	Core Supply (CVpp)				
133	Ground(Vss)	IO	-	Y	
134	AXR0[12]/AXR1[1]	IO	-	Y	McASP0 Serial Data 12 or McASP1 Serial Data 1
135	AXR0[13]/AXR1[0]				McASP0 Serial Data 13 or McASP1 Serial Data 0
136	IO Supply (DVpp)	IO	-	Y	
137	AXR0[14]/AXR2[1]	IO	-	Y	McASP0 Serial Data 14 or McASP2 Serial Data 1
138	AXR0[15]/AXR2[0]	IO	-	Y	McASP0 Serial Data 15 or McASP2 Serial Data 0
139	ACLKR0				McASP0 Receive bit Clock
140	Ground(Vss)	IO	-	Y	
141	AFSR0	IO	-	Y	McASP0 Receive Frame Sync (L/R Clock)
142	ACLKX0	IO	-	Y	McASP0 Transmit Bit Clock
143	AHCLKR0/AHCLKR1	IO	-	Y	McASP0 and McASP1 Receive Master Clock
144	AFSX0				McASP0 Transmit Frame Sync (L/R Clock)

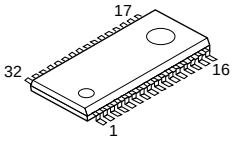
■ PIN CONNECTION DIAGRAM

• ICs

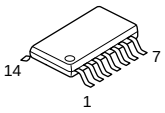
BD3816K1



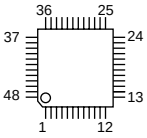
BD3841FS



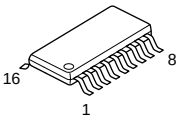
TC74HC4051AF
TC74HC4052AF
TC74HC4053AF
NJM2581M



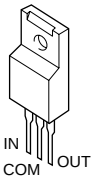
F2602E-01
YAC523-EVR2



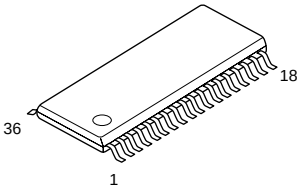
LA7106M-TLM-E
PCM1780DBQR
PCM1781DBQR
PCM1803DBR



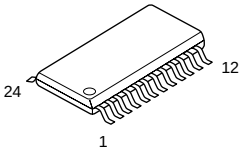
BD3816K1



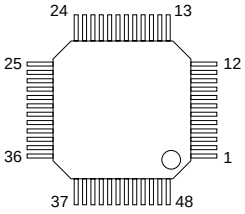
LA73050-TLM-E



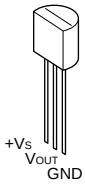
LC72722PM



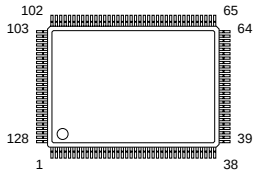
LC89057W-VF4A-E



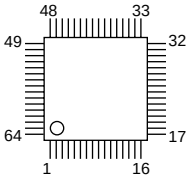
LM61CIZ THERMAL



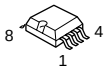
M30625MHP-A98GP



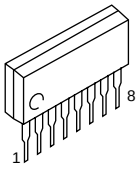
M66003-0131FP



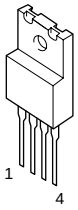
NE5532DR OP AMP



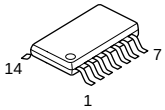
NJM2068LD
NJM2068MD-TE2
NJM4556AL



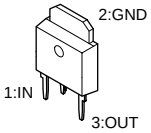
NJM2388F05 5.0V
NJM2388F33



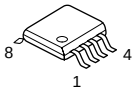
NJM2581M VIDEO AMP



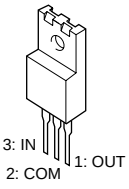
NJM2885DL1-18
NJM2885DL1-33



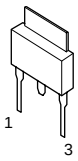
NJM4565M (TE1)



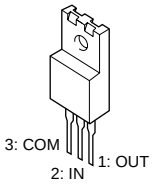
NJM7812FA



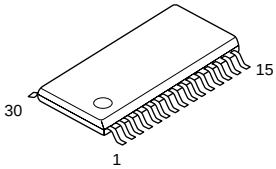
NJM78M05DL1A (TE1)



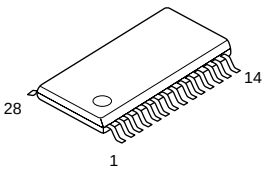
NJM7805FA 5V
NJM79M05FA
NJM79M12FA



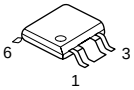
NJU7311AM
NJU7312AM
NJU7313AM



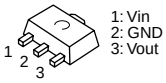
PCM1680DBQR



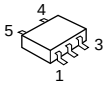
R1172S121D-E2-F



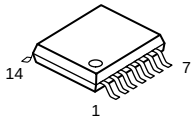
RH5RE58AA-T1-FA



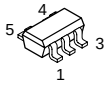
SN74AHC1G08DCKR



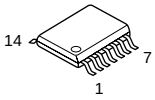
SN74AHCT08PWR



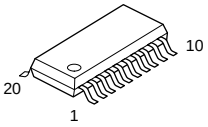
SN74AHCT1G32DCKR



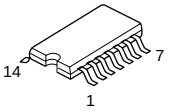
SN74LV157APWR
SN74LVU04APWR



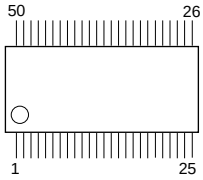
SN74LV245APWR TRAN



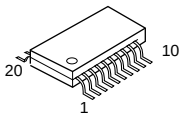
TC4013BP FF
TC74VHCU04FT INVER



W9816G6CH-7 SDRAM



YAC520-EE2

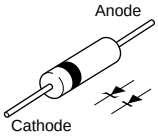


S29AL004D70TF1020

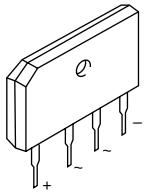
• Diodes

1N4002S
1SS133,176
1SS270A
1SS355
1SS380
1T2
MTZJ13A 13V
MTZJ15A 15V
MTZJ15B 15V
MTZJ2.4B 2.4V
MTZJ27B 27V
MTZJ30A 30V
MTZJ5.1C 5.1V

RB441Q-40 T-77
RB441Q-40 T-77

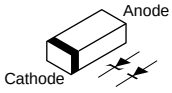


D2SBA20 1.5A 200V
D5SB20 5A 200V

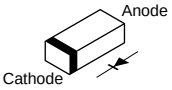


MA8030-L 2.9V
MA8051-M 5.1V
MA8056-M 5.6V
MA8068-L 6.6V
MA8068-M 6.8V
MA8075-H 7.7V
MA8091-M 9.1V
MA8100-M 10V

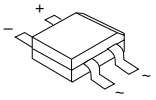
RB500V-40
RB501V-40
UDZ 3.6BTE-17 3.6V
UDZ5.1B 5.1V



MA8082-H 8.5V



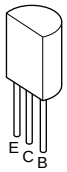
S1NB20 1A 200V
S1NB60 1.0A 600V



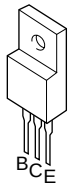
• Transistors

2SA1015 Y
2SA933S Q,R
2SA949 O,Y
2SC1740S QRS
2SC1815 Y
2SC1890A D,E
2SC2229 O,Y
2SC2240 GR,BL

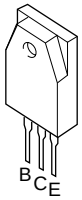
2SC3326 A,B
2SC3837K T146 N,P
2SC3906K T146 R,S



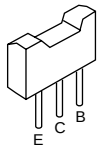
2SB1257
2SB1274 Q,R,S



2SA1695 O,P,Y
2SC4468 O,P,Y
2SD1915F S,T
2SD2014
2SK2158-T2B-A
2SK246 Y
2SK3288
2SK3850



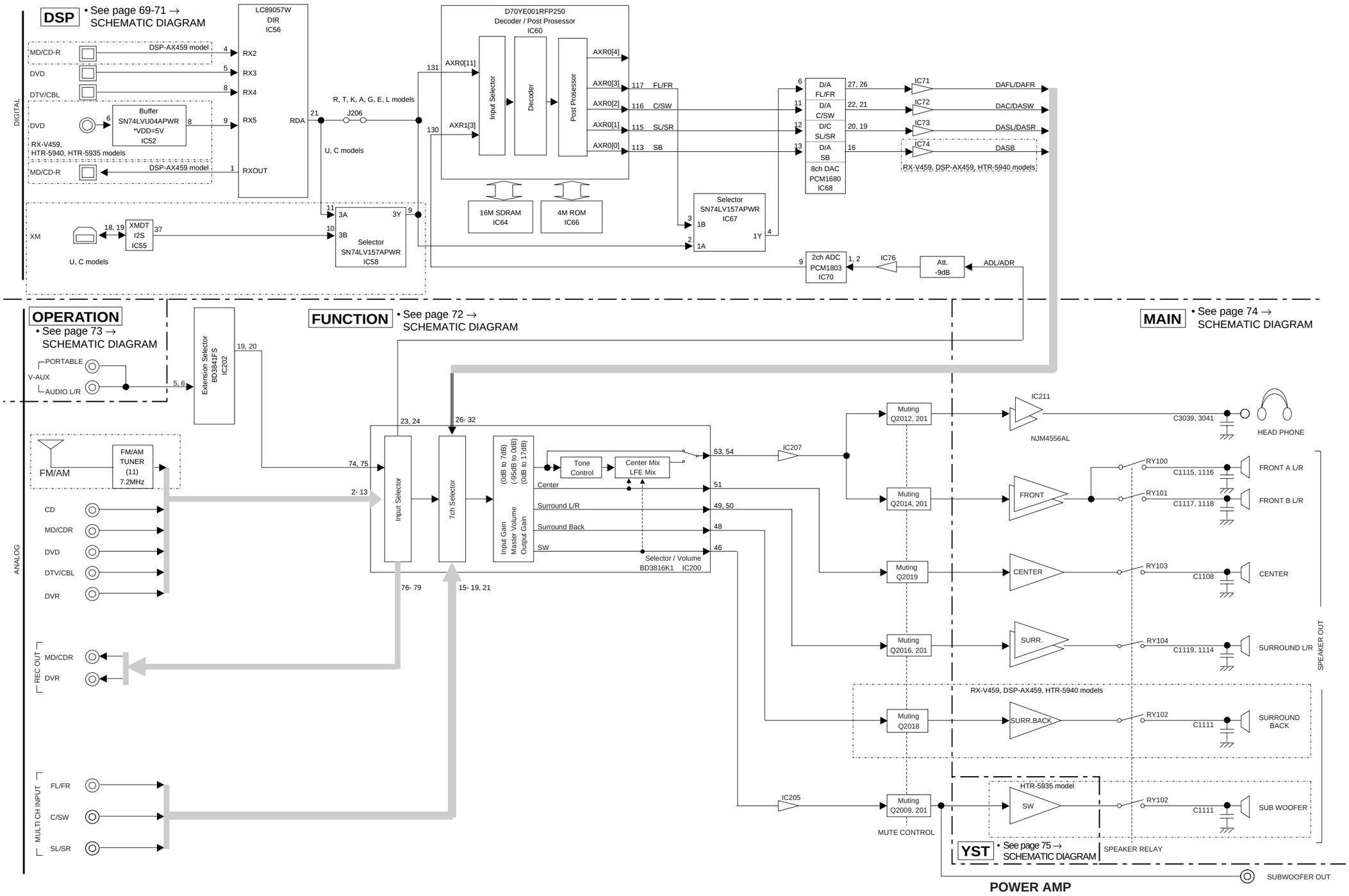
2SA1708 S,T
2SA1770 S,T
2SC4488 S,T
2SC4614 S,T
2SD1938F S,T



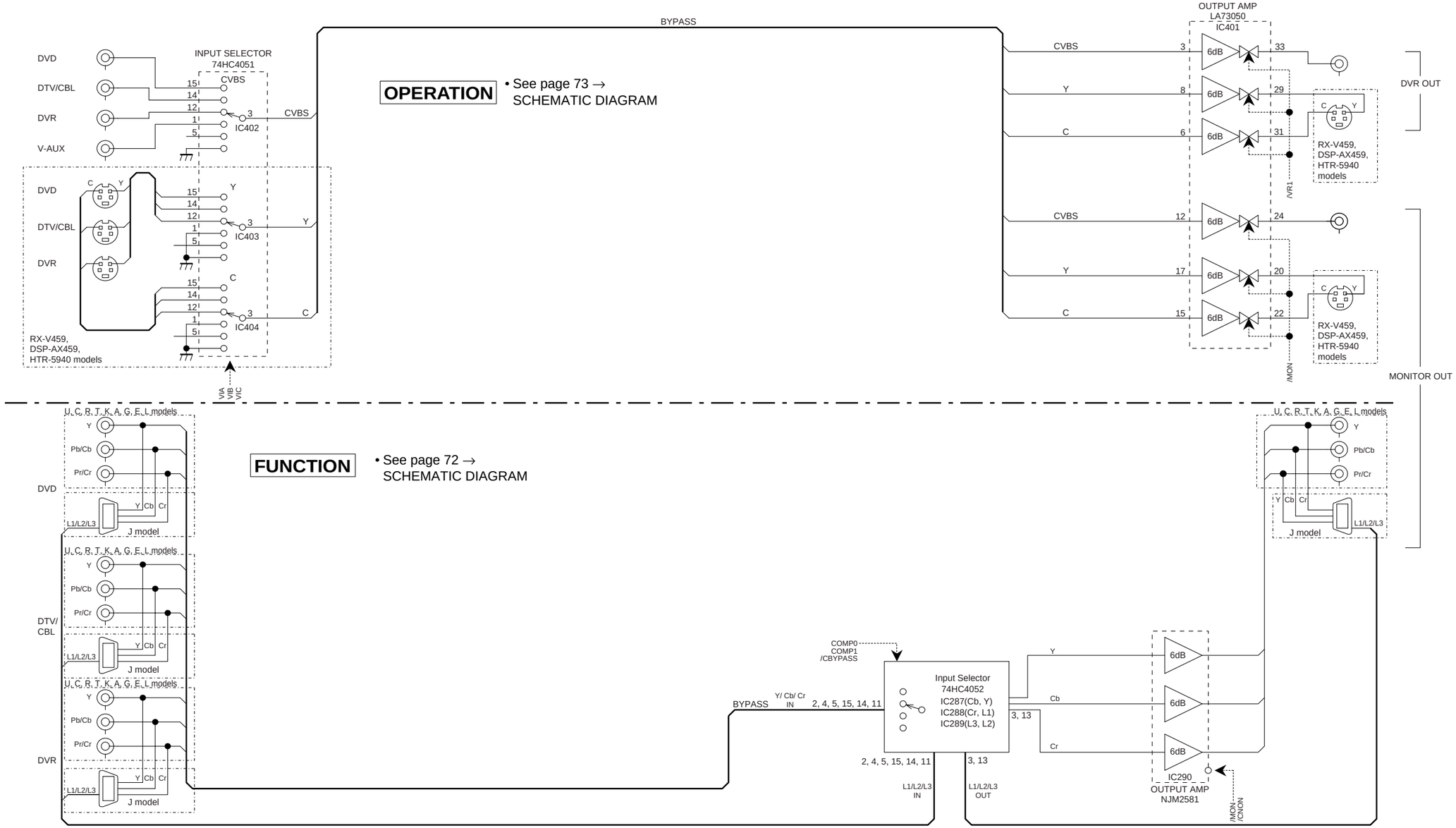
2SA1037K Q,R,S
2SC2412K Q,R,S
DTA114ES
DTC114EKA
DTC114ES
DTC124EKA
DTC144ES

■ BLOCK DIAGRAMS

AUDIO BLOCK DIAGRAM



VIDEO BLOCK DIAGRAM



OPERATION • See page 73 →
SCHEMATIC DIAGRAM

FUNCTION • See page 72 →
SCHEMATIC DIAGRAM

CONTROL/POWER BLOCK DIAGRAM

OPERATION
• See page 73 → SCHEMATIC DIAGRAM

DSP • See page 69-71 → SCHEMATIC DIAGRAM

/RESET 17 | PRI 53 | POWER DETECT 96 | /HP 99 | PRV2 120 | PRV1 121 | PRD 122 | PLDET 123 | THM 124 | DEST. DETECT 128 | MODEL DETECT 3/ 69/ 114 /117/ 119

IR REMOTE U3000 — 98
VOLUME SW300 — 63/ 64
INPUT SELECTOR SW301 — 58/ 59
TONE CONTROL/ DSP PROGRAM SW302 — 60/ 62
MAIN POWER SW SW323 — 97
Tack SW SW302, 304, 306, 309- 319, 321, 322, 324 — 125/ 126
FL DISPLAY V3000 ← FL DRIVER IC301 — 3/ 4/ 5/ 57

Microprocessor M30627 IC2

18 XL1 16MHz 20

6 — LIMITER CONTROL
55 — POWER RELAY
51/ 50/ 49/ 48/ 46 — SPEAKER RELAY
100- 104 — MUTE CONTROL
54 — POWER SAVE
47 — /4ohms
7 — XMPWR
8-10/ 15/ 16/ 23/ 24/ 26- 31 — DSP
12/ 42- 45 — Net-module
34/ 35 — XM
69/ 84/ 86/ 88/ 89/ 117 — RDS
83/ 90- 95 — TUNER
25/ 65- 68, 70- 74, 76- 81 — VIDEO SELECTOR
115/ 116/ 111- 117 — SELECTOR/VOLUME

RY301 — F3001 — F3000/J3002 — TE300

IC300, 302, 303 → Power Detector /Reset Q3006, 3002

D3016 — Q3007

T3000 — s10 — D3018 — RY301 — Q3003

+5.5V IC1

D3 → +5BU
D2 → +5M
D1 — Q1 → +5S
G

POWER RELAY — POWER SAVE

POWER TRANSFORMER

RY105 — /4ohms — D133 — C1105 — C1104 — C1107 — C1106
+B
G
-B

C1100 — C1101 — D1041, 1402, 1044, 1045
+BL
G
-BL
-30V Q1068
-VP

FL1
FL2

C1062 — C1083 — D1035
+12V IC104 → +12
G
-12V IC105 → -12

MAIN • See page 74 → SCHEMATIC DIAGRAM

DSP • See page 69-71→ SCHEMATIC DIAGRAM

+5V IC51 → +5A
E

+5V IC102 → +5D
+3.3V IC54 → +3.3V
+1.2V IC53 → +1.2V
DG

C1087 — C1088 — D1036
+3.3V IC306 → +3.3D
G
-5V IC103 → -5V
+5V IC106 → +5V

VE

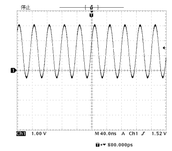
U, C models

C1109 — D1046
+5.3V IC100 → +5.3X
XMPWR
XGND

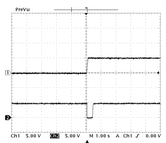
■ SCHEMATIC DIAGRAMS
DSP 1/3

DSP

POINT (A-1) Pin 18 of IC2

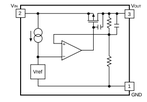


POINT (B-2) ①/ Pin7, ②/ Pin8 of CB3

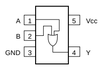


POWER ON
(connect the power cable)

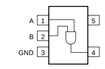
IC1 : RH5RE58AA-T1-FA
Voltage regulator



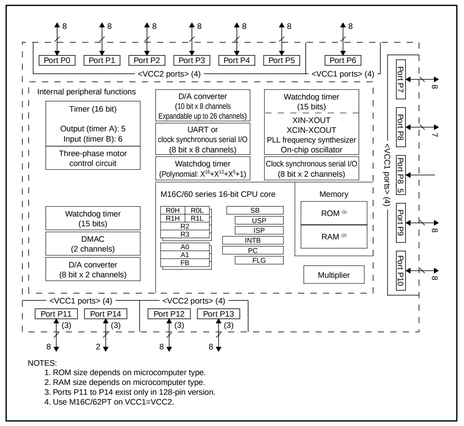
IC4, 5 : SN74AHCT1G32DCKR
Single 2-input positive-OR gate



IC6 : SN74AHC1G08DCKR
2-input positive-AND gate



IC2 : M30625MHP-A98GP
2-input positive-AND gate



NOTES:
1. ROM size depends on microcomputer type.
2. RAM size depends on microcomputer type.
3. Ports P11 to P14 exist only in 128-pin version.
4. Use M16C/62PT on VCC1=VCC2.

NOTICE (mode)
(J)····· JAPAN
(U)····· U.S.A
(C)····· CANADA
(E)····· GENERAL
(T)····· CHINA
(K)····· KOREA
(A)····· AUSTRALIA
(B)····· BRITISH
(G)····· EUROPE
(L)····· SINGAPORE
(E)····· SOUTH EUROPE
(V)····· TAIWAN

★ All voltages are measured with a 10MΩ/V DC electronic volt meter.
★ Components having special characteristics are marked ! and must be replaced with parts having specifications equal to those originally installed.
★ Schematic diagram is subject to change without notice.

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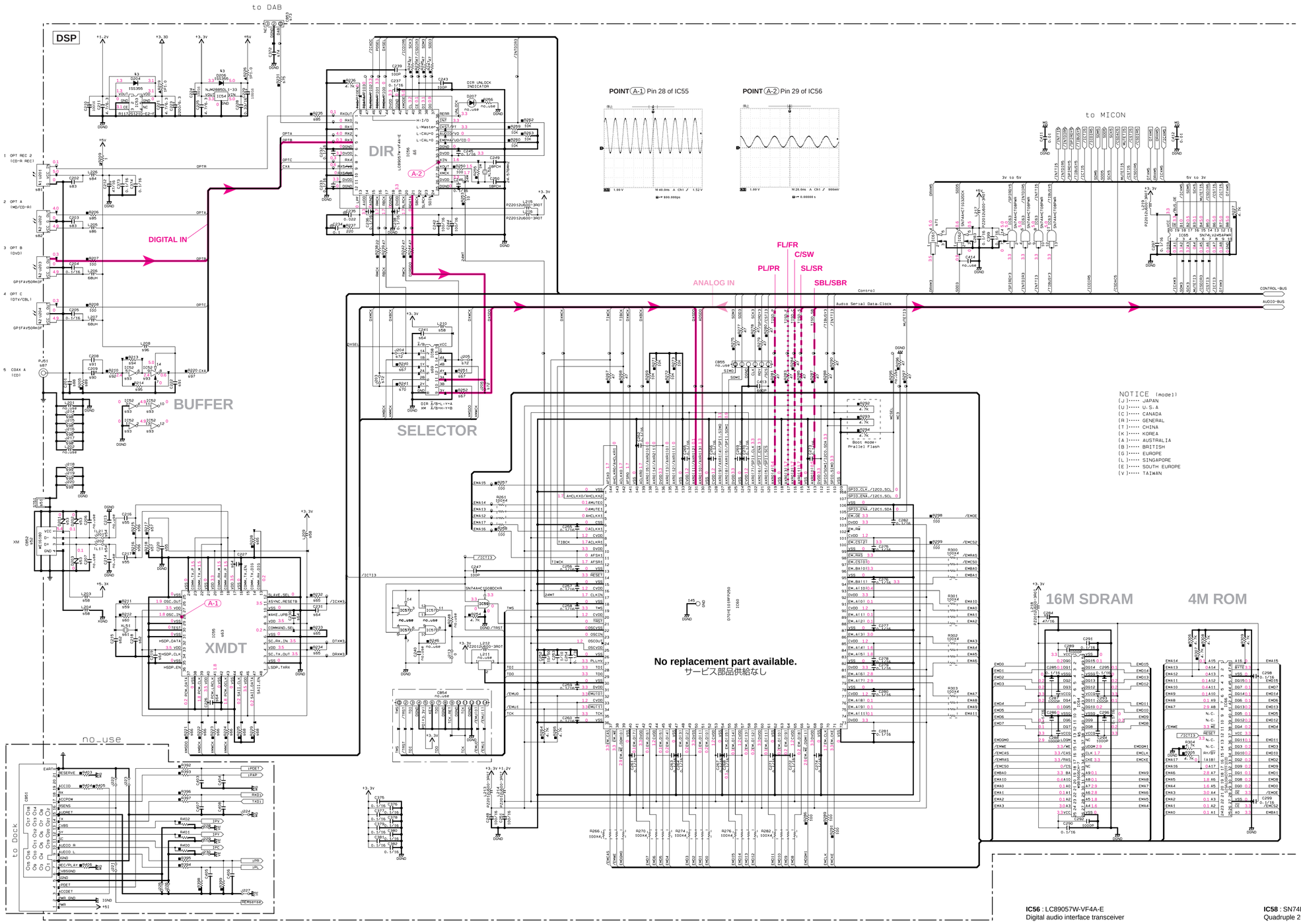
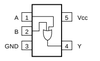
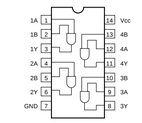
DSP 2/3



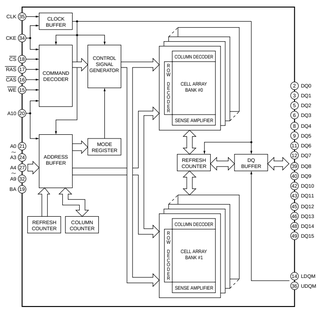
IC61, 62 : SN74AHCT1G32DCKR
Single 2-input positive-OR gate



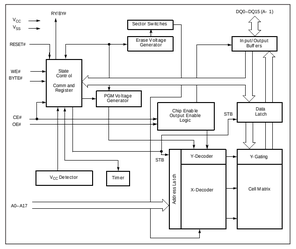
IC63 : SN74AHCT08PWR
Quadruple 2-input positive-AND gates



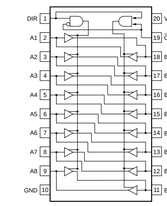
IC64 : W9816G6CH -7
512K x 2 banks x 16 bits SDRAM



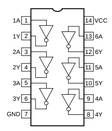
IC66 : S29AL004D70TF1020
4M-bit COMS 3.0 volt-only boot sector flash memory



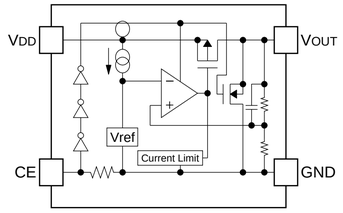
IC65 : SN74LV245APWR
Octal bus transceiver with 3-state outputs



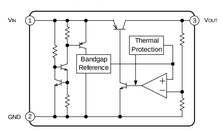
IC52 : SN74LVU04APWR
Hex inverters



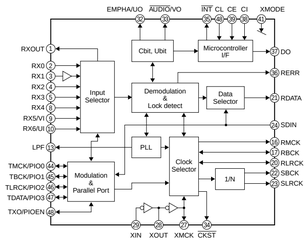
IC53 : R1172S121D-E2-F
Power supply



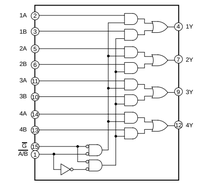
IC54 : NJM2885DL1-33
Low dropout voltage regulator



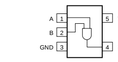
IC56 : LC89057W-VF4A-E
Digital audio interface transceiver



IC58 : SN74LV157APWR
Quadruple 2-line to 1-line data selectors/multiplexers



IC59 : SN74AHC1G08DCKR
2-input positive-AND gate



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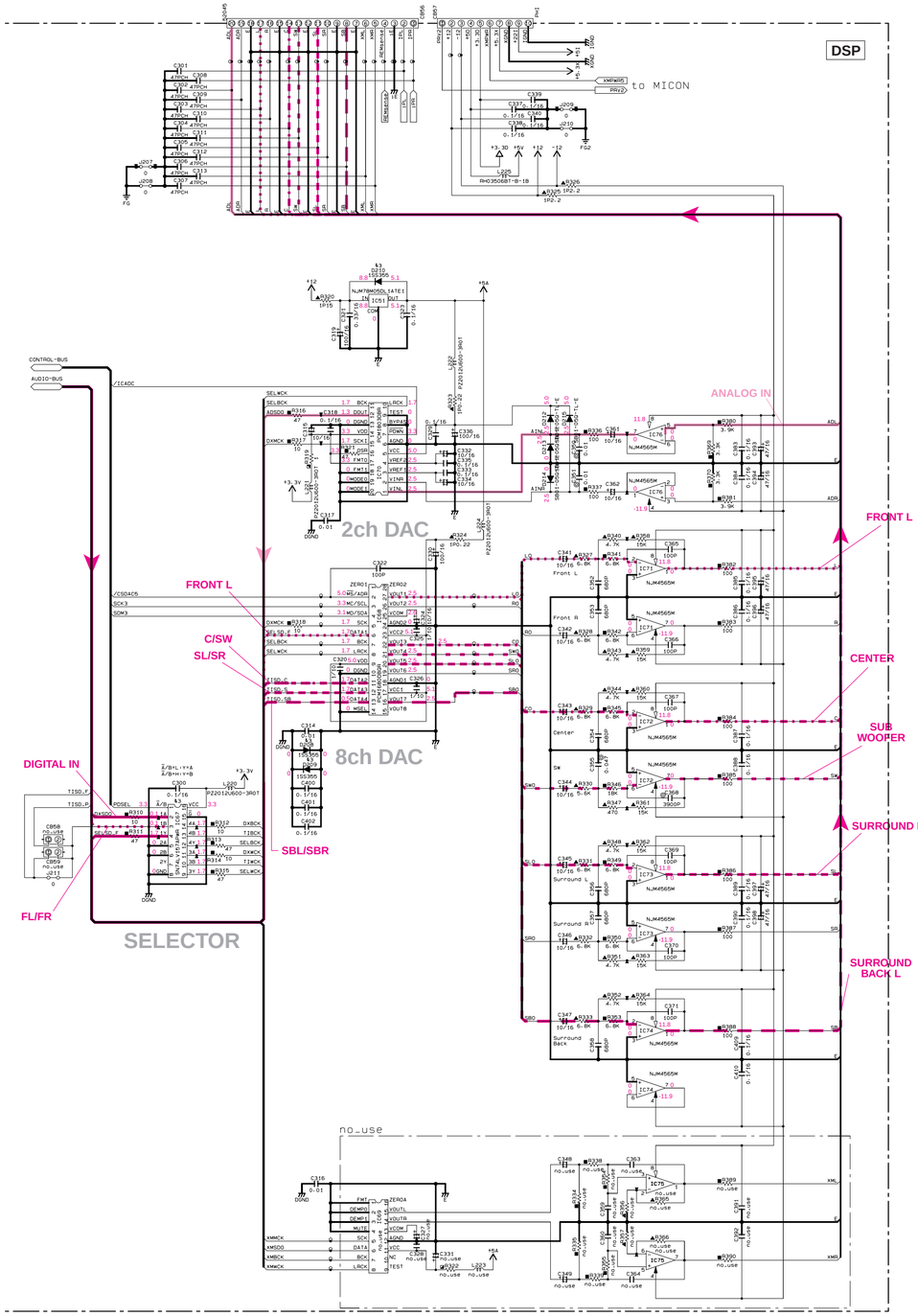
DSP 3/3

Page 72 D2
to FUNCTION (1)_CB202

Page 74 J7
to MAIN (2)_W1004



CAPACITOR

REMARKS	PARTS NAME
NO MARK	ELECTROLYTIC CAPACITOR
⊗	TANTALUM CAPACITOR
NO MARK	CERAMIC CAPACITOR
◉	CERAMIC TUBULAR CAPACITOR
Ⓜ	POLYESTER FILM CAPACITOR
○	POLYSTYRENE FILM CAPACITOR
Ⓜ	MICA CAPACITOR
Ⓟ	POLYPROPYLENE FILM CAPACITOR
◉	SEMICONDUCTIVE CERAMIC CAPACITOR
Ⓢ	POLYPHENYLENE SULFIDE FILM CAPACITOR

RESISTOR

REMARKS	PARTS NAME
NO MARK	CARBON FILM RESISTOR (P=5)
☑	CARBON FILM RESISTOR (P=10)
△	METAL OXIDE FILM RESISTOR
▲	METAL FILM RESISTOR
⊠	METAL PLATE RESISTOR
▨	FIRE PROOF CARBON FILM RESISTOR
□	CEMENT MOLDED RESISTOR
⊘	SEMI VARIABLE RESISTOR
■	CHIP RESISTOR

NOTICE (model)
(J)····· JAPAN
(U)····· U.S.A
(C)····· CANADA
(A)····· GENERAL
(T)····· CHINA
(K)····· KOREA
(A)····· AUSTRALIA
(B)····· BRITISH
(G)····· EUROPE
(L)····· SINGAPORE
(E)····· SOUTH EUROPE
(V)····· TAIWAN

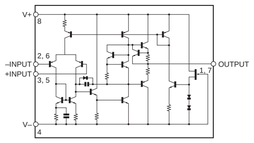
Destination Part List

&XX	LOC	J	UC	R	T	K	A	GE	L
s1	R21	RD35410 10	RD35612 1.2K	RD35647 4.7K	RD35668 6.8K	RD35710 10K	RD35715 15K	RD35747 47K	RD35810 100K
s2	R109	x	x	x	x	x	x	x	x
s3	R111	RD35810 100K	RD35810 100K	RD35810 100K	RD35810 100K	RD35810 100K	RD35810 100K	RD35810 100K	RD35810 100K
s4	R23	RD35715 15K	x	RD35715 15K	RD35715 15K	RD35715 15K	RD35715 15K	RD35715 15K	RD35715 15K
s5	CB8	x	x	x	x	x	x	x	x
s6	R54 R47	x	RD35510 100	x	x	x	x	x	x
s7	R52 R53	x	RD35510 100	x	x	x	x	x	x
s51	ST51	WG45640 EARTH_XW	WG45640 EARTH_XM	x	x	x	x	x	x
s52	CB52	x	WE16180 CAM-C16-004-581	x	x	x	x	x	x
s53	D203 D202 D201	x	WE67480 AVRL1616AIR1NTBT	x	x	x	x	x	x
s54	J201 J202	x	RD35000	x	x	x	x	x	x
s55	C217 C220 C216	x	US03510 0.1/16	x	x	x	x	x	x
s56	R215 R216	x	RD35510 100	x	x	x	x	x	x
s57	R217 R218	x	RD35610 1K	x	x	x	x	x	x
s58	L203 L209 L210 L201	x	WG53720 PZ2012U600-3ROT	x	x	x	x	x	x
s59	R211	x	RD35547 470	x	x	x	x	x	x
s60	R212	x	RD35610 1K	x	x	x	x	x	x
s61	XL51	x	WE43650 45-15840HZ	x	x	x	x	x	x
s62	C215 C218	x	US06050 5PCH	x	x	x	x	x	x
s63	IC55	x	X6Z2780 F2602E-01	x	x	x	x	x	x
s64	C226 C230 C227 C231 C241	x	US13510 0.1/16	x	x	x	x	x	x
s65	R232 R234 R233	x	RD35810 100K	x	x	x	x	x	x
s66	R221 R223 R222	x	RD35527 270	x	x	x	x	x	x
s67	R252 R251 R241	x	RD35447 47	x	x	x	x	x	x
s68	R235 R229	x	RD35847 470K	x	x	x	x	x	x
s69	IC58	x	X6Y2340 SN74LV157APWR	x	x	x	x	x	x
s70	R241	x	RD35422 22	x	x	x	x	x	x
s71	IC61	x	X2DB040 SN74AHCT1G32DCK	x	x	x	x	x	x
s72	J203 J204 J205 J206	RD35000 0	x	RD35000 0	RD35000 0	RD35000 0	RD35000 0	RD35000 0	RD35000 0
s73	CB53	x	x	x	x	x	x	x	x
s74	C372	x	x	x	x	x	x	x	x
s75	R231	x	x	x	x	x	x	x	x
s81	U201	x	x	x	x	x	x	x	x
s82	U202	x	x	x	x	x	x	x	x
s83	C203 C202	x	x	x	x	x	x	x	x
s84	L226	x	x	x	x	x	x	x	x
s85	R206 R235	RD35510 100	x	x	x	x	x	x	x
s86	L205	x	x	x	x	x	x	x	x
s87	FU51	x	Y448390 YKC21-3895N	Y448390 YKC21-3895N	Y448390 YKC21-3895N	Y448390 YKC21-3895N	Y448390 YKC21-3895N	Y448390 YKC21-3895N	Y448390 YKC21-3895N
s88	C201	x	US06122 22PCH	US06122 22PCH	US06122 22PCH	US06122 22PCH	US06122 22PCH	US06122 22PCH	US06122 22PCH
s89	R205	x	RD35482 82	RD35482 82	RD35482 82	RD35482 82	RD35482 82	RD35482 82	RD35482 82
s90	C209	x	UR84722 22/25	UR84722 22/25	UR84722 22/25	UR84722 22/25	UR84722 22/25	UR84722 22/25	UR84722 22/25
s91	C222 C205	x	US13510 0.1/16	US13510 0.1/16	US13510 0.1/16	US13510 0.1/16	US13510 0.1/16	US13510 0.1/16	US13510 0.1/16
s92	R210	x	RD35568 680	RD35568 680	RD35568 680	RD35568 680	RD35568 680	RD35568 680	RD35568 680
s93	IC52	x	X3936A0 SN74LVU04APWR	X3936A0 SN74LVU04APWR	X3936A0 SN74LVU04APWR	X3936A0 SN74LVU04APWR	X3936A0 SN74LVU04APWR	X3936A0 SN74LVU04APWR	X3936A0 SN74LVU04APWR
s94	R213	x	RD35647 4.7K	RD35647 4.7K	RD35647 4.7K	RD35647 4.7K	RD35647 4.7K	RD35647 4.7K	RD35647 4.7K
s95	R214	x	RD35718 18K	RD35718 18K	RD35718 18K	RD35718 18K	RD35718 18K	RD35718 18K	RD35718 18K
s96	L208	x	WG53720 PZ2012U600-3ROT	WG53720 PZ2012U600-3ROT	WG53720 PZ2012U600-3ROT	WG53720 PZ2012U600-3ROT	WG53720 PZ2012U600-3ROT	WG53720 PZ2012U600-3ROT	WG53720 PZ2012U600-3ROT
s97	R220	x	RD35510 100	RD35510 100	RD35510 100	RD35510 100	RD35510 100	RD35510 100	RD35510 100
s98	J215 J216 J214 J217	x	RD35000 0	RD35000 0	RD35000 0	RD35000 0	RD35000 0	RD35000 0	RD35000 0
s99	J218 J209 J213	RD35000 0	x	x	x	x	x	x	x

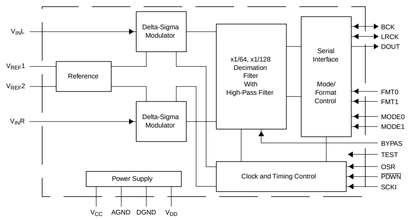
Interchangeable Parts at Manufacture-Stage

Mark	Reference Parts Number	Parts Name
k1	U201	GP1FAV50TKOF TOTX177IFTI
k2	U202-204	GP1FAV50RKOF TORX177IFTI
k3	D1-2-6-10-204-206 208-210	1SS355 MA111 KDS160-RTK/P
k4	Q2	DTC144EKA KRC104S-RTK/P
k5	IC64	MSB1666CH-7 1542S161GCT-7TLTR M12L16161-7TG
k6	IC56	LC89057W-VF4A-E LC89057W-VF4AD-E

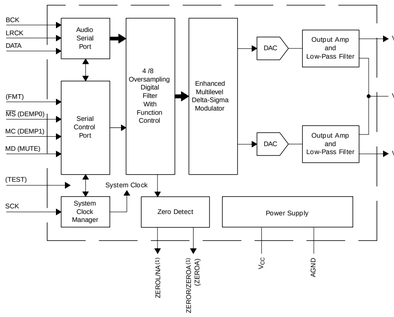
IC71-74, 75, 76 : NJM4565M
Dual operational amplifier



IC70 : PCM1803DBR
Stereo A/D converter

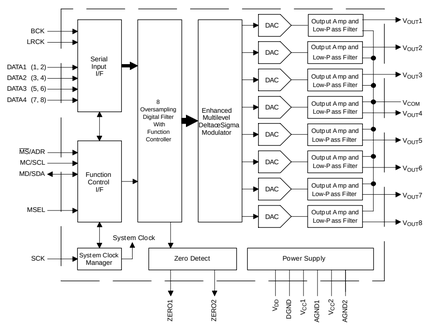


IC69 : PCM1781DBQR
Audio digital-to-analog converter

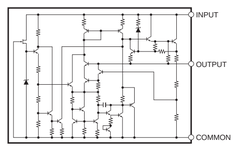


(1) Open-drainoutputforthePCM1782
NOTE: Signal names in parentheses ( ) areforthe PCM1781.

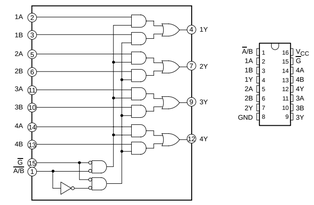
IC68 : PCM1680DBQR
Audio digital-to-analog converter



IC51 : NJM78M05DL1A
Voltage regulator



IC67 : SN74LV157APWR
Quadruple 2-line to 1-line data selectors/multiplexers



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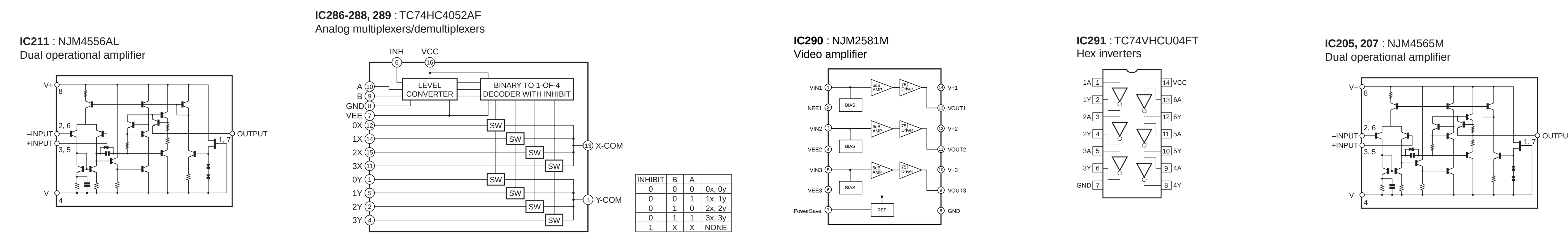
FUNCTION



★ All voltages are measured with a 10MΩ/V DC electronic volt meter.
★ Components having special characteristics are marked ⚠ and must be replaced with parts having specifications equal to those originally installed.
★ Schematic diagram is subject to change without notice.

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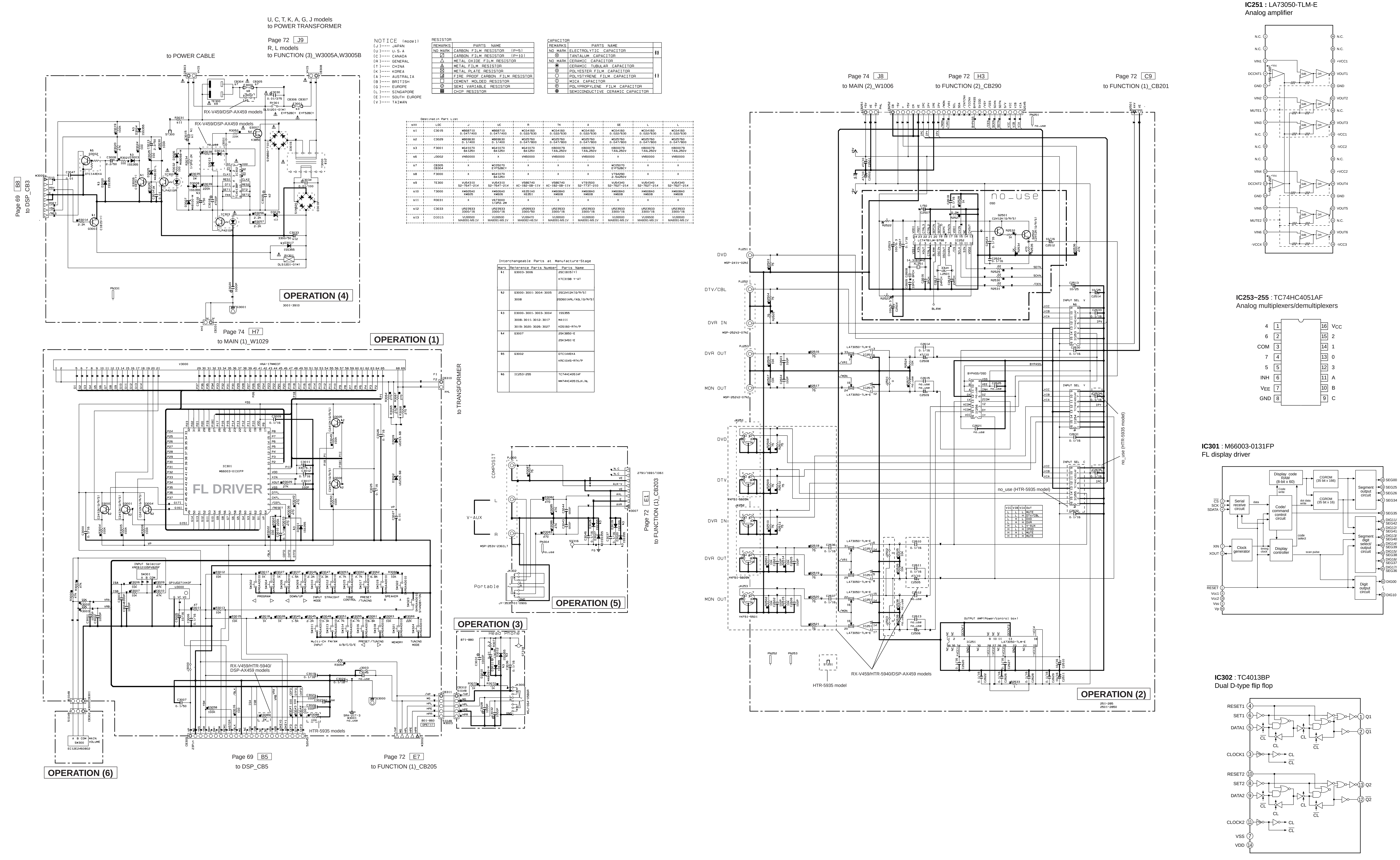
OPERATION



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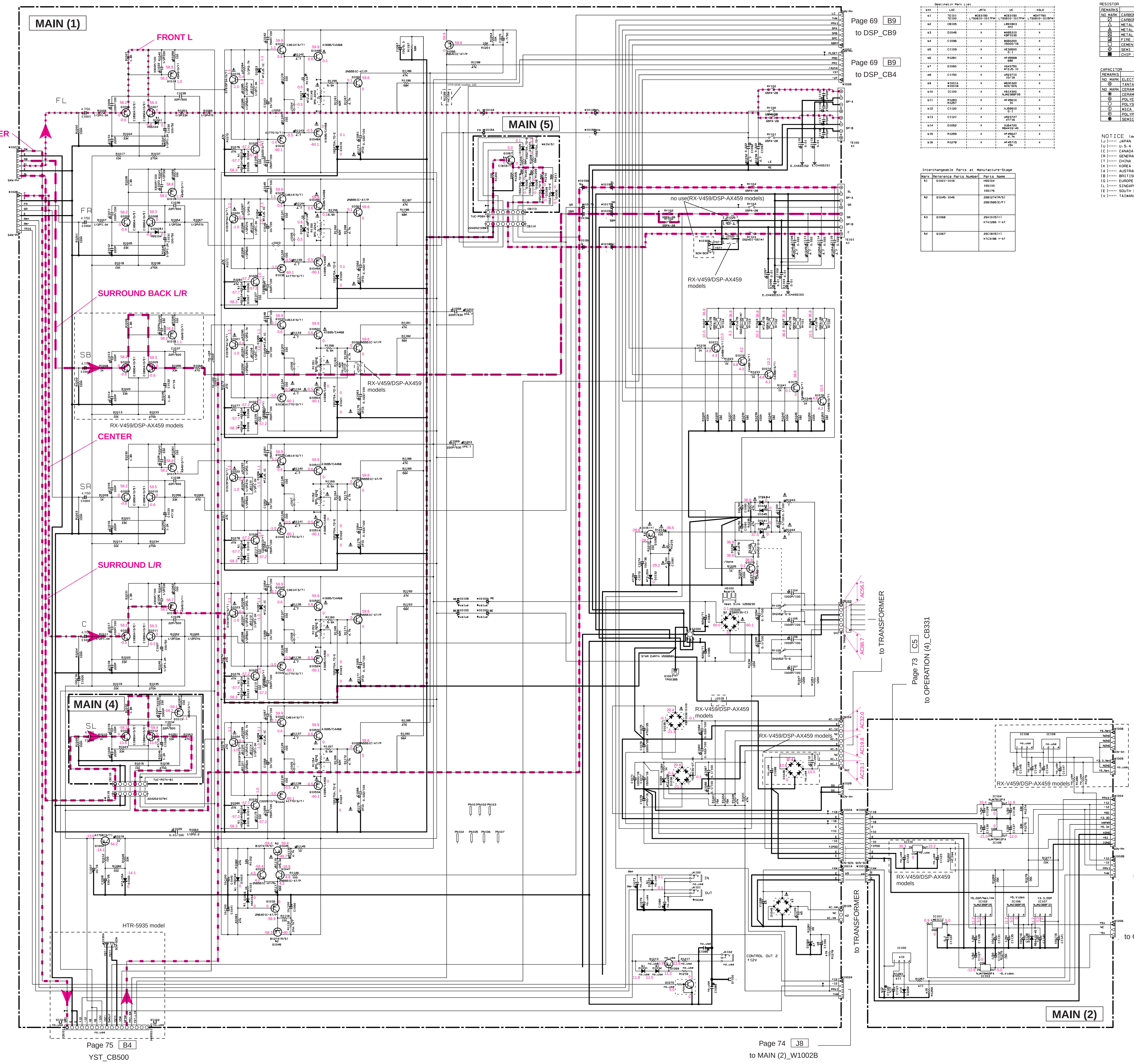
MAIN



Destinatin Part List

sXX	LOC	JRTA	UC	KGLE
s1	TE101 TE100	WC63190 LTS0810-1017FM	WC63190 LTS0810-1017FM	WD47750 LTS0810-1015FM
s2	CB105	x	LB91803 XHI	x
s3	D1046	x	WA65310 KBP103G	x
s4	C1096	x	WG60200 15000/16	x
s5	C1109	x	VE32600 0.1	x
s6	R1281	x	HF45568 680	x
s7	D1060	x	VG43750 MTZJ5.1C	x
s8	C1150	x	UR23710 10/16	x
s9	W1001A W1001B	x	MB30320 SCN-SCN	x
s10	IC100	x	X6143A0 NJM2388F05	x
s11	R1283 R1257	x	HF45610 1K	x
s12	C1120	x	VJ59910 0.1	x
s13	C1121	x	UR23747 47/16	x
s14	D1052	x	VU64720 RB441Q-40	x
s15	R1259	x	HF45647 4.7K	x
s16	R1278	x	HF45715 15K	x

Interchangeable Parts at Manufacture-Stage

Mark	Reference Parts Number	Parts Name
&1	D1001-1016	HSS104 1SS133 1SS176
&2	Q1045, 1046	2SB1274(R/S) 2SB1565(E/F)
&3	Q1068	2SA1015(Y) KTA1266 Y-AT
&4	Q1067	2SC1815(Y) KTC3198 Y-AT

RESISTOR

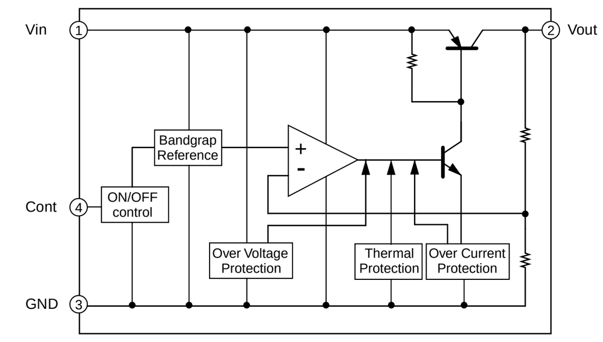
REMARKS	PARTS NAME
NO MARK	CARBON FILM RESISTOR (P=5)
◪	CARBON FILM RESISTOR (P=10)
△	METAL OXIDE FILM RESISTOR
▲	METAL FILM RESISTOR
☒	METAL PLATE RESISTOR
◩	FIRE PROOF CARBON FILM RESISTOR
□	CEMENT MOLDED RESISTOR
⊘	SEMI VARIABLE RESISTOR
■	CHIP RESISTOR

CAPACITOR

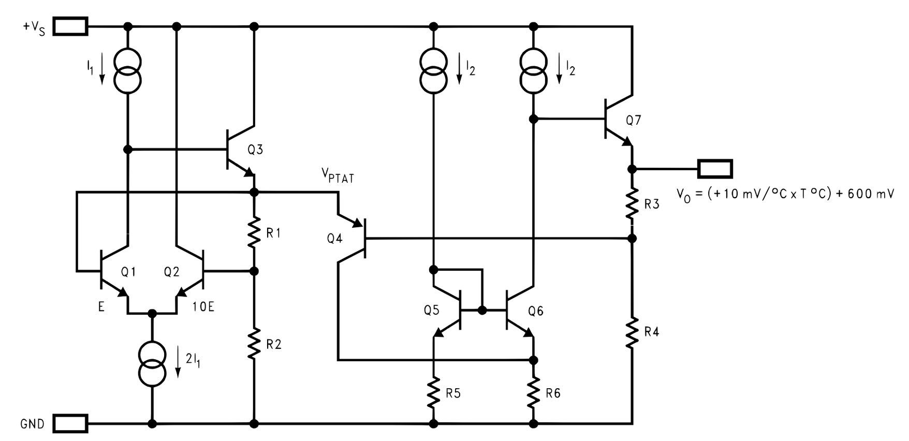
REMARKS	PARTS NAME
NO MARK	ELECTROLYTIC CAPACITOR
⊗	TANTALUM CAPACITOR
NO MARK	CERAMIC CAPACITOR
◉	CERAMIC TUBULAR CAPACITOR
◎	POLYESTER FILM CAPACITOR
○	POLYSTYRENE FILM CAPACITOR
⦶	MICA CAPACITOR
Ⓟ	POLYPROPYLENE FILM CAPACITOR
⊕	SEMICONDUCTIVE CERAMIC CAPACITOR

NOTICE (model)
(J)····· JAPAN
(U)····· U.S.A
(C)····· CANADA
(R)····· GENERAL
(T)····· CHINA
(K)····· KOREA
(A)····· AUSTRALIA
(B)····· BRITISH
(G)····· EUROPE
(L)····· SINGAPORE
(E)····· SOUTH EUROPE
(V)····· TAIWAN

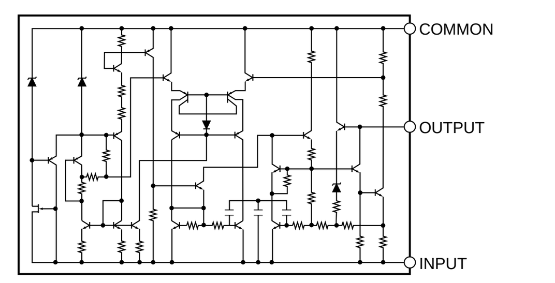
IC100, 102, 106 : NJM2388F
Low dropout voltage regulator with ON/OFF control



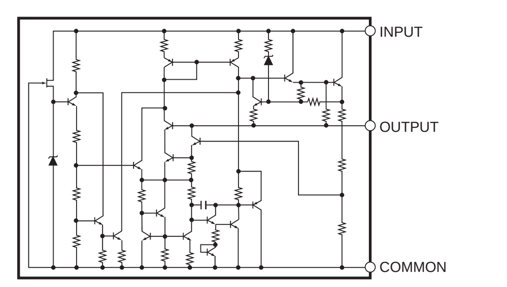
IC101: LM61CIZ
Temperature sensor



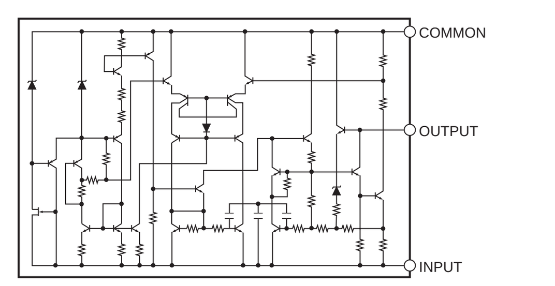
IC103 : NJM79M05FA
Voltage regulator



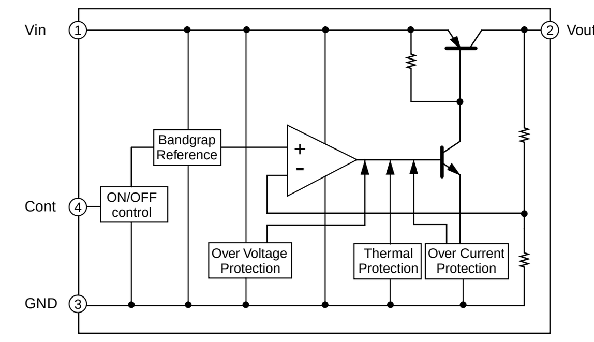
IC104 : NJM7812FA
Voltage regulator



IC105 : NJM79M12FA
Voltage regulator



IC107 : NJM2388F
Low dropout voltage regulator with ON/OFF control



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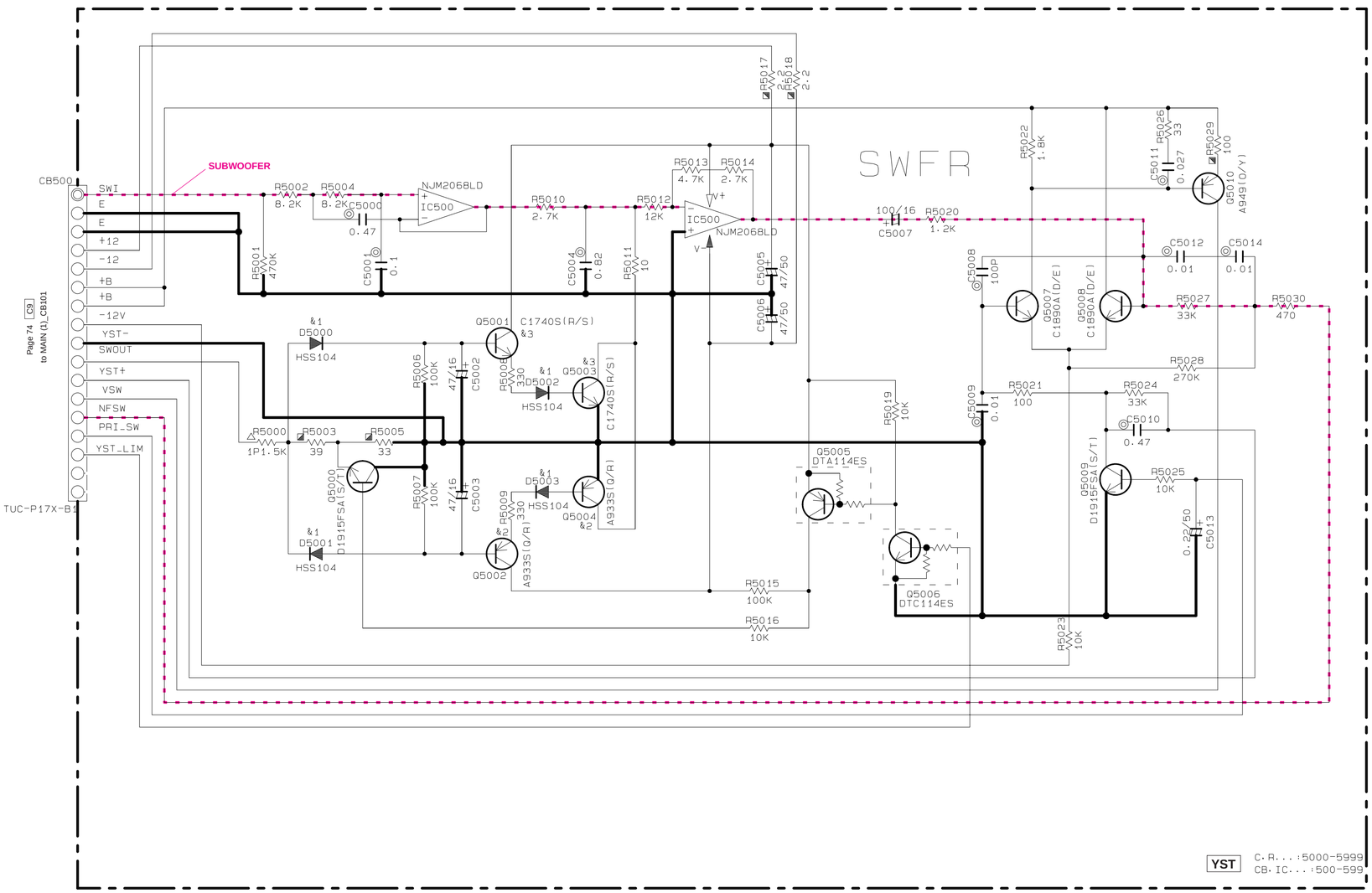
YST **HTR-5935**

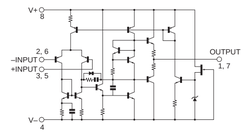


Interchangeable Parts at Manufacture-Stage

Mark	Reference Parts Number	Parts Name
&1	D5000-5003	HSS104 1SS355 1SS176
&2	Q5002.5004	2SA933S[Q/R] 2SA1309A[Q/R/S]
&3	Q5001.5003	2SC1740S[R/S] 2SC3311ARA[Q/R/S]

NOTICE (model)
[J]····· JAPAN
[U]····· U.S.A
[C]····· CANADA
[R]····· GENERAL
[T]····· CHINA
[K]····· KOREA
[A]····· AUSTRALIA
[B]····· BRITISH
[G]····· EUROPE
[L]····· SINGAPORE
[E]····· SOUTH EUROPE
[V]····· TAIWAN

IC500 : NJM2068LD
Dual operational-amplifier



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Service News

Audio

YAMAHA CORPORATION P.O. BOX1, HAMAMATSU, JAPAN

BULLETIN NO. E-1075

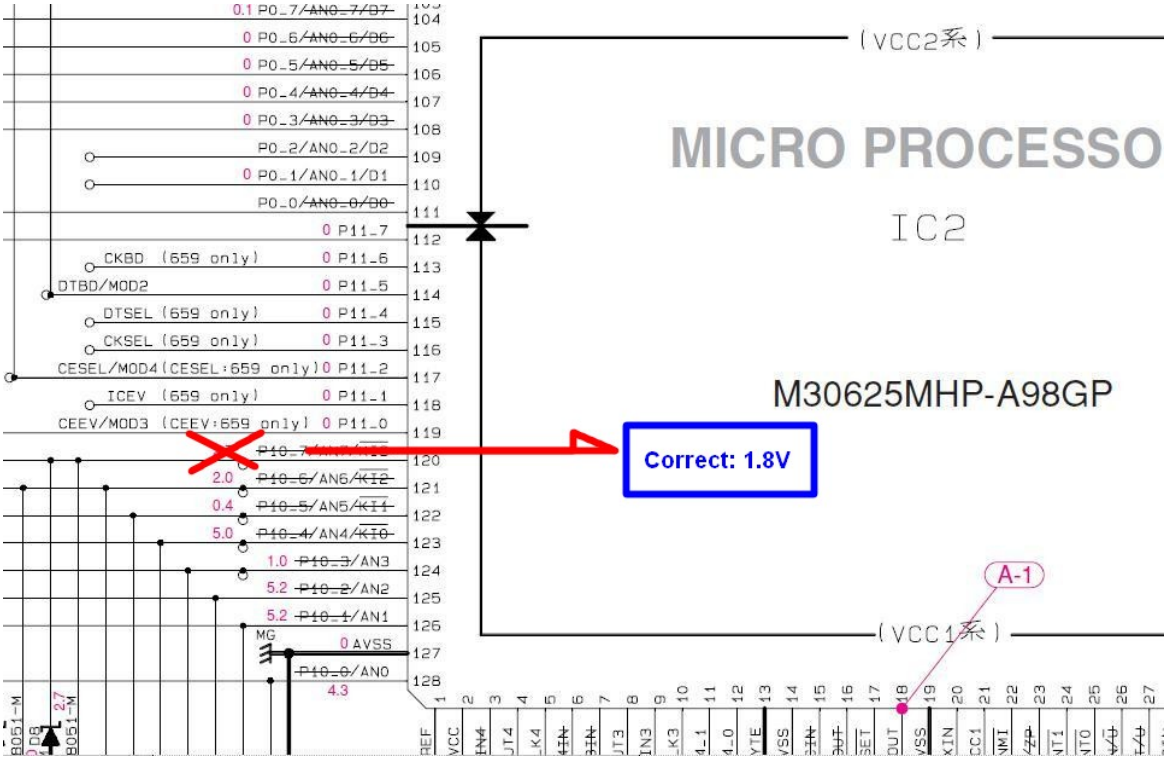
DATE October 2006

RELATED BULLETIN NO.

RX-V459/HTR-5940
HTR-5935

Service Manual Correction

Please make the correction on your Service Manual as follows.



ERROR Page69

Contents: SCHEMATIC DAIGRAMS DSP 1/3

Location: IC2 (MICRO PROCESSOR) Port.120

Error Description: 2.7V

↓

CORRECT

Correct Description: 1.8V