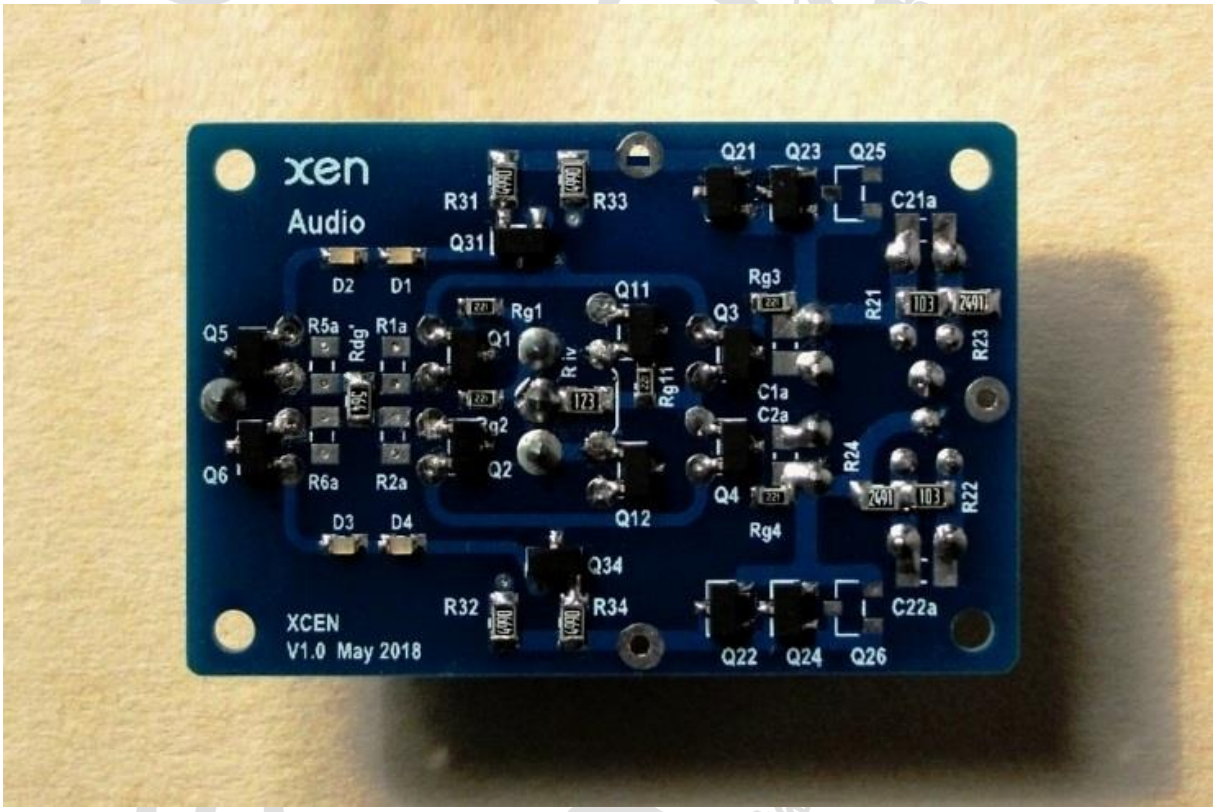
XCEN 2018 Balanced to Single-Ended Converter Revisited

XEN Audio

June 2018



Background

In 2012, we made a serious attempt to build an All-FET balanced to single-ended converter [1]. The AC performance met all expectations, but it suffered from some DC drift issues due to the different tempco of the N-FETs and the P-FETs. And we did not want to use a servo. So it was shelved for a few years.

But recently, the success of the NEXEN prototypes [2] and the Pioneer Super Linear [3] revived our interest in the XCEN circuit. In particular, quite some similarities can be drawn between the phase splitter and the XCEN.

Circuit Revision

Similar to the NEXEN and the Blowtorch, the original XCEN is based on a differential current conveyor followed by a source follower buffer. As in all circuits using a complementary JFET diff pair front end, the circuit is self-biasing and DC stable as long as the JFETs are well matched and thermally coupled. The diff pair in turn is being fed by cascoded current sources from both rails. The key to output DC stability is that both current sources track each other at all times.

In the original XCEN, the CCS were simply resistors cascoded by the 2nd stage MOSFETs, as in the Blowtorch by John Curl. The difference in tempco between the MOSFETs leads to difference in current through those resistors over time, ending up as DC shift in the IV resistors.

In a later revised version, those resistors were replaced by individual JFET CCS's. Although these were also thermally coupled, the difference in tempco between the N- & P-JFETs still contributed to DC offset drifts over time. But recently, in the Pioneer Super Linear headphone amplifier [3], we have successfully implemented self-tracking CCS's from the supply rails with a pair of current mirrors biased by a common JFET CCS. Especially when the current mirrors are well constructed (with thermally couple BJTs with matched hfe), the tracking is excellent, as proven in [3]. In addition, by reducing the diff pair bias to ~1mA per branch, the temperature rise is reduced by a factor of 8, thus further reducing any residual thermal drift.

An important additional benefit with the current mirror is that the AC current swing of both diff pair legs are now summed in the current mirrors. This not only doubles the signal current, allowing the use of a R iv of lower impedance and hence increased bandwidth. More importantly, it fully utilises the even harmonic cancellation of the diff pair, which was not the case in the previous versions.

The use of BJT current mirrors does deviate from an all-FET design, but it is much easier to implement and is also of lower noise than one built from FETs. One can, if so wish, also construct the current mirrors from MOSFETs, at the expense of additional voltage headroom and the need for Vgs matching.

The 2SK246 / 2SJ103 (or 2SK108 / 2SJ106) were chosen for the diff pair for good reasons :

1) They are less of a unobtanium than 2SK170 / 2SJ74.
2) They can be found in Y grade, which allows low bias current to compensate for their low Yfs.
3) Low bias also reduces thermal drift.
4) Importantly, they are less sensitive to Vds (low Early Effect), especially at low current and at Vds above 3V.
5) They have much lower capacitances, thus lower gate-current induced distortion in current conveyor circuits.
6) Their somewhat higher noise is not critical for line level applications at unity gain.

The circuit is very easy on power supply requirements, as the current draw is essentially constant even in the presence of signals.

The final circuit can look something like the schematics below. Although only SMD devices are specified, their TO92 equivalents can be used without any downside whatsoever, though 2SA970 / 2SC2240 might also be difficult to get these days. For lowest DC drift, thermal coupling is important for the current mirrors, the input JFET pair, and the source followers.

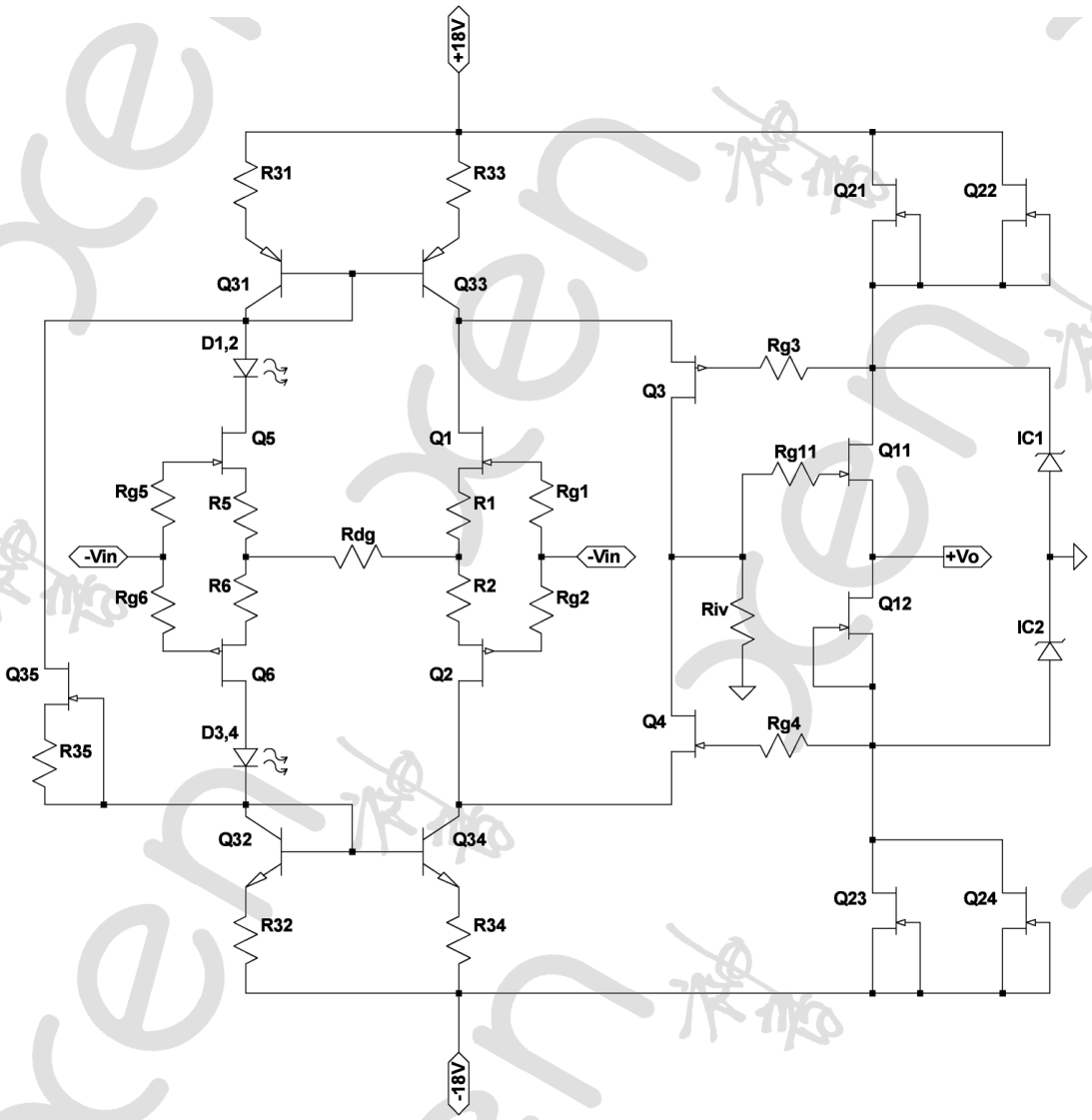
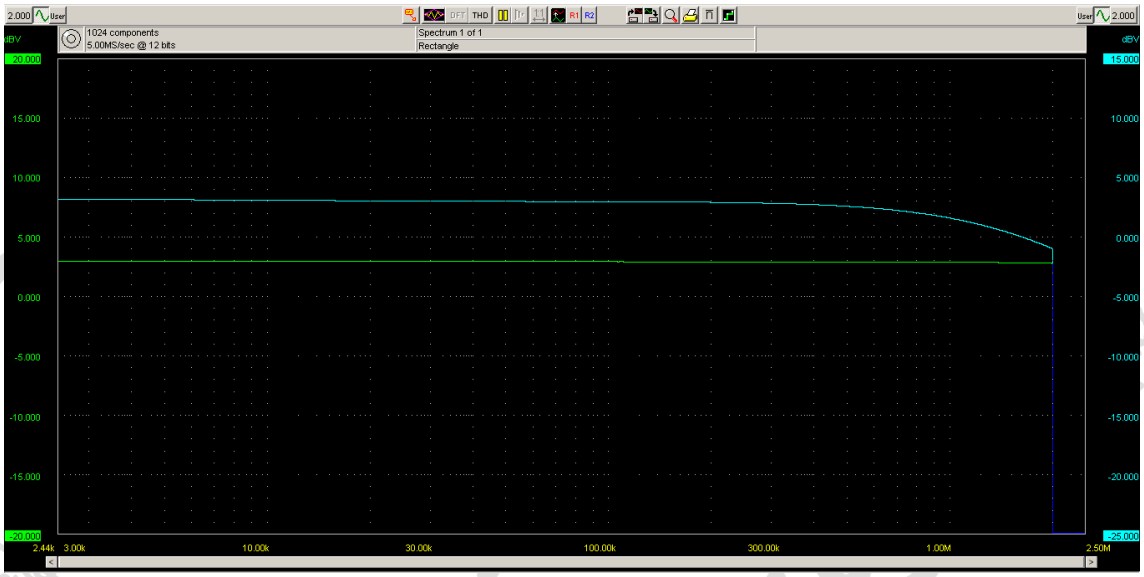


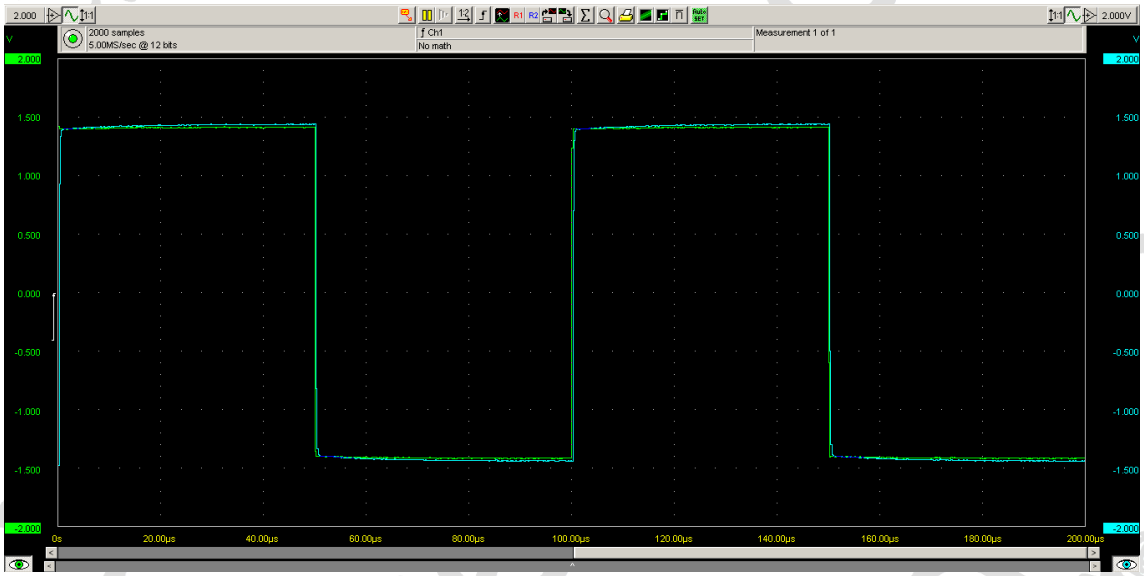
Fig. 1 Schematics of the XCEN 2018 Balanced to Single-Ended Converter

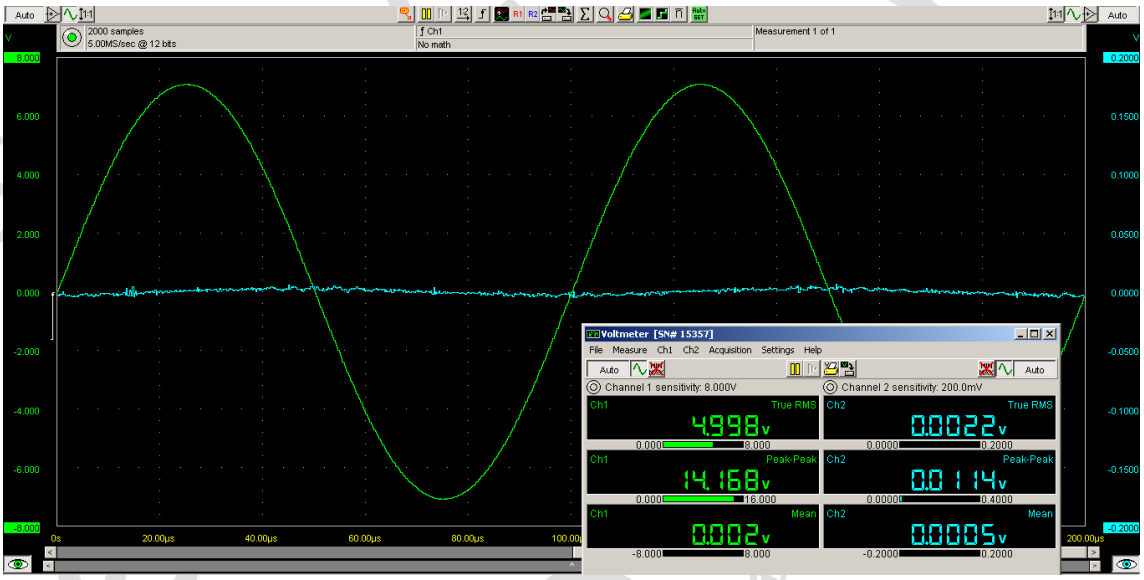
Prototype Measurements

We built a pair of the circuit in full SMD. It is not really essential to thermally couple all the devices, as dissipation is low, in the order of 10~20mW per device. One can, if so wish, mount the PCB against an aluminium plate or heatsink, with flexible thermal pads in between. Without thermal coupling, the DC offset was stable to < +/-2mV over 30 minutes after 2 minutes warm-up.

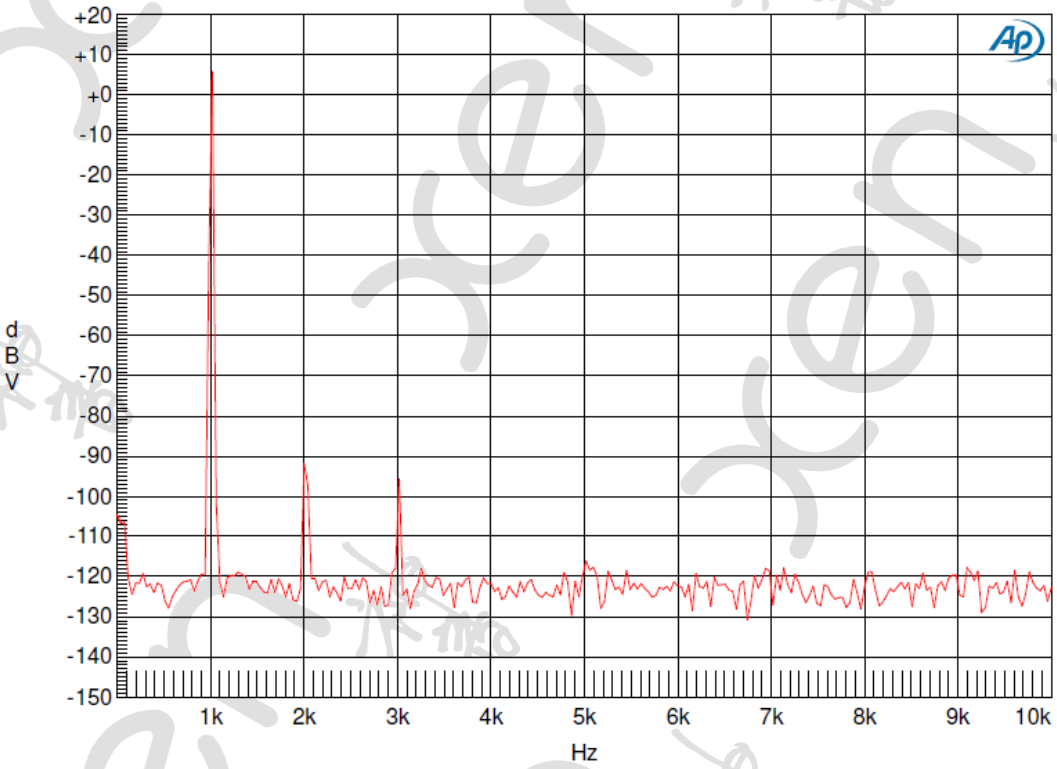
AC gain at 1kHz is 0.996 without trimming. Bandwidth was 1.5MHz at -3dB. 10kHz square waves were copybook perfect. Applying 5Vrms 10kHz sine wave to both inputs, CMRR was measured to be -67dB. And that is only using standard Susumu 0.5% resistors. The matching of the JFETs was excellent.


1024 components
5.00MS/sec @ 12 bits
Spectrum 1 of 1
Rectangle


2000 samples
5.00MS/sec @ 12 bits
Ch1
No math
Measurement 1 of 1


2000 samples
5.00MS/sec @ 12 bits
Ch1
No math
Measurement 1 of 1
Voltmeter [SN# 15357]
File Measure Ch1 Ch2 Acquisition Settings Help
Channel 1 sensitivity: 8.000V
Channel 2 sensitivity: 200.0mV
Ch1 True RMS 4.998v
Ch2 True RMS 0.0022v
Ch1 Peak-Peak 14.168v
Ch2 Peak-Peak 0.0114v
Ch1 Mean 0.002v
Ch2 Mean 0.0005v

Distortion was also measured with an Audio Precision 2722 Analyser. The results were surprisingly good. With 2Vrms 1kHz at the output, 2nd harmonics was at -98dB, 3rd harmonics at -101dB, and the noise floor was around -120dBV.



This concludes nicely a year-long unfinished project at last.

References

1. http://www.diyaudio.com/forums/analog-line-level/216557-xcen-balanced-single-converter.html

2. http://www.diyaudio.com/forums/the-lounge/146693-john-curls-blowtorch-preamplifier-ii-9814.html#post5270193

3. http://www.diyaudio.com/forums/headphone-systems/313163-pioneer-super-linear-circuit.html

Appendix 1 Bill of Materials

Per Channel (+/-18V rails)

Quantity	Designation	Description	Alternative
2	Q1,5	2SK208-Y, matched Idss ~ 2mA	2SK246-Y
2	Q2,6	2SJ106-Y, matched Idss ~ 2mA	2SJ103-Y
1	Q3	2SJ106-Y, Idss > 2mA	2SJ103-Y
1	Q4	2SK208-Y, Idss > 2mA	2SK246-Y
2	Q11 ~ 12	2SK209-GR, matched Idss	2SK117-GR
4	Q21 ~ 24	2SK209-GR, Idss matched to 10%	
2	Q31, 33	2SA1312-BL, matched hfe	
2	Q32, 34	2SC3324-BL, matched hfe	
1	Q35	2SK209-GR, Idss > 2mA	
4	D1,2,3,4	Red LEDs 0603	
2	IC21, 22	TL431 TO-92 On Semi	
2	R1, 5	Susumu 0805 0.5%, trim Q1 to 1mA	
2	R2, 6	Susumu 0805 0.5%, trim Q2 to 1mA	
2	R21, 22	Susumu 0805 10k 0.5%	
2	R23, 24	Susumu 0805 2.49k 0.5%	
4	R31 ~ 34	Susumu 0805 499R 0.5%	
2	R33a, 34a	Susumu 0805 0.5%, trim +Vo DC	
1	R35	Susumu 0805 0.5%, trim Q35 to 1mA	
1	R_dg	Susumu 0805 23.2k 0.5%	
1	R_iv	Susumu 0805 12k 0.5%	
6	Rg1 ~ 6, 11	Susumu 0603 100R 0.5%	
2	C1, 2	Nichicon KA 47µ 25V	
2	C21, 22	Nichicon KA 100µ 16V	
2	C21a, 22a	Panasonic 0805 ECPU 16V 100n	