Using Rectifiers in Voltage Multiplier Circuits

By Joseph M. Beck, Senior Applications Engineer

Systems designs frequently call for a high voltage, low current power source that needs only minimal regulation. A few familiar examples are CRT circuits, electrostatic copiers, and photoflash applications. Required voltages typically range from 10 to 30 kV and the current demand rarely exceeds 5 milliamperes.

When your design requires this type of power source, you may want to consider a voltage multiplier circuit. They are inexpensive, easy to design, versatile, and can provide virtually any output voltage that is an odd or even multiple of the input voltage.

This article explores the basic operation of multiplier circuits and discusses guidelines for electronic component selection. Since General Semiconductor is the industry's leading manufacturer of rectifier products, we will place special emphasis on selecting rectifier diodes for multiplier circuits.

BASIC OPERATING PRINCIPLES

Most voltage multiplier circuits, regardless of their topology, consist chiefly of rectifiers and capacitors. Figure 1. shows three basic multiplier circuits.

The operating principle of all three circuits is essentially the same. Capacitors connected in series are charged and discharged on alternate half-cycles of the supply voltage. Rectifiers and additional capacitors are used to force equal voltage increments across each of these series capacitors. The multiplier circuit's output voltage is simply the sum of these series capacitor voltages.

A wide variety of alternating signal inputs are used with multiplier circuits. The most popular are sine and square wave inputs. For simplicity, this discussion will be limited to sine wave inputs; the calculations become somewhat more involved with asymmetrical signals.

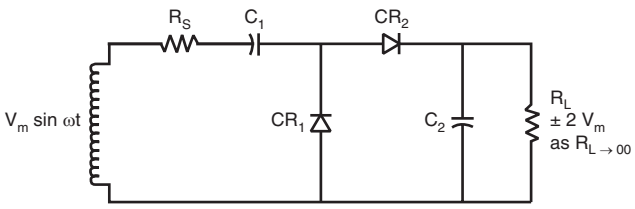

Figure 1A. Basic Multiplier Circuits. Half-Wave Voltage Doubler

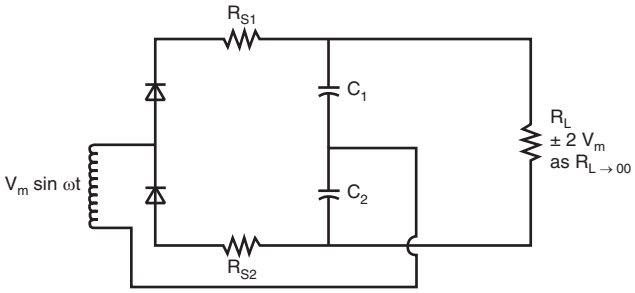

Figure 1B. Basic Multiplier Circuits. Half-Wave Voltage Doubler

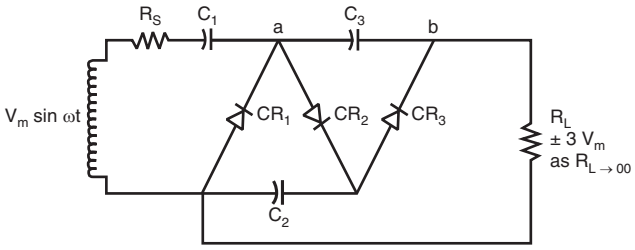

Figure 1C. Basic Multiplier Circuits. Half-Wave Voltage Tripler

Voltage Doublers - Figure 1A. shows a half-wave voltage doubler circuit. It functions as follows. On the negative halfcycle of the input voltage, capacitor C_1 charges, through rectifier CR_1, to a voltage of V_m. On the positive half-cycle, the input voltage, in series with the voltage of C_1 ($V_{C1} = V_m$), charges capacitor C_2 through rectifier CR_2 to the desired output voltage of 2 V_m. Capacitor C_1, which aides in the charging of a capacitor C_2, sees alternating current ("AC Cap") while C_2 sees only direct current ("DC Cap"). In this circuit, the output voltage and the input signal have the same ripple frequency.

The same operating principle extends to the full-wave voltage doubler circuit of figure 1B. On the negative half-cycle of the input voltage, capacitor C_2 is charged through rectifier CR_2 to a voltage of V_m. On the positive half-cycle, capacitor C_1 is also charged to a voltage of V_m, through rectifier CR_1. The series voltages of capacitors C_1 and C_2 ($V_{C1} = V_{C2} = V_m$) yield the desired output voltage: 2 V_m. In this case, capacitors C_1 and C_2 are "DC capacitors"; they see no alternating current. The output ripple frequency of the full-wave doubler is twice that of the input signal.

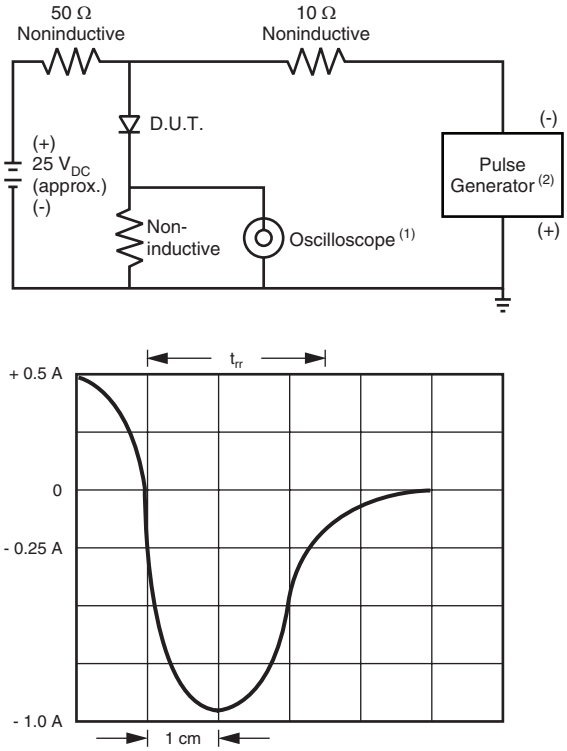

Figure 2. Reverse Recovery Time Characteristic and Test Circuit Diagram

Voltage Tripler - Higher output voltages are possible through the use of a half-wave voltage tripler circuit, shown in figure 1C. This circuit operates as follows. On the negative half-cycle of the input voltage, capacitor C_1 charges through rectifier CR_1 to a voltage of V_m. On the positive half-cycle, the input voltage, in series with the stored voltage on C_1 (V_{C1} = V_m), charges capacitor C_2 through rectifier CR_2 to a voltage of 2 V_m. On the next negative half-cycle, the charge on C_1 is replenished. At the same time, the input voltage, in series with the stored voltage on C_2 (V_{C2} = 2 V_m), charges capacitor C_3 through CR_3 to a voltage of 2 V_m ($V_{C3} = V_b - V_a = (V_m + V_{C2}) - V_{C1}$ = 2 V_m). V_{C1} and V_{C3}, in series, provide the output voltage of 3 V_m. In this case, the output ripple frequency is equal to that of the input signal.

Although half-wave and full-wave multiplier circuits can provide equivalent output voltages, there are some fundamental differences that should be considered. First, the full-wave circuit has the advantage of higher output ripple frequency (twice that of the half-wave circuit). In addition, the full-wave circuit provides better voltage regulation than the half-wave circuit, since the latter relies upon one capacitor (C_1 in figure 1A.) to provide the charging energy to a single DC load capacitor (C_2 in figure 1A.). The full-wave circuit, however, requires that the secondary side of the transformer be capable of withstanding high voltages (approximately 1/2 of the output voltage). For this reason, the half-wave multiplier is usually the preferred circuit when high voltage outputs (V_0 = kV) are required.

DESIGN GUIDELINES

Capacitor selection - The size of capacitors used in multiplier circuits is directly proportional to the frequency of the input signal. Capacitors used in off-line, 60 Hz applications are usually in the range of 1.0 to 200 µF while those used in higher frequency applications, say 10 kHz, are typically in the range of 0.02 to 0.06 µF. In practice, it is usually easier, and less costly, to use the same large capacitance value for all capacitors, both “AC” and “DC” type. The overall capacitive reactance of the circuit must be considered, however, to determine the largest permissible value.

The voltage rating of capacitors is determined solely by the type of multiplier circuit. In the half-wave doubler circuit of figure 1A., C_4 must be capable of withstanding a maximum voltage of V_m, while C_2 must withstand a voltage of 2 V_m. In the full-wave doubler circuit of figure 1B., both C_1 and C_2 must withstand voltages of Vm. The half-wave voltage tripler of figure 1C. requires C_1 to withstand a voltage of V_m, and both C_2 and C_3 to withstand voltages of 2 V_m. A good rule of thumb is to select capacitors whose voltage rating is approximately twice that of the actual peak applied voltage. For example, a capacitor which will see a peak voltage of 2 V_m should have a voltage rating of approximately 4 V_m.

RECTIFIER DIODE SELECTION

Several basic device parameters should be considered:

Repetitive Peak Reverse Voltage (V_{RRM}) - Repetitive peak reverse voltage is the maximum allowable instantaneous value of reverse voltage across the rectifier diode. Applied reverse voltages below this maximum value will produce only negligible leakage currents through the device.Voltages in excess of this maximum value, however, can cause circuit malfunction - and even permanent component damage - because significant reverse currents will flow through the device. For example, Vishay General Semiconductor’s GP02-40 rectifier diode has a peak reverse voltage rating (V_{RRM}) of 4000 V, maximum. Applied reverse voltages of 4 kV or less will produce a maximum reverse leakage current, I_R, of 5 µA through the device when operated at room temperature (25 °C). In most cases, this leakage current is considered negligible, and the device is said to be completely blocking (I_R = 0).

In the case of the three circuits of figure 1., the maximum reverse voltage seen by each rectifier diode is 2 V_m. So devices must be selected with reverse voltage (V_{RRM}) ratings of at least 2 V_m.

Reverse Recovery Time (t_{rr}) - In general terms, reverse recovery time is a measure of the time needed for a rectifier diode to reach a state of complete blocking (I_R = 0) upon the application of a reverse bias. Ideally, this time should be zero. In reality, however, there’s a finite period of time in which a stored charge at the diode junction must be “swept away” before the device can enter its blocking mode. This stored charge is directly related to the amount of forward current flowing through the device just prior to the application

of the reverse bias.Fortunately, since operating currents are very low in multiplier circuits, reverse recovery times are kept to a minimum. Nevertheless, t_{rr} plays an important role in multiplier design.

When selecting rectifier diodes, the frequency of the input signal to the multiplier network must be considered. For symmetrical signal inputs, the device chosen must be capable of switching at speeds faster than the rise and fall times of the input. If the reverse recovery time of the rectifier is too long, the efficiency and regulation of the circuit will suffer. In the worst case, insufficient recovery speeds will result in excessive device heating, as reverse power losses in the rectifier become significant. Continued operation in this mode usually results in permanent damage to the device.

The reverse recover time (t_{rr}) specification is very dependent upon the circuit and the conditions being used to make the measurement.Several industry standard t_{rr} test circuits exist (Figure 2. is the test circuit used for the GP02-40).Therefore, it's very important to note which test circuit is being referenced, as the same device may measure differently on different test circuits. Furthermore, the t_{rr} specification should be used for qualitative, not quantitative purposes, since conditions specified for t_{rr} measurement rarely reflect those found in actual real life circuit operation. The t_{rr} specification is most valuable when comparing two or more devices that are measured on the same circuit, under the same conditions.

Figure 3. shows the relationship between forward current and t_{rr} in the GPO2-40. As you can see, decreasing current flow in the multiplier circuit makes it possible to use higher input frequencies. An increase in current flow has the opposite effect. Ideally, the multiplier network load should draw no current.

Peak forward Surge Current (I_{FSM}) - A peak forward surge current rating is given for most rectifier diodes. Most often, this rating corresponds to the maximum peak value of a single half- sine wave (50 or 60 Hz) which, when superimposed upon the devices rated load current (JEDEC method), can be conducted, without damage by the rectifier. This rating becomes important when considering the large capacitance associated with multiplier circuitry.

Surge currents can develop in multiplier circuits, due to capacitive loading effects. The large step-up turns ratio between primary and secondary of most high voltage transformers causes the first multiplier capacitor (C_1, secondary side) to be reflected as a much larger capacitance into the primary.For example, a transformer with a turns ratio of 25 will cause a 1.0 µF capacitance to be reflected into the primary circuitry as a capacitance of (1.0)(25) µF, or 625 µF. At circuit turn-on, large currents will be developed in the primary side as this effective capacitance begins charging.

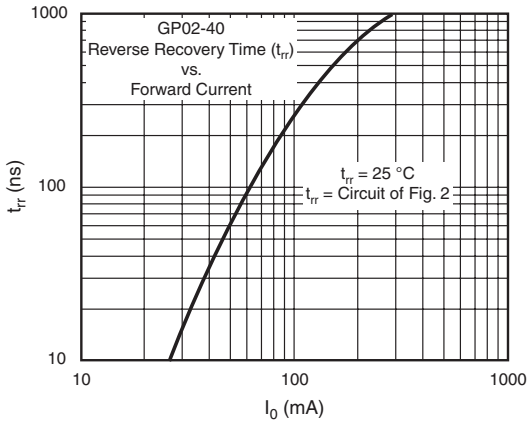

Figure 3. t_{rr} as a Function of Forward Current

On the secondary side, significant surge currents can flow through the rectifiers during initial capacitor charging at turn-on. The addition of a series resistance (R_S in figure 1.) can greatly reduce these current surges, as well as those in the primary circuitry. For example, the GPO2-40 has a forward surge rating, I_{FSM}, of 15 A. Considering a maximum secondary voltage of 260 V_{RMS}, 60 Hz, the calculation of R_S is as follows:

$$R_S \geq V_{peak}/I_{FSM} \qquad eq.1$$
$$R_S \geq (1.41)(260)/15$$
$$R_S \geq 24.4\ \Omega$$

Other Parameters - Of lesser significance are the forward current rating, I_0, and maximum forward voltage, V_F.

Forward current, I_0 - As stated earlier, in the ideal multiplier configuration the load will draw no current. Ideally, the only significant current flow through the rectifiers occurs during capacitor charging. Therefore, devices with very low current ratings (hundreds of milliamperes) can be used. It must be noted, however, that the forward current and forward surge current ratings are related, since both are a function of silicon die area. Generally speaking, devices with a high surge current rating, I_{FSM}, will also have a high forward current, I_0, rating, and vice versa.

Forward Voltage, V_F - In practice, the forward voltage drop, V_F, of the rectifiers does not have a significant effect on the multiplier networkfs overall efficiency. For instance, the GP02-40 has a typical forward drop of 2.0 V when measured at a current of 100 mA. A half-wave doubler with an 8 kV output will have less than 0.05 % (2 x 2 V/8 kV) loss in efficiency due to the forward voltage drops.

HIGHER ORDER CASCADE MULTIPLIER

Still higher voltages are possible by using the cascade multiplier circuit shown in figure 4. The output voltage is calculated as:

$$V_0 = (n)(V_m), \text{ as } I_L - 0 \qquad eq.2$$

where n = number of capacitors, or diodes, assuming equal value capacitors, ideal diodes and symmetrical signal input.

In theory, one can obtain any incremental output voltage increasing the value of n. In practice, however, voltage regulation and efficiency become increasingly poor as n increases. The potential for voltage arcing must also be considered as the value of n increases, and when higher output voltages are required. Careful mechanical design can minimize arcing, to a large extent.

From a pure circuits standpoint, voltage multipliers are relatively easy to design.The selection of circuit components, however, is one facet of the “overall design” that should not be taken for granted or trivialized. Careful consideration of all component parameters is the only way to ensure both reliable and predictable circuit performance. Put another way, ideal circuits require ideal circuit components.

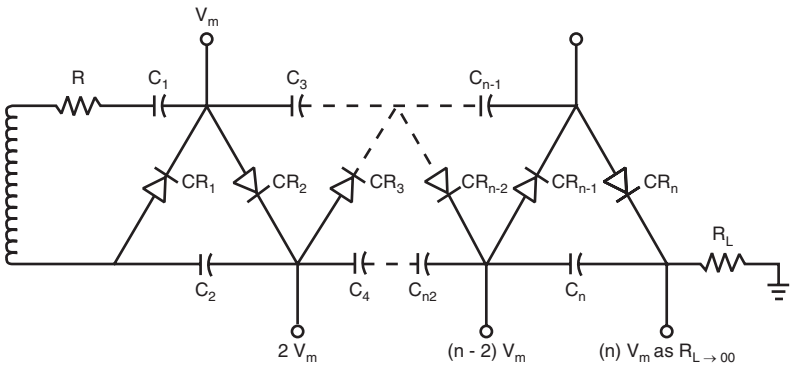

Figure 4. Cascade Multiplier