

11.3 Power MOSFET model (VDMOS)

The VDMOS model is a relatively simple power MOS model with 3 terminals drain, gate and source. Its current equations are partly based on a modified MOS1 model. The gate-source capacitance is set to a constant value by parameter Cgs. The drain-source capacitance is evaluated from parameters Cgdmax, Cgdmin, and A. The drain-source capacitance is that of a parallel pn diode and calculated by Cjo, fc, and m. Leakage and breakdown are modeled by the parallel pn diodes as well, using is and other parameters. A subthreshold current model is available, using a single parameter ksubthres. Quasi-saturation is modelled with parameters rq and vq. Mtriode may be used here as well.

The thermal network of the VDMOS model is shown in Fig. 11.1.

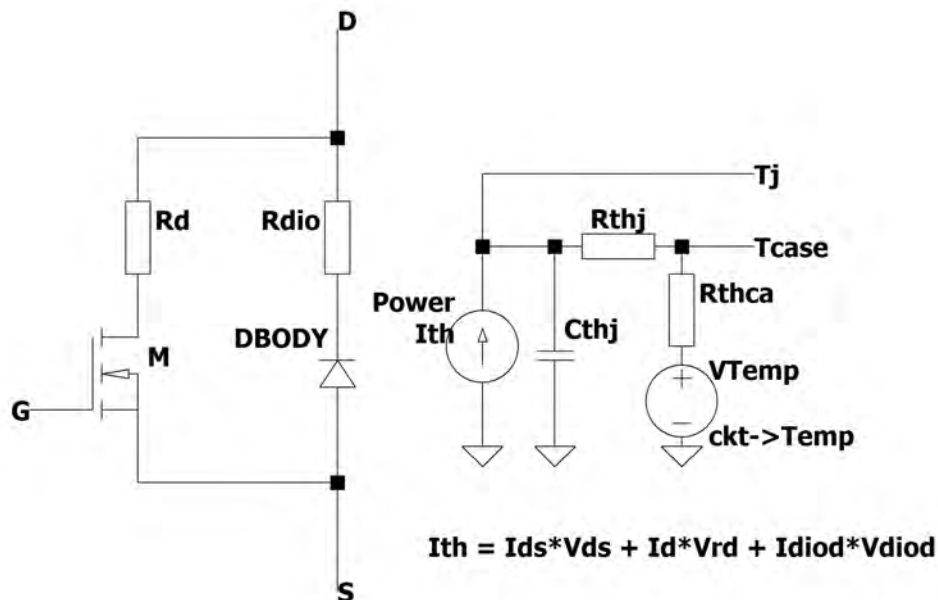


Figure 11.1: VDMOS model including thermal network

This model does not have a level parameter. It is invoked by the VDMOS token preceding the parameters on the .model line. P-channel or n-channel are selected by the model parameter CHAN and NANCHANG. If no flag is given, n-channel is the default. Standard MOS instance parameters W and L are not acknowledged because they are no design parameters and are not provided by the device manufacturers.

The following 'parameters' in the .model line are no model parameters, but serve information purposes for the user: mfg=..., Vds=..., Ron=..., and Qg=... They are ignored by ngspice.

General form:

```

MXXXXXXX nd ng ns mname <m=val> <temp=t> <dtemp=t>
.model mname VDMOS <Pchan> <parameters>

```

Example:

```

M1 24 2 0 IXTH48P20P
.MODEL IXTH48P20P VDMOS Pchan Vds=200 VTO=-4 KP=10 Lambda=5m
+ Mtriode=0.3 Ksubthres=120m Rs=10m Rd=20m Rds=200e6
+ Cgdmax=6000p Cgdmin=100p A=0.25 Cgs=5000p Cjo=9000p
+ Is=2e-6 Rb=20m BV=200 IBV=250e-6 NBV=4 TT=260e-9

```

VDMOS instance parameters

Name	Parameter	Units	Default	Example
m	device multiplier	-	1	-
off	Device initially off	-	0	
icvds	Initial D-S voltage	V	0.0	
icvgs	Initial G-S voltage	V	0.0	
temp	device temperature	°C	27	100
dtemp	device temperature difference	°C	0.0	50
ic	Vector of D-S, G-S voltages	V	0.0	
thermal	Thermal model switch on/off	-	-	

VDMOS model parameters

Name	Parameter	Units	Default	Example
VDMOS	select VDMOS model	-	must given	-
NCHAN	nch type transistor	-	default, if not given	-
PCHAN	pch type transistor	-	required, if PMOS	-
VTO	Zero-bias threshold voltage (V_{T0})	V	0.0	4
KP	Transconductance parameter	A/V ²	1.0	5.9
PHI	Surface potential	V		
LAMBDA	Channel length modulation (λ)	1/V	0.0	0.001
THETA	Vgs influence on mobility	1/V	0.0	0.015
RD	Drain ohmic resistance	Ω	1e-3	61m
RS	Source ohmic resistance	Ω	1e-3	18m
RG	Gate ohmic resistance	Ω	1e-3	3
KF	Flicker noise coefficient	-	0.0	

Name	Parameter	Units	Default	Example
AF	Flicker noise exponent	-	1.0	
TNOM	Parameter measurement temperature	$^{\circ}C$	27	25
RQ	Quasi saturation resistance fitting parameter	Ω	0.0	0.5
VQ	Quasi saturation voltage fitting parameter	V	1.0e-14	100
MTRIODE	Conductance multiplier in triode region	—	1.0	0.8
SUBSHIFT	shift along gate voltage axis in the dual parameter subthreshold model	V	0.0	
KSUBTHRES	slope in the single parameter subthreshold model	-	0.1	0.27
BV	Vds breakdown voltage	V	∞	
IBV	Current at Vds=bv	A	1.0e-10	
NBV	Vds breakdown emission coefficient	-	1.0	
RDS	Drain-source shunt resistance	Ω	∞	1e7
RB	Body diode ohmic resistance	Ω	0.0	14m
N	Body diode emission coefficient	-	0.0	1.1
TT	Body diode transit time	s	0.0	
EG	Body diode activation energy for temperature effect on IS	eV	1.11	
XTI	Body diode saturation current temperature exponent	-		3
IS	Body diode saturation current	A	1e-14	60p
VJ	Body diode junction potential	V	0.8	
FC	Body diode coefficient for forward-bias depletion capacitance formula	-	0.0	
CJO	Zero-bias body diode junction capacitance	F	0.0	1.5n

Name	Parameter	Units	Default	Example
M	Body diode grading coefficient	-	1.0	0.5
CGDMIN	Minimum non-linear G-D capacitance	F	0.0	10p
CGDMAX	Maximum non-linear G-D capacitance	F	0.0	2.45n
A	Non-linear Cgd capacitance parameter	-	1	0.3
CGS	Gate-source capacitance	F	0.0	1.2n
TCVTH (VTOTC)	Linear Vth0 temperature coefficient	$1/^{\circ}C$	0.0	0.0065
MU (BEX)	Exponent of gain temperature dependency	-	-1.5	-1.27
TEXP0	Drain resistance rd0 temperature exponent	-	1.5	
TEXP1	Drain resistance rd1 temperature exponent	-	0.3	
TRD1	Drain resistance linear temperature coefficient	$1/^{\circ}C$	0.0	
TRD2	Drain resistance quadratic temperature coefficient	$1/(^{\circ}C)^2$	0.0	
TRG1	Gate resistance linear temperature coefficient	$1/^{\circ}C$	0.0	
TRG2	Gate resistance quadratic temperature coefficient	$1/(^{\circ}C)^2$	0.0	
TRS1	Source resistance linear temperature coefficient	$1/^{\circ}C$	0.0	
TRS2	Source resistance quadratic temperature coefficient	$1/(^{\circ}C)^2$	0.0	
TRB1	Body resistance linear temperature coefficient	$1/^{\circ}C$	0.0	
TRB2	Body resistance quadratic temperature coefficient	$1/(^{\circ}C)^2$	0.0	
TKSUBTHRES1	Linear temperature coefficient of ksubthres	$1/^{\circ}C$	0.0	
TKSUBTHRES2	Quadratic temperature coefficient of ksubthres	$1/(^{\circ}C)^2$	0.0	
RTHJC	Thermal resistance junction-case	W/K	1e-3	0.4
CTHJ	Thermal capacitance	J/K	10e-6	5e-3
RTHCA	Thermal resistance case-ambient (w/o heatsink)	W/K	1000	

VDMOS electro-thermal model

Power electronic devices suffer the effect of self-heating effect. That means that the dissipated power has an impact to the electrical behavior of the terminal currents. To minimize this effect and to protect the element from thermal destruction heat sinks are supplied to this kind of power devices.

The ngspice VDMOS model has introduced an electro-thermal approach by stamping additional elements into the circuit matrix and by iteration the additional current control inside the spice solver.

The transistor now has 5 nodes. Besides D, G, and S we have TJ and TCASE. The additional nodes must be activated by the device switch THERMAL. Heat is generated in the MOS channel and peripheral elements like resistors, its temperature is available and may be measured at node TJ, and is fed back internally into the device equations. Within the transistor package the heat is flowing from the channel to the metal surface of the case, at node TCASE. Here you may connect a heat sink, to offer a flow path for the heat away from the device. The internal heat resistance is RTHJC (junction to case), a typical data sheet value. The model also includes the heat capacitance CTHJ of the semiconductor die and package (typically not available in the data sheet, so to be estimated only).

The following example show the usage of ngspice electro-thermal model including a simple heat sink:

General form:

```
MXXXXXXX nd ng ns tj tc mname thermal <m=val> <temp=t> <dtemp=t>
```

Example:

```
M1 24 2 0 tj tc IXTH48P20P thermal
rsc tc 1 0.1
csa 1 0 30m
rsa 1 amb 1.3
VTamb tamb 0 25
.MODEL IXTH48P20P VDMOS Pchan Vds=200 VT0=-4 KP=10 Lambda=5m
+ Mtriode=0.3 Ksubthres=120m Rs=10m Rd=20m Rds=200e6
+ Cgdmax=6000p Cgdmin=100p A=0.25 Cgs=5000p Cjo=9000p
+ Is=2e-6 Rb=20m BV=200 IBV=250e-6 NBV=4 TT=260e-9
+ Rthjc=0.4 Cthj=5e-3
```