Valve DAC: raw DSD version

Marcel van de Gevel, 19 July 2019, updated 21 August 2020

Introduction

The raw DSD version of the valve DAC is a simplified version that basically only consists of the DAC cores, voltage reference and reconstruction filters. The clock and the sigma-delta modulates are supplied externally. Buffering and level shifting of the clock is done with solid-state circuitry.

Hence, the FPGA board is not required, cutting down costs substantially, but the raw DSD version does not entirely meet the requirements of section 1 of the valve DAC article because of the solid-state clock circuitry. The raw DSD version was first built by Ray from Somerset, England.

Main board

In a sigma-delta DAC, any crosstalk from the sigma-delta modulate to the voltage reference or to the clock increases the noise floor. To minimize crosstalk, I designed a multilayer PCB for the valve DAC. The PCB for the raw DSD version is a simplified version of this design. A four-layer board provides two layers of shielding when you use the inner layers as supply and ground planes and put all the digital stuff on the back side and all the analogue stuff on the front. Inner layer 2 is used as a ground plane. Inner layer 1 is a -300 V supply plane below the valve circuitry, on the rest of the board it is a second ground plane. To give more control over the low-frequency (50 and 100 Hz) return currents, there are no planes below the supply section. The complete schematics and the PCB design can be found in the KiCAD archive.

Ideally, everything should be made in surface mount technology to minimize the number of wires sticking out of the wrong side of the board. This seemed inappropriate for the valve circuits, though[1]. As a compromise, I used SMD technology for the data handling digital circuitry, for the solid-state clock circuitry and through-hole components for the rest. Where possible I used relatively large SMD components (like 1206 or 0805 size) to make soldering them a bit easier.

Generally, the through-hole components and the SMD components that handle the clock are on the top side and the SMD components that handle the data on the bottom side. The input connectors are all placed on the top.

The point-to-point wired prototype of the original valve DAC had several problems related to transmission line reflections. Terminating the lines at the source side with roughly the right impedance was enough to solve these issues. The PCB also contains several resistors meant as transmission line terminators, namely R_{29}, R_{30}, R_{33}, R_{34}, R_{37} and R_{38}.

The transmission lines on the four-layer PCB were designed assuming that the dielectric between the outer and inner metal layers is 360 µm thick and has a relative dielectric constant of 4.35, which should more or less match the Eurocircuits PCBProto stack-up. Eurocircuits by default uses two layers of 180 µm thick PR7628 prepreg, while most other PCB manufacturers use only a single prepreg layer. Although the first raw DSD valve DAC boards were manufactured by PCBway rather than Eurocircuits, we kept the prepreg the same

[1] People who have seen the rebuilt Colossus in the National Museum of Computing, block H, Bletchley Park, England, know that Colossus was actually made with surface mounted valve holders so valves could be mounted on both sides of the huge mounting panels. The resistors and capacitors were normal wired components, though.

because double prepreg layers are much less likely to have poor insulation due to voids. Hence, the boards were manufactured to a custom stack-up. The dielectric thickness between the two inner layers is not critical, as long as the dielectric can easily handle 400 V, which it normally can.

The PCB has a top and a bottom legend layer. There is solder mask on both sides, which helps with soldering but also improves insulation.

The boards were designed using the KiCAD open-source PCB design program. One KiCAD feature that I rather like is the fact that schematic components can be associated with different footprints. By assigning a connector footprint or no footprint at all, you can also include off-board components in your schematic if you wish. I have used this trick for the mains transformer.

Regarding the choice of mains transformer, I did most experiments and measurements of the original valve DAC with an old Nordmende transformer (bought at Radio Twenthe in The Hague) that supplied all the required voltages. As it was quite large and made an audible humming sound, I later switched to using two modern toriods, a Noratel AA-53129 (50 VA, 2 times 115 V) for the -300 V supply and a Noratel AA-58023 (50 VA, 2 times 7 V) for the heaters and the +5 V supply.

Theoretically a 30 VA transformer should be sufficient for the high voltage supply, but using a slightly oversized 50 VA transformer brought the filtered supply voltage closer to the desired -300 V and reduced the overshoot you get when the valves have not warmed up yet. As there are many components used that are rated for 400 V, it is essential that the filtered supply voltage never gets more negative than -400 V, not even when the valves are still cold and the mains voltage is 10 % above nominal.

NTC resistor TH_1, an Epcos B57153S0479M0, acts as an inrush current limiter for the heaters. As there is about half a volt of voltage drop across it when heated up, it should only be used if the voltage from the transformer is a bit higher than the nominal 6.3 V, for example because you use a transformer meant for 220 V with 230 V mains or because you use a 7 V instead of a 6.3 V toriod. In fact I had to add an extra 0.1 Ω resistor in the heater circuit to get to the correct voltage with the Noratel AA-58023.

A suitable connector for the connection to the transformer(s) is Würth Elektronik type 691311500006 from the WR-TBL / 311 series, or any other well-insulated 6-pin connector with 5.08 mm pitch. Most of the other connectors of the original valve DAC are shrouded headers with 2.54 mm pitch. I used Amphenol FCI Dubox headers, crimp sockets and socket housings; the sockets and socket housings officially require a special crimping tool, but they are easily mounted without one once you realize that the barb of each contact has to point to the side of the connector.

The inputs for the clock and the sigma-delta modulates (DSD signals) are U.FL coaxial connectors. By placing some 0 Ω resistors, the clock and data inputs can also be connected to a 2.54 mm pitch header that should be compatible with the Amanero Combo 384 USB-interface (header P13). Mind you, the clock signals of the Amanero are placed in between the DSD data lines, which is the worst possible place for crosstalk, so don't place the 0 Ω resistors unless you really need the Amanero interface.

P13 not used: R48, R57, R58 and R59 not mounted
P13 used with the bit clock: R48, R57 and R59 mounted, R58 not mounted

P13 used with the master clock: R48, R57 and R58 mounted, R59 not mounted

Jumpers at P8, P9 and P11:
Using the bit clock or a master clock below 25 MHz: jumper on P8, pins 1 and 2 of P9 shorted, pins 1 and 2 of P11 shorted
Using a master clock between 40 MHz and 50 MHz: no jumper on P8, pins 2 and 3 of P9 shorted, pins 2 and 3 of P11 shorted

When a master clock is used, it has to run at an integer multiple of the bit clock (an even multiple for master clocks between 40 and 50 MHz) and the data have to be stable between 5 ns before and 0 ns after the rising edge of the master clock. When the bit clock is used, the data have to be stable between 5 ns before and 0 ns after the rising edge of the bit clock.

Nothing needs to be mounted at the indicated test points (TP).

Decoupling capacitors C_{10}, C_{19}, C_{23}, C_{30}, C_{44}, C_{45} and C_{52} should be film capacitors with a very low inductance, such as stacked rather than wound capacitors, or wound capacitors that have all windings shorted.

I specified a working voltage of at least 1000 V (DC) for C_{119} and C_{120} because the voltage across them has a large AC component. Large AC voltages are more difficult for the capacitor's insulation than a DC voltage equal to the peak value of the AC voltage, see http://www.wima.de/EN/pulseselection.htm. On top of that, there is only limited filtering between the mains and the voltage across these capacitors and there can sometimes be nasty spikes on the mains. Class X2 capacitors meant for at least 300 V AC would be even better.

Reconstruction filter

C_{28}, C_{29}, C_{50} and C_{51} are part of the reconstruction filter, so their value depends on what reconstruction filter is used. Ray uses a filter as shown in figure 1, except that R_1 and R_4 are lumped into a single 806 Ω resistor and he uses RM cores rather than potcores. For this filter, C_{28}, C_{29}, C_{50} and C_{51} on the main board have to be 15 nF each.

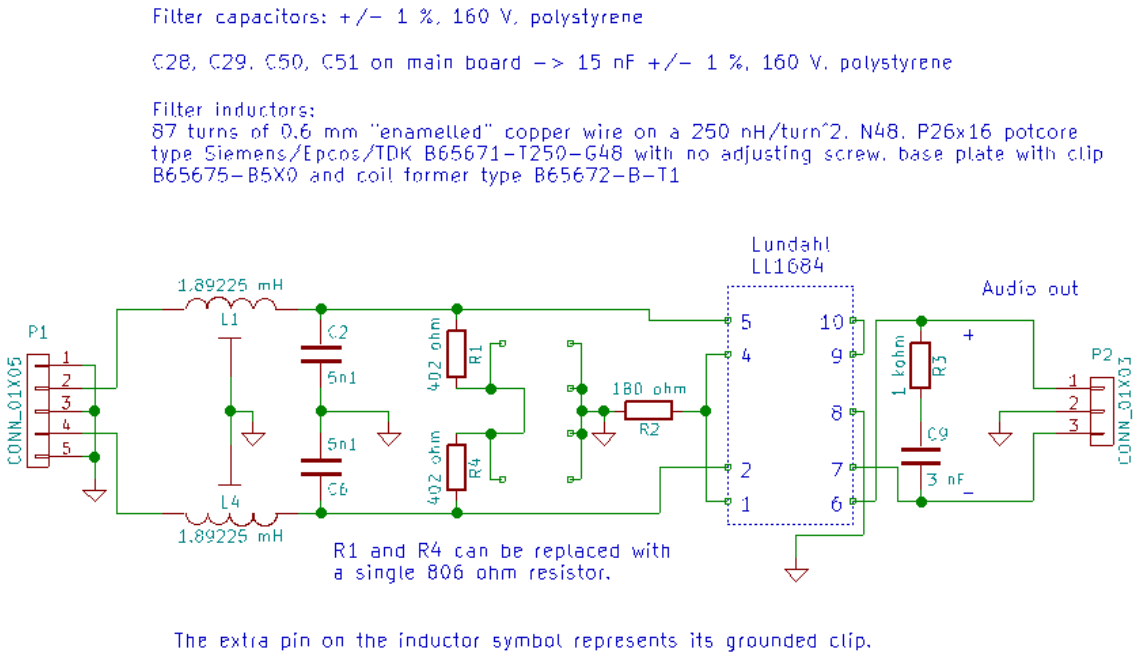

Figure 1: Filter circuit, 43 kHz third-order Butterworth

Build up

It is handy to first solder the SMDs, particularly the fine-pitched ones, before starting with the through-hole components. Once there are through-hole components mounted, the PCB can not be laid flat on a table anymore. Besides, if soldering the fine-pitched SMDs should go wrong and the PCB should become unusable, at least all larger components are salvaged for a new attempt on a new PCB.

Some resistors are best mounted a few millimetres above the surface of the PCB, either because they get quite hot or to improve insulation to a track that passes under them. I did this with R_{86}, R_{100}, R_{128}, R_{131}, R_{132}, R_{136}, R_{139}, R_{140} and R_{141}.

The polystyrene capacitors have the lowest melting point of all the through-hole components, so I mounted them last. These capacitors are both grounded on one side. They usually have a ring indicating which side is connected to the outer foil. This side must preferably be connected to ground, so that the outer foil works as an electrostatic shield.

It is advisable to remove flux residues, particularly from small DC blocking capacitors that handle high voltages, such as C_1, C_2, C_3, C_{26}, C_{33}, their right-channel colleagues C_{20}, C_{21}, C_{22}, C_{48}, C_{55}, and C_4 and C_{15}. With a bit of moisture, flux residues become electrolytic conductors. I usually gently scratch off most of the residue, making sure not to damage the solder mask, and try to remove the remains with a cotton bud soaked in isopropyl alcohol and a dry cotton bud to dry the PCB again. Mind you, some IC type number prints dissolve in isopropyl alcohol. Ray knows a better method.

Valve sockets for PCB mounting are available with many incompatible footprints. Two relatively common types are ceramic noval (B9A) sockets with flat 1.6 mm-wide pins placed on a circle with a diameter of approximately 21 mm, and ceramic sockets with flat 1 mm-wide pins placed on a circle with a diameter of approximately 19 mm. The footprint I drew for the noval valve sockets is more or less compatible with both, as it has pads with a hole of 2 mm placed on a circle with a diameter of 20 mm. The 85A2 requires a miniature (B7G) socket, these often have pins of about 1 mm wide on a circle with a diameter between 16 mm and 19

mm in diameter. The PCB footprint has pads with 2 mm holes placed on a circle with a diameter of 17 mm. As many valve sockets also have a centre pin, the footprints have a 3.5 mm hole in the middle connected to the -300 V plane.

There are many footprint-incompatible variants of the BAS70 diodes used in the DAC core. The variant I've used is a single diode in a SOT-23 package that is simply called BAS70 and not BAS70-04, BAS70-05, BAS70-06, BAS70W, BAS70Z, BAS70J, BAS70K or BAS70-with-cream-on-top.

Availability of the components

Good sources for valves and associated components are Radio Twenthe in The Hague and the NVHR fairs, or similar antique electronics fairs in other countries. Farnell has a good assortment of polystyrene capacitors, and Distrelec is good at potcores. Most of the other components are available from any of the larger electronic component distributors. High capacitance polypropylene capacitors are readily available at loudspeaker DIY shops such as Speaker & Co.

Functional testing

Contrary to the first version of this document and based on Ray's experience with the first raw DSD valve DAC, I now recommend doing the first functional tests with whatever clock and DSD rate you actually want to use, with trimming potmeters RV_1 and RV_2 in the mid position and with RV_3 and RV_4 set to minimum resistance. Make sure the correct 0 Ω resistors and jumpers are placed, as explained earlier in this document.

For debugging if it doesn't work at all, you can resort to using a relatively slow input signal, like DSD128, and using the bit clock rather than the master clock. This minimizes the chances of running into timing problems.

Trimming procedure

In the DAC cores, the trimming potmeters RV_1 (left) and RV_2 (right) that set the balance between the DAC anode resistors must be adjusted for minimum idle-channel noise. This can be done by listening to the noise while playing a DSD signal with silence or with a very soft tone (-80 dB, -90 dB) while adjusting the trimming potmeters, trying to ignore the scratching sounds that occur when you change the wiper position. If the trimming range should be too small, pulling out the E88CC valves and putting them back in in a different order may help.

The data signal to the differential pairs U_{1A}-U_{1B}, U_{2A}-U_{2B} and their right channel equivalents should switch when there is no tail current flowing through them. That means that the clock of the flip-flops U_{4A}, U_{4B} needs to be delayed compared to the clock going to U_{3A}-U_{3B}. The trimming potmeters RV_3 and RV_4 in the clocking section are meant to adjust this delay to whatever value gives the lowest noise floor at high DSD rates (like DSD512). That is, again listen to the noise floor and adjust RV_3 and RV_4 for minimum noise.

Adjustments like this are best done with a headphone and a headphone amplifier with a large gain, but a low maximum output power. This prevents hearing damage if something should go wrong and suddenly produce a very large signal.

Things that may need to be changed experimentally

Based on Ray's experience with the first raw DSD valve DAC, R_{14}, R_{25}, R_{26}, R_{27}, R_{103}, R_{104}, R_{105} and R_{106} have to become 2 kΩ ± 1 %, 0.6 W metal film as otherwise the trimming range can be too small. RV_1 and RV_2 either stay as is (Bourns 3386P-1-502LF) or become Bourns 3296Y-1-502LF, depending on whether one prefers single or multiturn. The same holds for any new builds of the original valve DAC.

The delay lines around U_{12} and U_{13} (clock and data input section) are meant to prevent hold time issues in the flip-flops that drive the E88CCs without causing any set-up time issues. According to my calculations they should do so for all rates up to and including DSD512, but if my calculations are not accurate enough, it could be that you get very loud noise or no signal at all for DSD512 while DSD256 and below work fine. In that case, R_{31}, R_{35}, R_{32} and R_{36} have to be reduced experimentally. Ray has had no such problems.

If the data signals are stable from 5 ns before until 0 ns after the rising edge of the master clock, one could consider using the master clock rather than the bit clock. It then needs to be determined experimentally whether the circuit works best with the bit clock or with the master clock at its clock input; the master clock will probably have less jitter, but also a higher frequency that may aggravate incomplete settling issues. When the bit clock is used, the data signals have to be stable from 5 ns before until 0 ns after the rising edge of the bit clock.

Whenever the bit clock is used, there need to be jumpers between pins 1 and 2 of P_9, pins 1 and 2 of P_{11} and pins 1 and 2 of P_8 in the clocking section. When the master clock is used and when it is always at least twice as high as the bit clock, one can instead place jumpers between pins 2 and 3 of P_9, pins 2 and 3 of P_{11} and remove the jumper from P_8. The master clock then gets divided by two by U_7, which has the advantage that (random) variations of the duty cycle of the master clock have no impact anymore.

According to my calculations, without division by two, the highest DSD rate that is supported is DSD512 (22.5792 Mbit/s or 24.576 Mbit/s) with a 22.5792 MHz or 24.576 MHz clock with a duty cycle between 35 % and 65 %. With division by two, the highest DSD rate that is supported is still DSD512 (22.5792 Mbit/s or 24.576 Mbit/s) with a 45.1584 MHz or 49.152 MHz master clock with a high time of at least 6.5 ns and a low time of at least 8.9 ns (corresponding to a duty cycle between 31.9488 % and 56.25472 % at 49.152 MHz).

In the power supply/muting section, capacitor C_{35} that sets the mute time after power on may have to be increased when you hear loud pops or loud noise after power on. If you hear funny sounds after every format change, C_{16} may have to be increased.