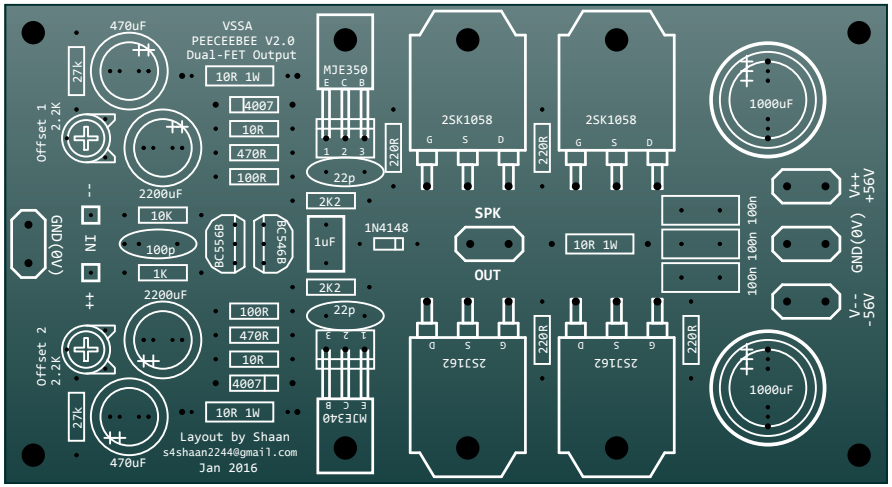
VSSA
PEECEEBEE V2.0
Dual-FET Output
Layout by Shaan
s4shaan2244@gmail.com
Jan 2016
470uF
27k
Offset 1
2.2K
2200uF
10R 1W
4007
10R
470R
100R
10K
100p
1K
IN
GND(0V)
MJE350
E C B
1 2 3
22p
2K2
1uF
1N4148
BC556B
BC546B
220R
2SK1058
G S D
SPK
OUT
1000uF
V++
+56V
GND(0V)
V--
-56V
100n
2SJ162
MJE340