



Square-law class-A:

a family of efficient class-A power amplifiers

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Best in class Class A is generally considered the best way to build a power amp that is inherently linear and free from crossover artefacts. The major drawback is the very high idle dissipation: text books state the theoretical upper limit of efficiency for Class-A is 50% for sine waves. This is a result from the fact that with (assumed) linear law output devices we need to bias the class A amp at half the maximum output current. It's not just the electricity bill; because of the idle dissipation, the amp needs to be build with enough output devices, heat sinks and transformer capacity, to mention just a few factors, for that continuous dissipation.

Square law class A is based on the fact, known from Fourier series analysis, that two symmetrical devices in push-pull cancel all even harmonics. In addition, square-law devices, if they existed, would generate only 2nd harmonic distortion, and thus, in push-pull, their distortion cancels to zero. Using square law devices, we could bias the class A amp at less than half the maximum output current, and still reap all advantages of class A. Lower bias current with the same output power thus gives better efficiency: for sine waves, 66.7% versus 50% in conventional class A. (See: Square-Law class A efficiency analysis).

This new type of Class-A is based on the 'quarter-square' mathematical identity which provides a basis to get linearity from two non-linear devices. Square-law Class-A is a special case of 'Curved Class-A' [1]. In the usual push-pull Class-A, two devices are each approximately linear, but in Curved Class-A they are far from linear and in the special case of Square-law Class-A the two devices' transfer functions are made as close as possible to a square-law so their 2nd order distortion cancels to zero.

The principle is shown in Figure 1, the simpli-

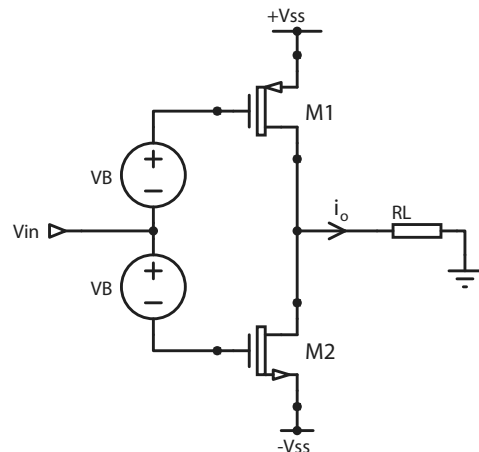


Figure 1: Simplified schematic of a curve linear Class-A output stage [1].

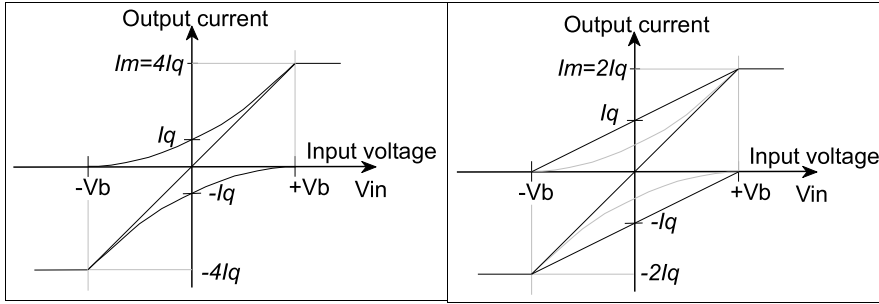


Figure 2: a, left: Square-law Class-A currents with ideal MOSFETs square-law devices; b, right: Linear-law class-A currents with linear output devices.

fied schematic of a curve-linear Class-A output stage [1 Sjöland]. If the devices are matched and of ideal square law characteristic, then this stage will be linear for output currents up to 4 times the quiescent current.

Figure 2a shows that the output current for matched ideal square-law devices is linear between $-V_b$ and $+V_b$. The output current reaches 4 times the quiescent current.

Figure 2b shows the currents in the more usual Class-A where two devices provide essentially linear currents and is called Linear-law Class-A here to distinguish it from Curved-Class-A and Square-law Class-A. The region between $-V_b$ and V_b is Class-A and the square-law currents combine to give a perfectly straight line. In Linear-law Class-A the quiescent current must be set at half the full output current, but in Square-law Class-A the quiescent current is set to one quarter of the full output current. The quiescent current for Square-law Class-A can therefore be half that of conventional Linear-law Class-A. This is the basis for the significantly higher efficiency of square-law class-A over the traditional linear-law class-A.

In Square-law Class-A the currents in the upper and lower MOSFETs can be written as:

$I_{Dp} = \frac{1}{4} I_m \left(1 + V_{in}/V_b \right)^2$ and $I_{Dn} = \frac{1}{4} I_m \left(1 - V_{in}/V_b \right)^2$ respectively. The value of I_m is calculated from $I_m = V_{DD}/R_L$. The limits for V_{in} for Class-A operation are $|V_{in}| < V_b$.

The output current in Square-law Class-A is therefore, $I_{out} = I_{Dp} - I_{Dn} = \left(I_m/V_b \right) V_{in}$ hence the transconductance gain $g_m = I_m/V_b$ Siemens (A/V). Note this is linear – there is no distortion at the output with square-law devices and within the Class-A region.

Most MOSFET audio power amplifier output stages biased for Class-A include source resistors, usually for bias temperature stability or current sharing of parallel devices, and these resistors convert



each MOSFETs square-law-like current relationship into an almost linear one, like those shown in Figure 2b. Even when the external source resistors are omitted, MOSFET currents still deviate significantly from square-law, due to their internal parasitic resistance and the Early effect, both causing “sub-square law” operation [2]. These effects introduce distortion and increase the quiescent current needed for Class-A operation. The tricky bit in practice is obtaining good square-law currents using off the shelf devices that only approximate this mathematical function.

Figure 3 shows the arrangement used to achieve Square-law Class-A. MOSFET T1 and T2 operate in Class-A and although their currents deviate significantly from a square-law at high currents the additional parallel connected MOSFETs T3 and T4 supply extra current to T1 and T2 to make the total currents for each side close to square-law.

This type of distortion reduction technique is similar to that used by Mark van der Heijden [3] for a mobile phone Class-AB MOSFET power amplifier. He subdivided 4 MOSFETs and biased each at slightly different voltages to minimise Class-AB distortion. In a later article the subdivisions were integrated into a composite MOSFET where the threshold voltages were trimmed at manufacture. My circuit uses two stages and is optimised for Square-law Class-A rather than Class-AB.

A practical Square-law Class-A circuit. Figure 4 shows the complete 50 watt MOSFET Square-law Class-A amplifier output stage based on the technique shown in Figure 3. It gives sufficiently low distortion, hum and noise figures for it to be used as a stand-alone amplifier for high quality audio.

The use of lateral MOSFETs allows this simple design to

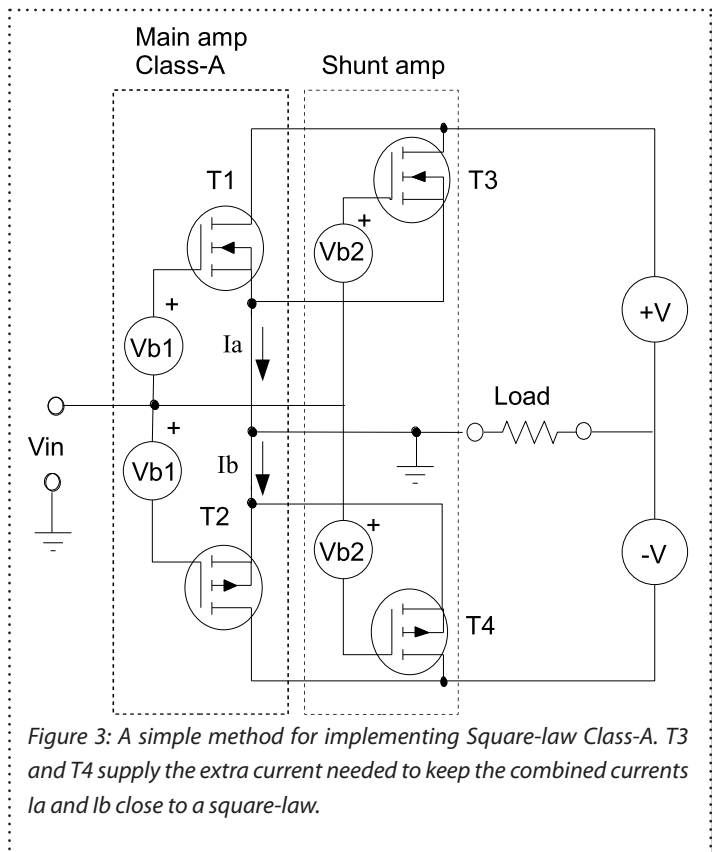
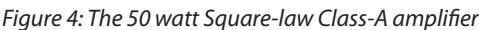


Figure 3: A simple method for implementing Square-law Class-A. T3 and T4 supply the extra current needed to keep the combined currents I_a and I_b close to a square-law.



I used Exicon ECX20N20 and ECX20P20 complementary pair for T1 and T2. The MOSFETs in the shunt stage need a higher gain so I used Hitachi 2SK400/2SJ114 200V 8A pair for T3/T4 respectively. The plastic pair 2SK413/2SJ118 can also be used for T3/4 being lower voltage versions (140V). Calculations for the gain needed for the paralleled MOSFETs are given below.

Circuit description There are 3 main sections in this amplifier: the bias circuit, the power MOSFETs, and the power supply. The paralleled complementary pairs of power MOSFETs



are arranged as common-source amplifiers. Their drain currents pass through each half of the floating power supply, and flow through the speaker load if one side conducts more than the other.

The floating topology is very useful for Square-law Class-A because it introduces voltage gain by the output stage and thus allows a complete power amplifier to be made without the need for an additional gain stage. The floating power supply topology eliminates the need for level shifting driver transistors which introduce undesirable effects such as extra hum, thermal effects, more complexity, more cost and lower reliability. This means that the power supply cannot be shared by the amplifier for another channel, but that need not be a disadvantage given the popularity of “monoblocks”.

In this arrangement spikes on the mains can couple to the speaker via the inter-winding capacitance, typically a few nano farads, but they can be blocked by adding a shield between the windings and grounding it to the amplifier common.

The only change needed to make it a floating supply output stage is to reconnect the load to common on the source side rather than the power supply side for the more usual voltage follower output stage.

The bias circuit is powered from the floating power supply by filtering the output swing using 47k Ω and 10 μ F capacitors. This simplifies the amplifier. If a preamp is needed then the bias circuit could be supplied by the preamp supply such as a ± 9 to ± 15 V and connected to the 10 μ F capacitors.

The filtered DC biases a string of floating LED's to generate a temperature-stable voltage of ± 3 V for T1 and T2, and ± 5 V for T3 and T4. The bias voltage to T3 and T4 needs to be higher than T1 and T2 because the threshold voltage for verticals T3 and T4 is about 3 volts more than lateral MOSFETs T1 and T2.

The resistors supplying the LED's should be 1% to keep the input offset voltage small. Also the LED's should be all the same type and should all be within about ± 5 mV. This prevents a ‘thump’ in the speakers if the input is connected after power-up, or, if the input capacitor is not used then a variable input resistance such as the volume control will not upset the output offset voltage.

The LED voltage is divided down to bias each MOSFET using two 10 turn (or 25T) trimmers. The wiper voltage is bypassed by 1 μ F capacitors so the trimmer resistance does not reduce the bandwidth, since the MOSFET gates present several nF of capacitance and need a source resistance of less than 5k Ω to achieve their full bandwidth of 100kHz. These capacitors can be electrolytic since their voltage drop is minuscule so they cannot introduce any distortion.

The bias voltage for the p-channel MOSFET T2 is increased by about 0.5V by diode D1. The n-channel MOSFET does not require a similar diode. This diode is mounted on T2 for temperature compensa-



tion to equalise the net temperature coefficient of threshold voltage, mainly to improve the output offset voltage to the speaker during warm up. The amplifier therefore does not need a feedback loop to null the DC component to the loudspeaker. It also means there is no “thump” when the amplifier is turned on, provided the volume potentiometer is turned down to prevent other equipment sending their turn on transient to the amplifier. D1 is a b-c junction diode of a BD139 (or BD140) TO-18 transistor under T2’s mounting bolt. Other diodes such as a 1N4148 or transistor such as BC547 could be glued to T2’s top.

A 1M Ω resistor provides a bias current through D1 and a second 1M Ω resistor is used on the n-channel MOSFET side as well to balance the input. The bias supply floats on the input voltage. The 220 Ω and 470 Ω gate resistors prevent parasitic oscillations. They cannot be omitted. They are around 2 to 4 times the minimum value to stop oscillations into a direct connected resistive load. The 10 Ω and 22nF ‘zobel’ series network was not essential for testing with resistive dummy loads, but when I connected a 5m length of standard twin speaker lead the amplifier did oscillate at a high frequency without damage.

LEDs D2 and D3 provide voltage limiting to the MOSFETs which limits the maximum current they can deliver. This limits the peak output current to some 14 amps which can be safely handled by 20 amp dual-die lateral MOSFETs, but note this level of current can only flow if the amplifier is driving a short or an unusually small impedance. Since the speaker line includes a 4 amp fuse the fuse will blow before the MOSFETs junction temperature rises enough to destroy them.

LEDs D2 and D3 give a visual indication when the input voltage clips. If a normal load is connected to the amplifier then the amplifier will clip before the LEDs light. If the LEDs light with a normal load then there must be very severe clipping to the supply rails. The input voltage required to light D2 or D3 is 5.1V peak or 3.5V RMS. The normal maximum input voltage for the start of clipping is 1V RMS without feedback and 2V RMS with 6dB of feedback.

Fast fuses are used in the drains of T3 and T4 to protect them during output shorts. The 4 amp fuse in the speaker line blows after a few seconds of an output short. The extra fuse is added to protect T3 and T4 because of their positive temperature coefficient and their high gain. Normally these MOSFETs only contribute 0.2 amp average with full 50 watts RMS output with a sine wave input. But with a shorted output T3 and T4 carry around half the peak fault current. Therefore a 0.5 amp fuse provides adequate protection for T3 and T4. Poly switches can be used instead of fuses.

The final part is the negative feedback provided by R_{in} and R_f . With a floating supply the live side of the speaker is inverted with respect to the input voltage, so R_f provides shunt voltage feedback. The gain is given very approximately by R_f/R_{in} . This arrangement necessitates a low and constant source impedance of course. If necessary, this can be provided by an (opamp) input buffer or line stage (see below)



Circuit measurements Figure 5 shows measured open loop gains (transconductance or gm) for the Class-A stage T1 and T2 (lower plot), the correction stage T3 and T4 (middle), and the combined gain (top). The output voltage VL is shown with correction and the dotted line allows deviation from linearity to be seen due to the onset of soft clipping. The input voltage is slightly less than that needed for 50W into 8 ohms, giving 25 V peak rather than the full 28 V peak.

Best linearity was obtained when the correction MOSFETs T3 and T4 were biased at approximately 15mA. The bias level for T3 and T4 was not critical for best linearity, as long as the bias was somewhere between 5mA and 30mA (measured after warming up). Between the 5mA and 30mA limits the distortion increased by a factor of only 2 indicating a low sensitivity factor. Under-biasing does not lead to a marked increase in high-order distortion like Class-B. It is best to slightly under-bias at say 10mA once the amp has warmed up.

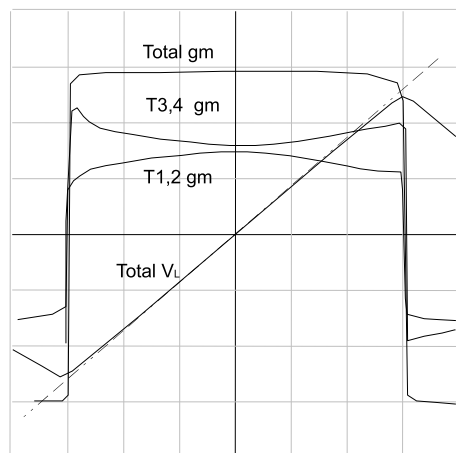


Figure 5: Measured open loop gains for the Class-A stage T1 and T2 (lower) and the shunt stage T3 and T4 (middle) and the combined gain (top). VL is the output voltage, VL = 10 V/div. $I_{q1,2} = 0.92A$, $I_{q3,4} = 35mA$. Y-axis gain approximately 1 S/div, x-axis 0.3V/div using 0.2ms/div.

It may seem strange to designers of Class-A amplifiers that an optimum bias setting is discussed in a Class-A amplifier. But here the optimum bias is for the additional stage to the main Class-A stage and this extra stage is essentially under-biased Class-B. Inspection of the gain curves in Figure 5 does not suggest the generation of any high-order distortion products by the paralleled Class-B stage when correctly set, because it is a mirror image of the Class-A stage which is known to produce only low-order distortion. If you want to experiment with this issue then add a DPST 2A switch or relay in series with the fuses for T3 and T4 to allow a comparison while the amplifier is running.

Figure 6 shows waveforms of the individual currents for the top half of the push-pull circuit (Fig 4). I1 is the current through T1. Ia is the total current for one side. The total current is 3.5A peak and with 0.9A quiescent current it is close to 1/4 or 25% of Ipk for a square-law for 50 watts into 8 ohms. Current Ia at its minimum was measured using a variable DC input voltage and was about 10mA, indicating Class-A operation is occurring over the full 50 watts.

Figure 6 also shows the current in a Linear-law Class-A amplifier as the dotted triangular line. Note

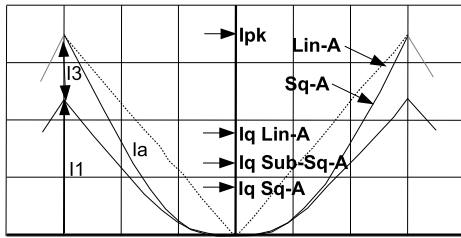


Figure 6: Oscilloscope currents through the top half of the push-pull circuit with the full output swing of 3.5A peak, with 0.9A quiescent current this is close to 1/4 or 25% of I_{pk} for a square-law. At the peak T1 delivers 2.4A while T3 contributes 1.1A.

how Square-law Class-A follows a parabolic curve rather than the straight line of Linear-law Class-A. The quiescent current needed for Linear-law Class-A is 50% of I_{pk} because it needs to midway of a linear current trajectory. A simulation of the Pass Zen V5 [5] Class-A amp gave a linear current plot like this. My Square-law design therefore achieves close to half the bias of Linear-law Class-A amplifiers. Without the shunt stage a quiescent current of 34% of I_{pk} is required, while the circuit with the parallel stage requires 25.7% of I_{pk} . Figure 6 clearly displays the difference between conventional Linear-law Class-A and Square-law Class-A.

The lower bias current for the same output rating immediately gives a practical advantage; in Class-A the heatsink size is determined by the quiescent current and so the Square-law Class-A version using the parallel stage only needs half the heatsink rating of Linear-law Class-A.

Choosing suitable FETs for the shunt stage The gain of the shunt stage can be calculated using the Figure 6 current values. The gain of T3/4 needs to be sufficient to make up the current shortfall at the peaks. The peak gate drive (voltage above V_{th}) for T1 and T2 is $2 \times V_{inpk}$ (from $V_{inpk} + V_{bias}$). For T3 and T4 the peak gate drive is V_{inpk} . Hence the gain parameter for MOSFET T3/4 needs to be approximately 2 squared or 4 times the shortfall ratio ($I_{pk3,4} / I_{pk1,2}$).

Since the shortfall ratio is 1.1A/2.4A or 0.46 times, the ratio $\beta_{3,4} / \beta_{1,2}$ needs to be 4×0.46 or 1.8 times. Since the peak gm of a MOSFETs is roughly proportional to its beta we require MOSFETs with $gm_{3,4} \sim 1.8 gm_{1,2}$.

With T1, T2 being Exicon ECX20N20 and ECX20P20, vertical MOSFETs 2SJ201 & 2SK1530 pair are 12A 200V devices and can provide a slightly higher gain to meet the minimum requirement for this 50W version and are available from RS Components (Part No's 184-925 and 184-931). An IRF620 and IRF9620 200V DMOS FET pair appears suitable for higher voltage designs. I have not tried any other FETs for the shunt stage prior to publication, but hope to check more readily available DMOS FETs soon.

Performance Figure 7 shows the distortion for the amplifier of Figure 4 in open loop (upper curve) and closed loop (6dB nfb; lower curve). With the shunt stage the open loop distortion is reduced by a factor of around 3 with large output swings but has little effect at low power levels. In Class-A dis-



tortion reduces naturally with power so at normal listening levels around the 1 watt level distortion is so low that the shunt stage is not needed – the main purpose for the extra shunt stage is to get the best efficiency in Class-A using square-laws.

You may be wondering why I have not applied distortion weighting to my THD measurements. It is because in Class-A there is no indication of any high order gain variations as seen in Class-B or Class-AB gm plots. So the figures quoted here are expected to correlate well to known distortion threshold values.

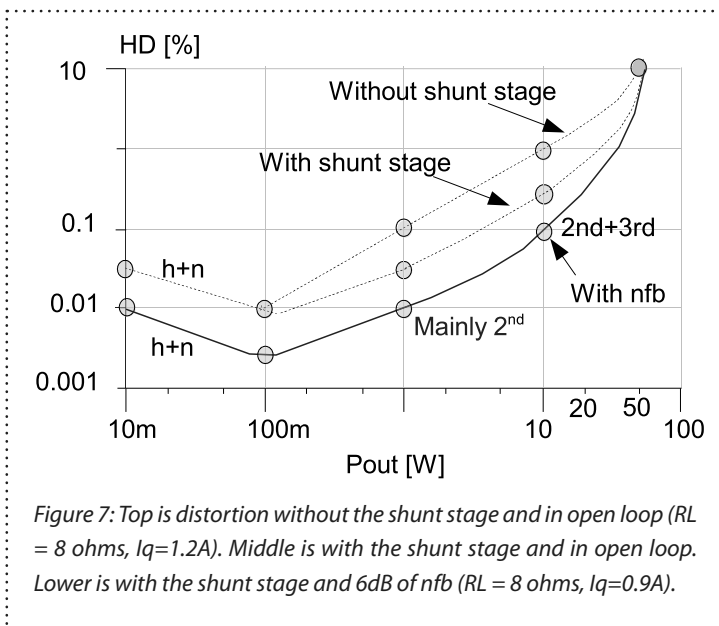
At half-full voltage swing (12W) distortion is reduced from 1% without the shunt stage and in open loop to 0.3% with the shunt stage, then after adding negative feedback to 0.1%.

Louis Fielder [3] showed that at 1 watt (90dB SPL) third harmonic distortion needs to be slightly above 0.1% to be audible. Distortion becomes just audible with the shunt stage and with feedback when a pure tone is used and the output swing is more than 50% or above about 12 watts.

Usually about 1 watt is the average listening power and 50 to 100 watts generally allows sufficient “headroom” for the majority of the peaks in most types of music. So excursions above half of the full voltage swing are so short and infrequent that distortion above 12 watts is unlikely to be audible with music.

This effect can allow the bias to be halved again so operation above 12 watts can be in Class-AB mode, and Class-A below 12 watts. This again allows a significant reduction in the heatsink size by half, to about the same

as Class-B amplifiers designed for continuous sine wave operation. I tried halving the Class-A quiescent current and the sonic effects from Class-AB operation above 12 watts appear to be quite small and therefore a worthwhile way to make the amplifier more compact and/or use less power. A relay could be used to switch between two quiescent currents to allow easy comparisons and this can be done by





using two bias boards (more on this later in the section on scaling options).

Table 1 provides a comparison of the Square-law Class-A amplifier with two other designs that use roughly the same transformer and heatsink ratings. The Curved-A version has no shunt stage and has the quiescent current and the supply voltage increased slightly to give 50 watts output in Class-A.

	Square-law (Fig 2)	Curved-A (no shunt stage)	Pass ZV5	JLH 15W (1996)
Input sensitivity (RMS) 50W/8R	2V	2V	2V†	~1V
Input impedance	~1k//~1.5nF	~1k//~1nF	500R†	47k//220pF
Power output (Class-A into 8R)	50W	50W	15W	15W
Efficiency at 50W	59%	52%	18%†	28% (with reg.)
Peak output current	20A	14A	10A†	-
Open loop gain into 8R	27dB	26dB	35dB†	-
Open loop bandwidth	50kHz	50kHz	20kHz†	-
Power bandwidth	100kHz	100kHz	100kHz	-
CL Load ripple (RMS)	~1mV	~1mV	3mV†	3mV
CL s/n ratio w.r.t. max. Pout	-83dB (80kHz bw)	-83dB (80kHz bw)	-75dB†	-75dB†
Output resistance at 1kHz	6.5R	8R	2R	0.25R
CL Slew rate	100V/us	100V/us	-	40V/us
Harmonic distortion at 1kHz	See Fig. 7	1% @12W	1% @ 15W†	<0.1% @15W
Typical THD at 1W	0.01%	0.02%	0,10%	0,03%
Quiescent current	0.9A	1.2A**	1.5A	1.0A
Supply voltage	±32V*	±34V**	20V	±22V (27V unreg.)
Quiescent power dissipation	60W	77W**	84W (24W reg.)	64W (10W for reg.)
Heatsinks	0.5K/W	0.4K/W	0.36K/W†	2x 0.3K/W
P.S. Capacitors	2x10,000uF	2x10,000uF	6x33mF	2x33mF
Mains transformer	160VA	180VA	~210VA	~180VA
* Shunt version supply voltage rises to ±33V at idle. ** In the version without a shunt stage the idle current falls to 1.1A due to higher dissipation at idle than at full power, so Pq falls from 83W to 77W after 15 minutes on idle. The supply voltage rises to ±35V at idle. † Estimated.				

Table 1: Specifications for several Class-A designs.



Although clipping is not clearly visible in Figure 7, soft clipping occurs when over-driven since very little negative feedback is used. The low damping factor emulates early valve amplifiers when over-driven. Valve amplifiers were both low feedback and Class-A until the Williamson amplifier at the end of the valve era.

Soft clipping allows this amplifier to be driven harder before clipping distortion becomes noticeable compared to most solid-state designs which use lots more negative feedback. Some transistor designs claim to be “zero feedback” but nearly all mean “zero global feedback” since their output stages use voltage followers that typically include 30dB of local negative feedback and therefore all solid state amplifiers hard-clip.

Solid state amplifier power has risen over the years to the hundreds of watts range to provide the headroom needed to reduce the likelihood of hard clipping. Soft-clipping from minimal negative feedback is therefore a very desirable feature in a power amplifier since it allows lower power amplifiers to be used before clipping distortion becomes noticeable. This is particularly useful for Class-A amplifiers because they are presently more expensive per watt than Class-B amplifiers.

Until now it has been unthinkable to operate an output stage with no local feedback and so hard clipping of a solid-state output stage was assumed to be unavoidable. Russell Hamm [6] suggested the main reason for the audible difference between early soft-clip valve amplifiers and modern solid state amplifiers is the very hard-clip of solid state amplifiers, particularly the first stage in the recording chain.

With this soft clip design you can compare it to other hard clip amps of the same rating to see if there is anything in this idea. Use digital recordings since they don't usually include hard clipping. (This is not always the case; CD recordings post-early 90-s often have digitally hard-clipped signals on the disk. CDs issued before the early 90-s (or vinyl) are more likely to be clip-free – ed.).

Effect of amplifier damping on loudspeakers frequency response The only “bad” specification for my amplifier appears to be the high output resistance of 6 ohms. With a high amplifier output resistance the frequency response of any loudspeaker will change slightly, creating additional dips and peaks at certain frequencies. If the new dips and peaks are large enough to be heard then amplifier and speaker comparisons can be upset by this additional effect.

To make this effect negligible amplifier designers provide a high damping factor (DF) of usually more than 20, so any tonal differences when comparing different amplifiers cannot be attributed to differences in output resistance. Damping factor is a concern to commercial amplifier designers to ensure they do not get a bad review from a low damping factor.



Tonal variations in amps due to output resistance, if audible, are similar to the effects from moving furniture or the loudspeaker, or altering the listeners seating position.

But how high does the DF need to be to make the effect undetectable? It firstly depends on how small the frequency response dips and peaks must be to be undetectable during listening. Tests by Sean Olive [7] found that +10dB peaks at 90Hz with moderate Q of 1.8 and -25dB dips were detected by less than half the listeners. This is astonishing; it means the average listener is quite insensitive to frequency response changes. However, in later tests the same researcher [8] found trained listeners could consistently detect changes between 3 to 27 times smaller than untrained listeners.

This suggests that trained listeners can still only detect around $\pm 3\text{dB}$ frequency dips or peaks. If a further safety margin is added then frequency response variation due to a low damping amplifier should not add more than say $\pm 1\text{dB}$ or $\pm 2\text{dB}$ to the loudspeaker response plot.

Figure 8 shows my simulation of the Square-law amplifier driving a JV60 loudspeaker [9] which shows a frequency response deviation of $\pm 1.4\text{dB}$.

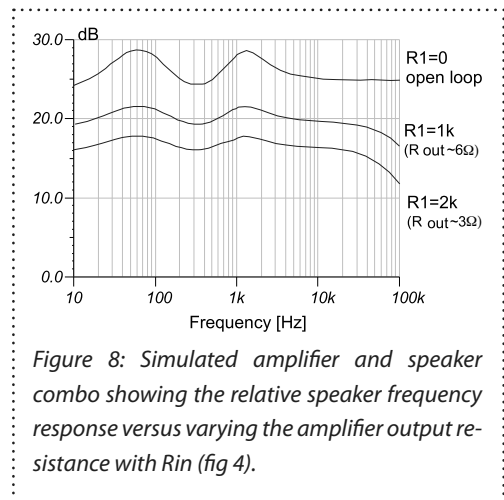
With these speakers it should be possible to swap amplifiers and not worry about the effect of the low damping factor of this amplifier. My speakers' measured impedance peak was 10 ohms at 60Hz and 1.5 kHz and the minimum was 5.4 ohms at 350Hz.

If the tonal difference is not acceptable then you can use one of the options below to make it acceptable.

If you need to reduce the output resistance some options are:

- increase the feedback by raising R_{in} to 2k2 or 4k7 (which will also lower the closed loop gain), or
- precede the output stage with a gain stage such as an opamp to increase the loop gain, or
- convert to a voltage follower (move the speaker common to the other side).

(There are of course other options, such as adding a conjugate network across the speaker, use of a parametric or graphic equaliser somewhere in the chain, or active crossovers combined with voltage or current drive).



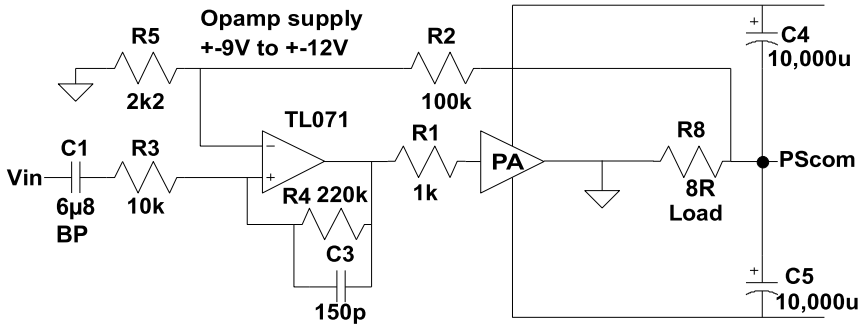


Figure 9. Adding an opamp to increase the loop gain increases speaker damping.

The first option of increasing R_{in} requires a higher drive voltage and this will probably require an additional gain stage as described below.

The second option of adding a gain stage such as an opamp to increase the loop gain was tried using a TL071 and worked well with an opamp gain of 20. Figure 9 shows the additional circuit. The overall gain is now around 40 instead of 10 and 0.5Vrms input provides full output swing into 8 ohms but gives hard clipping. The damping factor is around 10 ($R_{out} \sim 0.8$ ohms). This opamp can drive the relatively high MOSFET gate capacitance when the 1k input resistor R_{in} is retained. Compensation was provided with a 150pF capacitor across the 220k opamp feedback resistor, and the capacitor value was chosen for slight overshoot when driving a 2uF capacitor across an 8 ohm load.

(One way around the problem of global negative feedback from the opamp creating hard clipping is to add a soft clipping circuit immediately prior to the power amplifier such as Robert Cordell's "Klever Klipper" [14] which is an adaptive soft clipping circuit that tracks short term changes in the power supply rail voltage).

The third option requires a reconfiguration from common source to voltage follower and being unity gain requires a high voltage driver stage as the Lin topology or the Hitachi MOSFET topology but this option gives hard clipping. (The voltage follower allows several amplifiers to be run from a common power supply which might also be a factor).

Construction Photo 1 shows a 2 channel 50 watt Square-law Class-A amplifier assembled into a PC tower case. The two heat sinks are offset vertically for natural convection with air entering via the vacant peripheral slots and leaving via the empty power supply bay.

The heatsink used is 300mm long 75mm high and 46mm deep rated at 0.37 K/W (Altronics part H0545). This is higher than the minimum 0.5 K/W since it was intended to operate in a high am-

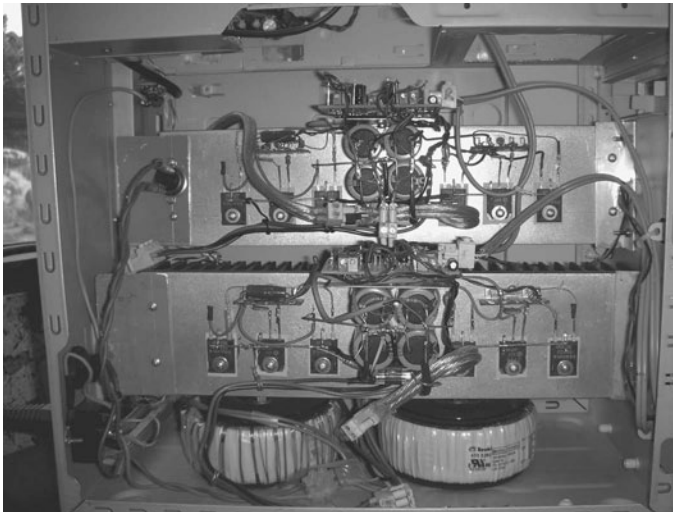


Photo 1: A 50 watt 2-channel Square-law Class-A amp built in Christchurch, New Zealand 2004.

bient temperature of up to 40° C rather than the more standard 25° C. This larger heatsink is also suitable for the version without the shunt stage which runs hotter due to a higher quiescent current. A 80° C or 90° C thermal switch was also mounted on the heatsink and opens the mains circuit if the ambient temperature is too high.

In countries where the ambient temperature rarely exceeds 25° C a

smaller heatsink can be used for the 50 watt Square-law version such as Altronics H0536 (0.55 K/W 200x75x46mm or Jaycar HH8546.

T1 and T2 shown in Figures 3 and 4 are single MOSFETs but in this 50W design they are pairs of ECX10N20 MOSFETs. Two MOSFETs spread the heating more evenly over the heatsink and reduce each thermal washer temperature drop allowing a smaller heatsink. T1 and T2 can be mounted

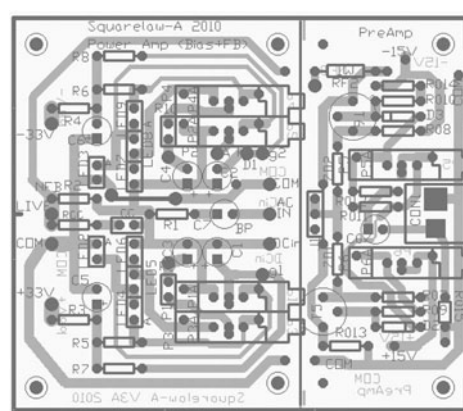
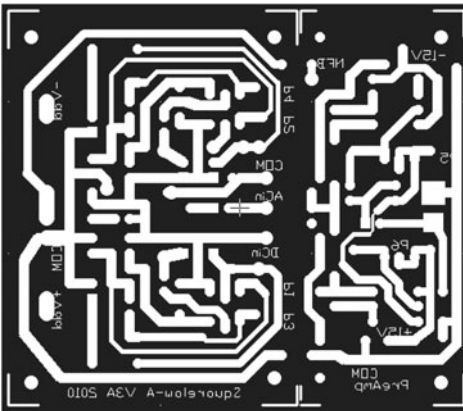


Figure 10 a: bias/preamp circuit PCB layout; b: top view/stuffing guide. (Detailed illustrations are available from the author)

My prototype used 0.9 amp Poly-switches instead of 0.5 amp fuses for T3 and T4. This allows self-resetting following a short lived output short. They were type RDE090A (Farnell 608-889) and con-

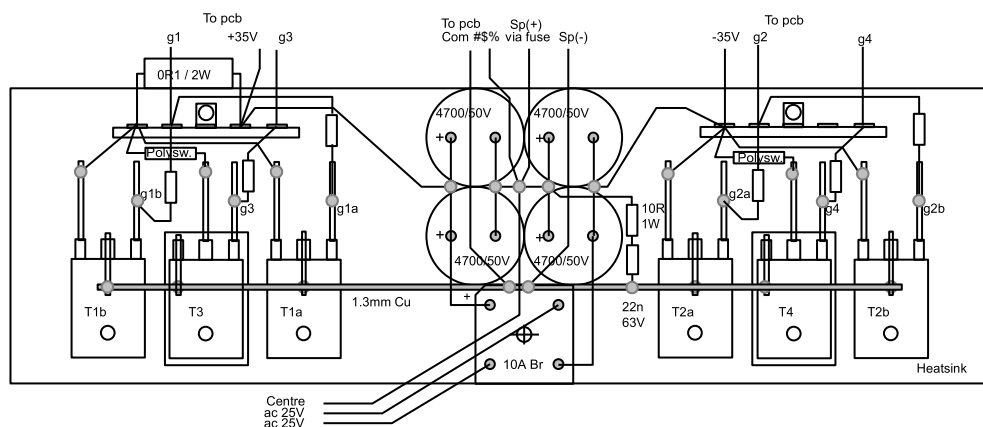


Figure 11: Mounting arrangement for the power transistors and power supply.



tribute only $0.2\ \Omega$ to the MOSFET on-resistance. They need to be mounted away from the heatsink to prevent premature tripping. They can be made pluggable by soldering them across a blown fuse case.

With Poly-switches the output can be safely shorted even when fully driven. The short term output current is 9A RMS initially, falling to 7A after 1 second after the poly switches trip. The 4 amp fuse in the speaker line trips after a further 2 seconds. This design is unusually robust and useful for PA work where robustness is paramount and can justify the relatively high cost of silicon used in this amplifier. This extra silicon also allows scaling to 150 watts in Class-A by increasing the supply voltage (covered later).

Setup This is done in 2 steps. First T1 and T2 will be biased for Class-A, then the shunt stage T3 and T4 is biased. Start with the power off and unplugged.

The $0.1\ \text{ohm}$ current sensing resistor in the drain of T1 (Rd fig 4) is used for initially setting the quiescent current through T1. (A resistor is safer and more convenient than to insert an ammeter into the supply line).

Short the output terminals and the input terminals. Set the bias voltage of T2 to zero by turning P2 fully anticlockwise (until the end-stop 'click' is heard). Check the resistance between the wiper and the input node using a meter to make sure all trim pots are at their minimum.

Turn on the power. Check the green bias LED's all light up (they are quite dim). Set the quiescent current through T1 using P1 and start with 1.0A (100mV across Rd while the heatsink is still cool. After the heatsink has warmed up after 10 minutes and, while still running, remove the output short and connect an ammeter across the load terminals. The current should be around 1.0A. Adjust the T2 bias trim pot P2 until the output current decreases to less than 100mA.

Wait another 15 minutes and re-trim the voltage across Rd to 90mV (900mA through T1) and then re-trim P2 so the output current is less than 10mA (either positive or negative); this will ensure matching of the quiescent currents of T1 and T2.

Setup of the correction MOSFETs quiescent current is between 10mA and 30mA and is done when the heatsink is hot. With fuses in the drains of T3 and T4 it is easy to insert an ammeter to first set T3 to 10mA then T4 to the same.

Next, connect an $8\ \text{ohm}$ 50 watt dummy load and apply a sine wave input signal sufficient to give full output swing of 20V RMS. This setup step can be done by ear in open loop (with one end of Rf open) if you don't have a distortion meter, but you need a reasonably clean sine wave source of 0.05% or less distortion in the 300 to 500Hz range plus an $8\ \text{ohm}$ 50 watt dummy load and a monitor



speaker fed via a 100 ohm 5 watt attenuation resistor (to keep your sanity).

If you have access to a clean sine wave and a distortion meter you can adjust for minimum distortion at half output swing in closed loop into a 8Ω load.

You do this minimum distortion setup by adjusting both P3 and P4 by the same increments. A tip when using a distortion meter is to add a 1M trim pot with a 1M fixed resistor in series and connected between the two gates of T3 and T4 to trim the quiescent current using one trimmer. First, trim pots P3 and P4 are adjusted as before to obtain say 30mA in T3 and T4 with the 1M trim pot set at maximum resistance, then the 1M trim pot can be reduced for minimum distortion. Once the optimum quiescent current is found the 1M trim pot can be removed and T3 and T4 trimmed to obtain this current. Then check the DC output offset for less than 50mV with an 8Ω load.

Finally, turn the amplifier off and let it cool down for 15 minutes. Turn it on again and check that the DC offset voltage across an 8Ω load remains below 400mV (50mA). This amount of DC is quite safe as it cannot harm a voice coil (since 400mV of DC is only 3mW).

If you use very expensive speakers, then for peace of mind you could either install a speaker protection system, or add a bipolar capacitor (to the power supply side of the speaker line). A bipolar capacitor can be made from two back-to-back 15,000uF 63V electrolytic capacitors and shunted with a 1uF 63V polypropylene capacitor. This completes the amplifier setup.

Scaling options Table 2 offers various options for those who want more than 50 watts of Class-A from this design.

	Pout	RL	V _{FL} [V]	Bias [A]	Pdis [W]	C [uF]	Vc [V]	Trans- former	VA	Fuse	+Rps
1	100	4	±33	2x0.9	2x60	2x 10,000	35/ 50	25-0-25	2x160	2x4A	0
2	100	8	±46	2x0.63	2x57	2x 15,000	50	31-0-31	1x330	1x8A	47k
3	150	8	±55	2x0.75	2x70	2x 15,000	63	37-0-37	1x500	1x8A	100k
4	150 (200)	8	±63	2x0.75	2x93	2x 20,000	75	43-0-43	1x530	1x8A	150k

Table 2: Obtaining 100 watts or more in Class-A.



The first option provides 100 watts into 4 ohms simply by paralleling a 2 channel amp. This can be done by directly connecting the outputs and inputs together giving a monoblock. Shorting the outputs of two amplifiers is normally not possible, but it is possible with this design since the damping factor is low. This first option does not require any changes to the circuitry or bias settings and can be returned to a two channel amplifier at any stage (neat! – ed).

The other options provide either 100 watts or 150 watts in Class-A into 8 ohms. They all require paralleling of two output stages, modifications to the power supply and a higher bias setting. They all use the same MOSFETs as the 50 watt design given above where two banks are operated in parallel to supply the higher output current.

Options 3 and 4 require larger heatsinks than options 1 and 2. The larger heatsink I used above (0.37 K/W) is suitable for options 3 and 4. Option 4 is the same quiescent current as option 3 and provides 200 watts in Class-AB with the first 150 watts in Class-A.

Options 2 to 4 use a single custom transformer for both banks of MOSFETs to reduce cost slightly and to improve efficiency. Options 2 to 4 also use a single fuse in the speaker line. A single bias PCB can be used for both banks although this is optional. Another change is to the bias resistor chain, where additional resistors (+Rps in Table 2) are added to each supply rail.

Wrap-up Several Curved Class-A designs have been made public such as Bengt Olsson's, the MJ amp and the Sage Supermos. This is probably first DIY amplifier in print that intentionally applies Square-law Class-A to a power amplifier for audio, and the first proof that over 50% efficiency can be achieved in Class-A.

Listening tests An audiophile friend has been using this Class-A amplifier since 2004 and is pleased with it. He has also performed A/B comparisons with my Square-law Class-AB design [11]. Neither he nor I were able to detect any noticeable differences despite the Class-A's higher output resistance.

It would be good to hear from anyone who builds and test drives any of the designs presented here. You can contact me through the Editor.

Acknowledgement: I would like to thank Mark Aitchison for taking the photos and for his helpful suggestions while compiling this article.



Bill of Material Summary (fig 4; 50W one channel)			
DESCRIPTION	QUAN	COMPONENT	COMMENTS
	1	PCB board	Alternatively use peg-board and overlay printout on top
1K	1	Rin	Input gain resistor
1M	2	R7, R8	
1uF	4	C1, C2, C3, C4	
6u8FBP	1	C7	Input DC filter
10uF/35V	2	C5, C6	
22K	1	Rf	Feedback resistor
47K 1%	2	R3, R4	
100K	4	P1(P1A),P2(P2A),P3(P3A), P4(P4A)	"PxA" smaller size presets
100K 1%	4	R5, R6, R9, R10	
GRN	6	LED4,to LED9	Bias LED's
RED	2	LED2, LED3	Current limit LED's
CON1	2	INPUT and BIAS SUPPLY	Cut from 36-way block
470R	6	Gate resistors	
BD139	1	Temp comp diode	Alternate: BD140 (see text)
0.1R/2W	1	Drain resistor	
0.22R/6W	1	Current feedback	Optional if current feedback not required
10R/1W	1	HF compensation	Can use 22R/1W on higher voltage version.
22nF/100V	1	MKT or Mylar	Can use 63V on 50W version.



0.5A Fast 3AG	2	T3,4 Fuses	Alternate: RDE090A poly switches (see text)
4A fast 3AG	1	Speaker fuse	
35A/400V Bridge	1	Bridge rectifier	Can use 10A on 50W version.
4,700uF/50V	4	PS Caps	
25-0-25V 160VA	1	Transformer	25Vac is at FL (~27Vac NL).
DPDT 2A	1	Shunt stage In/Out switch	See text. Normally not used.
Tag strips	2	5 way tag strips	
Heatsink	1	0.37 K/W eg 300x75x46mm	Altronics* part H0545 by Conrad.
Heatsink (Alternate: see text)	0	0.55 K/W eg 200x75x46mm	Alternate: Altronics H0536 or Jaycar HH8546
T1	2	Exicon ECX10N20 10A/200V	Alternate: Magnatec BUZ900
T2	2	Exicon ECX10P20 10A/200V	Alternate: Magnatec BUZ905
T3	1	Hitachi 2SK400 N-ch 8A/200V	Alternate: 2SK413, 4, 5 or 2SK1530
T4	1	Hitachi 2SJ114 P-ch 8A/200V	Alternate: 2SJ115, 8, 9 or 2SJ201

*Altronics site is www.altronics.com.au

Other components common to 2 channels			
DESCRIPTION	QUAN	COMPONENT	COMMENTS
Mains socket and fuse	1	IEC socket fused	Can include the On/Off mains switch
35A/400V Bridge	1	Bridge rectifier	See text. For earth lifter [4]
10k Log Potentiometer	1	Volume control	Optional
Over-temp cutout	1	80 to 90° C self resetting	Optional, on heatsink, in primary circuit.



Level 1*	Vth [V]	β [A/V]	Rs [Ω]	Rd [Ω]	λ [1/V]	Level 3*	Vth [V]	Kp [-]	L [m]	W [m]	Rs [Ω]
IRF240	3.8	8	10m	98m	3.3m	IRF240	3.82	20.8u	2u	0.44	10m
IRF640	"	"	"	"	"	IRF640	"	"	"	"	"
IRF9240	-3.8	6	30m	0.25	13m	IRF9240	-3.81	10.5u	2u	1.9	30m
IRF9640	"	"	"	"	"	IRF9640	"	"	"	"	"

Table 3: MOSFET parameters for IRF640 and IRF9640 DMOS FETs. (Note values at operating temperature $T_j \sim 100^\circ\text{C}$)

Exicon Lateral	Vth [V]	β [A/V ²]	Rs [Ω]	Rd [Ω]	λ [1/V]	JVth [mV/C]	Jb [mA/V ² /C]
ECF10N20	25m	0.8	125m	1,1	5m	-1.6	-4.5
ECF10P20	-0.37	0.8	125m	1,1	5m	-1.6	-4.5
ECF20N20	25m	1.6	63m	0.55	5m	-1.6	-4.5
ECF20P20	-0.37	1.6	63m	0.55	5m	-1.5	-1.5

Table 4: MOSFET parameters for lateral MOSFETs. (Note values at operating temperature $T_j \sim 100^\circ\text{C}$)

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Appendix A

Square-Law class A efficiency analysis

Square-law Class-A efficiency can be calculated for a sine wave as follows.

Assuming matched and exact square-law devices, with a sine wave input signal ($V_{in} = k \sin \omega t$ where k is the input level fraction between 0 and 1) and for a resistive load we get:

$$I_{DI} = \frac{1}{4} I_m (1 + k \sin \omega t)^2 = \frac{1}{4} I_m (1 + 2k \sin \omega t + k^2 \sin^2 \omega t)$$

where $I_m = V_{DD}/R_L$. Note the last term, the $\sin^2 \omega t$ term, gives only 2nd harmonic distortion.

The voltage drop across each device is $V_{DSI} = V_{dd} (1 - k \sin \omega t)^2$ and so

$$P_{1ave} = V_{DSI} I_{DI} = \frac{1}{4} (1 - \frac{1}{2} k^2) V_{dd} I_m$$

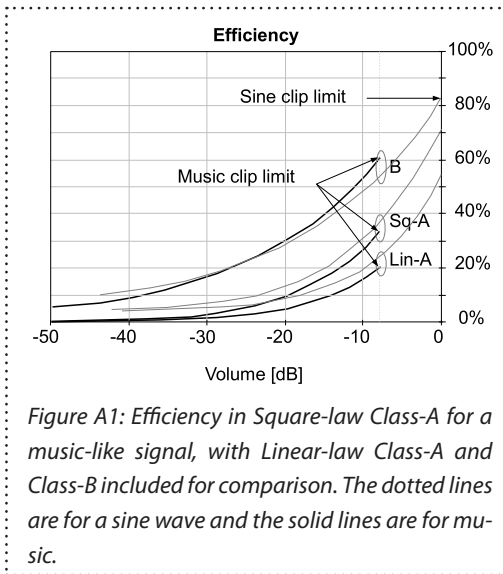
Due to symmetry $P_{DISave} = \frac{1}{2} (1 - \frac{1}{2} k^2) V_{dd} I_{dd}$ so $P_{DISave} = \frac{1}{2} (1 - \frac{1}{2} k^2) V_{dd} I_{dd}$

$$\text{and } P_{OUT} = \frac{1}{2} k^2 V_{dd} I_m \text{ so } \eta = \frac{P_{OUT}}{P_{OUT} + P_{DIS}} = \frac{\frac{1}{2} k^2 V_{dd} I_m}{\frac{1}{2} k^2 V_{dd} I_m + \frac{1}{2} (1 - \frac{1}{2} k^2) V_{dd} I_m}$$

$$\text{hence } \eta = \frac{k^2}{1 + \frac{1}{2} k^2}$$

The maximum theoretical efficiency is when $k=1$, so the maximum efficiency is 2/3 or 66.7%.

This gives a significant improvement in efficiency over Linear-law Class-A with a sine wave, being roughly midway between Linear-law Class-A and Class-B in terms of the amount of hardware needed per output watt. It would be helpful to know whether this relative improvement in efficiency can be maintained with music signals rather than with sine wave signals.



The efficiency in Square-law Class-A with music can be calculated by choosing a waveform with a 8dB Peak-to-Mean Ratio (PMR). An 8dB PMR signal only applies to popular music; orchestral music can be estimated by roughly extrapolating the trend from a sine wave to a 25dB PMR waveform.

Figure A1 plots the results of efficiency analysis for three amplifier classes for both music (solid lines) and sine waves (dotted) signals. Classes are: Class-B, Linear-law Class-A and Square-law Class-A. (The equations used to generate this plot will be given below).

To emulate the waveform for music a bipolar quadratic function was chosen since it is simple

and gives the required triangular probability density function of music. In Figure A1 the maximum volume (or output power) for music stops 8dB short of the sine wave maximum due to occasional clipping. With a PMR of 8dB for the waveform used the amplifiers maximum undistorted output power is 40% of the maximum sine wave power (40% of the power rating of the amplifier).

Waveform	PM R	Linear-law Class-A	Sq. Class-A	Class-B
Sine wave	3dB	50.0%	66.7%	78.5%
Popular Music	8dB	15.0%	30.0%	50.0%
Classical Music	25dB	~ 3%	~ 8%	~ 25%

Table A1: Theoretical maximum efficiency for three classes using sine waves and music.

Table A1 summarises the theoretical maximum efficiencies for Linear-law Class-A, Square-law Class-A and Class-B when driven by different signals: Sine wave, Popular music and Classical music.

Square-law Class-A efficiency is double that of Linear-law Class-A, up from 15% to 30%

with popular music. This was expected at low signal levels since Square-law Class-A is biased at half the bias of Linear-law Class-A. To get close to these figures in practice the volume will have to be set so clipping occurs about 1% of the time. Also, in practical designs, the ON resistance of the MOSFETs plus a volt or two of power supply ripple will lower these efficiencies to about 25% in practical Square-law Class-A amps and about 13% for practical Linear-law Class-A amps.



Transformer and heatsink size comparison Five cases are compared: Linear-law Class-A, Class-B designed for music only, Class-B designed for continuous sine wave operation, the Curved Class-A amp (no shunt stage), and my Square-law Class-A amp.

The quiescent current needed for 50 watts into 8 ohms in Square-law Class-A is $\frac{1}{4}$ the peak current of 3.536A so the bias for true Square-law Class-A is 884mA and with no saturation and power supply ripple (in the ideal world) the dissipation at idle is $2 \times 28.28V \times 0.836A$ or 50 watts, and the quiescent dissipation is the same as the maximum output power.

In the practical Square-law Class-A the quiescent current can be set at $\frac{1}{4}$ of the peak but it was found that 4.7V drop was needed across the MOSFET at the onset of soft clipping, and with a power supply ripple of 1Vpk-pk the supply voltage needs to be 34V when fully driven.

This requires a transformer secondary voltage of 26Vac when measured at rated full load. Transformer output voltage is usually specified at full load, so if you measure a transformer at no load then it will be around 10% more, so the no load voltage will be measured as 28.6V (assuming your mains voltage is the same as the transformer rated primary voltage).

Measured average power supply current for the Sub-squarelaw (no shunt) Class-A amp at 50 watts RMS into 8 ohms was 1.42A when driving an 8R load and 50 watts RMS output. The average input power is therefore $2 \times 1.42 \times 34.0$ or 96.56 watts and the power dissipation by difference is $96.56 - 50.0$ or 46.56 watts and the efficiency is $50.0/96.56 = 51.7\%$. Quiescent power dissipation for the same amplifier when set for 1.2A bias is calculated as $2 \times 35.0 \times 1.2$ or 84 watts or 1.67 times the maximum output power or 67% more than the ideal with true square-law devices and no saturation and power supply ripple. Since the quiescent current with lateral MOSFETs falls from 1.2A when fully driven to the standing quiescent current of 1.1A the power dissipated at idle becomes $2 \times 35 \times 1.1$ or 77 watts or 1.5 times the maximum output power (note the supply voltage rises by 1V from full power to idle).

A bipolar Class-A design can typically swing closer to the rails than a lateral MOSFET version, requiring say 31V supply to achieve 50 watts output. The minimum quiescent current is 50% of 3.54A or 1.77A. The dissipation is therefore $2 \times 31 \times 1.77$ or 110 watts. This is 60% larger than for the Sub-squarelaw Class-A amp. The efficiency for this Linear-law Class-A bipolar example (with 110 watts dissipated and 50 watts output) is at best 31% in practice.

My Square-law Class-A amplifiers average power supply current was 1.32A when driving an 8 ohms load at 50 watts. The power supply voltage needed for 50 watts output was 32V or 2V lower than the Sub-squarelaw Class-A amp due to the extra paralleled MOSFETs. The average input power is therefore $2 \times 1.32 \times 32.0$ or 84.9 watt, and the efficiency is $50/84.9 = 59.2\%$. At idle the supply voltage rises to 33V supply so the quiescent power dissipation is $2 \times 33 \times 0.9$ or 60 watts which is now 1.2 times the



ideal, down from 1.5 times for the Sub-squarelaw Class-A amp (without the shunt stage). The main improvement with the shunt stage is a smaller heatsink requirement for 60 watts versus 77 watts. The transformer VA rating for any amplifier needs to be minimally 1.67 times due to the power factor of the rectifier and filter circuit. My Sub-squarelaw Class-A amplifier required 96.6 watts input and hence the transformer rating needs to be 160VA. But an 180VA transformer is recommended since it will run slightly under its maximum rating.

The transformer rating for my Square-law amplifier with 84.9 watts input is 141VA and 160VA is recommended. The rule of thumb for a practical Square-law Class-A amplifier is therefore a transformer with a VA rating that is 3 times the amplifiers output power. For the Linear-law Class-A case the transformer needs to be minimally 266VA for 50 watts output, and 300VA is recommended. Hence the rule of thumb for a Linear-law Class-A the transformer VA is minimally 6 times the amplifier output power. In other words this Square-law Class-A design only needs half the transformer rating as bipolar Class-A amplifiers. Heatsink dissipation is 60 watts compared to 110 watts, also almost half Linear-law Class-A. This 60 watts dissipation compares well with the value of 60.5 watts calculated earlier for a practical Square-law Class-A amplifier.

Table A2 summarises the figures for the heatsinks and transformers for the various cases for 50 watts output power. These are the best practical values likely assuming regulated power supplies are not used and the loads are mainly resistive. The bold type shows at a glance the relative heatsink sizes and the transformer ratings for the 3 main contenders.

For practical Class-B amplifiers the transformer rule of thumb depends on the signals used (the PMR) as well as the average load reactance. For music and Class-B a transformers VA rating of twice

	Mode	Efficiency P_{out}/P_{in}	Pdis W	HS K/W	Pin W	Min. Tr VA	Re c. VA	VA Ratio (x Pout)
1	Practical Linear-law Class-A	31%	110	0.25	159	266	300	6
2	Sub-squarelaw Class-A	52%	77	0.4	96.6	161	180	3.6
3	Square-law Class-A	59%	60	0.5	84.5	141	160	3.2
4	Practical Class-B (sine)*	75%	~25	1.1	66	109	125	2.5
5	Practical Class-B (music)*	45%	~12	2.2	33	75	75	1.5

**for low reactance loads (pf >0.95)*

Table A2: Heatsink and transformer ratings for 5 practical 50 watt amplifiers.



the amplifiers output power is adequate, although a factor of 1.5 with music can be tolerated for light duty listeners with near resistive loads. For PA work a factor of 2.5 times is recommended. For continuous sine wave operation into lightly reactive loads a factor of 3.5 times is needed with moderately reactive loads ($pf > 0.7$).

Comparing Rows 3 and 5 in Table A2 it can be seen that in practise Class-B for music is far more economical than a practical Square-law Class-A design, where Class-B for music only needs $\frac{1}{4}$ the heatsink of a practical Square-law Class-A design.

As previously suggested, one way to close the gap between Square-law Class-A and Class-B is to operate at a reduced bias in Class-AB, where the quiescent current is reduced to say half that needed for Square-law Class-A operation at full power. For a 50 watt amplifier this is a bias of around 440mA, and Class-AB distortion therefore starts from $\frac{1}{4}$ full power or 12 watts.

Detailed efficiency calculations for three amplifier Classes with a music-like signal.

True Square-law Class-A Efficiency for a Music-like waveform.

Let $\frac{V_{out}}{V_{dd}} = \text{sgn}(t) k t^2 V_{dd}$ for $-1 < t < 1$ and k ranges from 0 to 1 and has period $T=2$.

This provides a triangular PDF which approximates music [13]. This function gives an average power that is 40% of a sine wave.

The output current is $I_{OUT} = \text{sgn}(t) k I_m t^2$ for $-1 < t < 1$ where $I_m = V_{dd}/R_L$ and $I_q = I_m/4$ for the true Square-law Class-A amplifier. Hence the average output power is

$$P_{OUTave} = \frac{1}{2} \int_{-1}^1 V_{OUT} \times I_{OUT} dt = \int_0^1 k V_{dd} t^2 \times k I_m t^2 dt = \int_0^1 k^2 V_{dd} I_m t^4$$

$$P_{OUTave} = \left[\frac{1}{5} k^2 t^5 V_{dd} I_m \right]_0^1 = \frac{1}{5} k^2 V_{dd} I_m$$

Hence PMR is 8dB. This gives a maximum music power 40% of the maximum sine wave power.



$$P_{IN} = V_{dd} I_{D1} + (-V_{dd}) (-I_{D2}) = V_{dd} \left(\frac{1}{4} I_m \left(1 + \frac{V_{OUT}}{V_{dd}} \right)^2 + \frac{1}{4} I_m \left(1 - \frac{V_{OUT}}{V_{dd}} \right)^2 \right)$$

For the parabolic waveform above

$$P_{IN} = V_{dd} \left(\frac{1}{4} I_m (1 + \text{sgn}(t) k t^2) + \frac{1}{4} I_m (1 - \text{sgn}(t) k t^2) \right)$$

$$P_{IN} = \frac{1}{4} V_{dd} I_m (1 + 2 \text{sgn}(t) k t^2 + k^2 t^4 + 1 - 1 - 2 \text{sgn}(t) k t^2 + k^2 t^4) = \frac{1}{2} V_{dd} I_m (1 + k^2 t^4)$$

$$P_{INave} = \int_{-1}^1 P_{IN} dt = \int_{-1}^1 \frac{1}{2} V_{dd} I_m (1 + k^2 t^4) dt \quad \text{so}$$

$$P_{OUTave} = \frac{1}{2} V_{dd} I_m \left[t + \frac{1}{5} k^2 t^5 \right]_0^1 = \frac{1}{2} V_{dd} I_m \left(1 + \frac{1}{5} k^2 \right) \quad \text{so}$$

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{\frac{1}{5} k^2 V_{dd} I_m}{\frac{1}{2} V_{dd} I_m \left(1 + \frac{1}{5} k^2 \right)} = \frac{\frac{2}{5} k^2}{1 + \frac{1}{5} k^2}$$

Hence best music efficiency is 33%, half that for a single sine wave.

$$\frac{P_{INave}}{P_{OUTmax}} = \frac{\frac{1}{2} V_{dd} I_m \left(1 + \frac{1}{5} k^2 \right)}{\frac{1}{2} I^2 V_{dd} I_m} = 1 + \frac{1}{5} k^2$$

Hence the maximum average input power is 1.2 times the maximum sine wave RMS output power.

$$P_{DISave} = P_{INave} - P_{OUTave} = \frac{1}{2} \left(1 + \frac{1}{5} k^2 \right) V_{dd} I_m - \frac{1}{5} k^2 V_{dd} I_m = \frac{1}{2} \left(1 - \frac{1}{5} k^2 \right) V_{dd} I_m$$

$$\frac{P_{DISave}}{P_{OUTmax}} = \frac{\frac{1}{2} V_{dd} I_m \left(1 - \frac{1}{5} k^2 \right)}{\frac{1}{2} I^2 V_{dd} I_m} = 1 - \frac{1}{5} k^2$$

Hence the maximum average dissipation is 0.8 times the maximum sine wave RMS output power.

This is less than the quiescent power dissipation ($P_q = P_{out \max}$) so worst case dissipation is P_q (also $P_{out \max}$).

Linear-law Class-A efficiency for a Music-like waveform

From the previous section $P_{OUTave} = \frac{1}{5} k^2 V_{dd} I_m$ – it is not dependent on the class used.



$$I_{D1} = \frac{1}{2} I_m (1 - k t^2) \quad \text{for } -1 < t < 0 \quad \text{and} \quad I_{D2} = \frac{1}{2} I_m (1 + k t^2) \quad \text{for } 0 < t < 1 \quad \text{and} \\ I_{OUT} = k I_m t^2 \quad \text{for } 0 < t < 1 \quad \text{and} \quad I_{OUT} = -k I_m t^2 \quad \text{for } -1 < t < 0 \quad \text{where} \quad I_m = V_{dd} / R_L \quad \text{and} \\ I_q = \frac{1}{2} I_m.$$

In Linear-Law Class-A Pin is constant and therefore independent of the waveform used, so

$$P_{INave} = V_{dd} I_m = 2 P_{OUTmax} \\ \eta = \frac{P_{OUT}}{P_{IN}} = \frac{\frac{1}{5} k^2 V_{dd} I_m}{V_{dd} I_m} = \frac{1}{5} k^2$$

Hence, for $k=1$ the maximum music efficiency is 20%, or 2/3 that of true square-law Class-A.

$$\frac{P_{INave}}{P_{OUTmax}} = 2 \\ P_{DISave} = P_{INave} - P_{OUTave} = V_{dd} I_m - \frac{1}{5} k^2 V_{dd} I_m = V_{dd} I_m \left(1 - \frac{1}{5} k^2 \right) \\ \frac{P_{DISave}}{P_{OUTmax}} = \frac{V_{dd} I_m \left(1 - \frac{1}{5} k^2 \right)}{\frac{1}{2} V_{dd} I_m} = 2 \left(1 + \frac{1}{5} k^2 \right)$$

Hence the worst case dissipation for Linear-law Class-A is twice that of true square-law Class-A (for all k , music or sine waves).

Class-B efficiency for a Music-like waveform

From previous $P_{OUTave} = \frac{1}{5} k^2 V_{dd} I_m$ where $I_m = I_{pk}$ is the peak current for a

sine wave that reaches full output voltage with no loss in the transistors. Since only one side conducts at one time we have

$$P_{INave} = V_{dd} I_{INave} \quad \text{where} \quad I_{INave} = \int_{-1}^1 I_m k t^2 dt = \left[\frac{1}{3} I_m k t^3 \right]_{-1}^1 = \frac{1}{3} k I_m$$

so $P_{INave} = \frac{1}{3} k V_{dd} I_m$ hence

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{\frac{1}{5} k^2 V_{dd} I_m}{\frac{1}{3} k V_{dd} I_m} = \frac{3}{5} k$$



Hence when $k=1$ the maximum music efficiency is 60%, about twice that of true square-law Class-A with music and 3 times better than Linear-Law Class-A with music.

$$\frac{P_{INave}}{P_{OUTmax}} = \frac{\frac{1}{3}k V_{dd} I_m}{1^2 V_{dd} I_m} = \frac{2}{3}k$$

Hence the maximum input power with music is 2/3 of Pmax with a sine wave.

$$P_{DISave} = P_{INave} - P_{OUTave} = \frac{1}{3}k V_{dd} I_m - \frac{1}{5}k^2 V_{dd} I_m = V_{dd} I_m \left(\frac{1}{3}k - \frac{1}{5}k^2 \right)$$

$$\frac{P_{DISave}}{P_{OUTmax}} = \frac{V_{dd} I_m \left(\frac{1}{3}k - \frac{1}{5}k^2 \right)}{\frac{1}{2} \times 1^2 V_{dd} I_m} = 2 \left(\frac{1}{3}k - \frac{1}{5}k^2 \right)$$

For $k=1$ dissipation is 4/15th or 26.7% of Pmax sine wave. But the maximum dissipation occurs when $k=5/6$, so the maximum dissipation is 5/18 (27.7%) of Pout maximum. If designed for music only, the heatsink size for Class-B is 28% of true square-law Class-A and 1/7th of Linear-law Class-A.

The following tables summarise the results of these calculations.

	Linear-law-A		Square-law-A		Class-B	
	sine wave	Music	sine wave	Music	sine wave	Music
Eff(k)	$\frac{1}{2}k^2$	$\frac{1}{5}k^2$	$\frac{k^2}{1+\frac{1}{2}k^2}$	$\frac{\frac{2}{5}k^2}{1+\frac{1}{5}k^2}$	$\frac{\pi}{4}k$	$\frac{3}{5}k$
$\frac{P_{dis}(k)}{P_{out.max}}$	$2\left(1+\frac{1}{2}k^2\right)$	$2\left(1+\frac{1}{5}k^2\right)$	$1-\frac{1}{2}k^2$	$1-\frac{1}{5}k^2$	$\frac{4}{\pi}k-k^2$	$2\left(\frac{1}{3}k-\frac{1}{5}k^2\right)$
$\frac{P_{in}(k)}{P_{out.max}}$	2.0	2.0	$1+\frac{1}{2}k^2$	$1+\frac{1}{5}k^2$	$\frac{4}{\pi}k$	$\frac{2}{3}k$

* An equivalent waveform with a PMR of 5 (7dB), maximum music power is 40% of the maximum power using a sine wave .

† Volume fraction k ranges from 0 to 1. With real music $k=1$ means occasional clipping (about 1% of the time).

Table A3: Efficiency and power summary for a sine wave and music* as a function of volume level †.



	Linear-law-A		True Square-law-A*		Class-B	
	sine wave	Music	sine wave	Music	sine wave	Music
Max Eff	50%	20%	66.7%	33.3%	78.5%	60%
Practical max Eff (k=0.95)	45%	16%	62%	26%	75%	54%

Table A4: Theoretical and practical Efficiencies for sine waves and music.

	Linear-law-A		True Square-law-A*		Class-B	
	sine wave	Music	sine wave	Music	sine wave	Music
Quiescent dissipation	2.0	2.0	1.0	1.0	0	0
$\frac{P_{dis}(k=1)}{P_{out,max}}$	1.0	1.6	0.5	0.8		
$\frac{P_{in}(k=1)}{P_{out,max}}$	2.0	2.0	1.0	1.0	$(2/\pi)^2 \sim 0.4$	$5/18 \sim 0.28$
Practical worst Pdis (k=0.95)	1.1	2.0	0.55	1.0	0.31	0.28

Table A5 Theoretical and practical Dissipation Fraction for sine waves and music.

	Linear-law-A		True Square-law-A*		Class-B	
	sine wave	Music	sine wave	Music	sine wave	Music
Worst case Pin/Pout max	2.0	2.0	1.5	1.2	1.27	0.667
Practical worst Pin (k=0.95)	2.0	2.0	1.45	1.0	1.30	0.60

Table A6: Theoretical and practical Input Power Fraction for sine waves and music.



Appendix B

Distortion analysis in Square-law Class-A

Step 1: Calculating the quiescent current required for Square-law Class-A. The distortion in Square-law Class-A can be calculated for a practical circuit using the SPICE MOSFET model parameters by first calculating the quiescent current required for Square-law Class-A then calculating the amount of gm fall at full output swing. Next, the level of 3rd harmonic distortion can be calculated with reasonable accuracy from the percentage gain drop.

The Level-3 MOSFET model includes the Early effect λ ($\lambda=1/V_A$ where V_A is the Early voltage), mobility modulation (θ), and source resistance (R_s). The MOSFET current is described by

$$I_D = \frac{\beta}{2} \frac{(V_{gs} - V_{th})^2 (1 + \lambda V_{ds})}{1 + \theta (V_{gs} - V_{th})} \dots\dots\dots (\text{eq. 1})$$

where V_{th} is the threshold voltage, $\theta = \theta_{fet} + \beta R_{stot}$. In Square-law Class-A each MOSFET is biased by a voltage (V_{bias}) in addition to the threshold voltage, and this bias needs to be sufficient for Class-A. When one device gets close to zero current the other reaches its maximum current, and this occurs when $V_{in} = V_{bias}$.

The maximum current is $I_{max} = (V_{DD} - V_{Dson})/R_L$ giving $I_{max} = \frac{\beta_{eff}}{2} \frac{(2V_{bias})^2}{1 + 2\theta V_{bias}}$

where $\beta_{eff} = \beta_0 (1 + \lambda V_{Dson})$ Since V_{Dson} is small when I_D is maximum we can approximate

to $\beta_{eff} = \beta_0$.

Cross multiplying gives $2\beta_0 V_{bias}^2 - 2\theta I_{max} V_{bias} - I_{max} = 0$ and solving for V_{bias} using the

quadratic equation gives $V_{bias} = \frac{2\theta I_{max} \pm \sqrt{(2\theta I_{max})^2 + 8\beta_0 I_{max}}}{4\beta_0}$ The positive root is



used since it is the largest. Substituting $\theta = \beta R_{\text{Stot}}$ we get

$$V_{\text{bias}} = \sqrt{\frac{I_{\text{max}}}{2\beta_0} + \left(\frac{1}{2} I_{\text{max}} R_{s_{\text{tot}}}\right)^2} + \frac{1}{2} I_{\text{max}} R_{s_{\text{tot}}}$$

The following example is for the Sub-Square-law Class-A amp (no shunt stage). Parameters for a dual-die lateral MOSFET (eg Execon 20N20) at 100°C are: $\beta = 1.6 \text{ A/V}^2$, $\theta = 0.1 \text{ V-1}$ and $\lambda = 3 \text{ mV-1}$. For a supply voltage $V_{\text{dd}} = \pm 34 \text{V}$ and $V_{\text{max}} = 28.28 \text{V}$, P_{out} is 50W RMS into 8 ohms, so $I_{\text{max}} = 28.28/8 = 3.535 \text{A}$.

The bias voltage

$$V_{\text{bias}} = \sqrt{\frac{3.536}{2 \cdot 1.6} + 0.11^2} + \frac{1}{2} \cdot 0.063 \cdot 3.536 = 1.06 + 0.11 = 1.17 \text{ Volts}$$

Now this bias voltage is used to find the quiescent current

$$I_q = \frac{1.6}{2} \frac{1.17^2 (1 + 3 \text{m} \cdot 34)}{1 + 0.1 \cdot 1.17} = 1.06 \text{ Amps}$$

With true square-law devices the quiescent current is $\frac{1}{4}$ the peak current I_{max} or $3.536/4 = 884 \text{mA}$. In this case (Sub-Square-law, no shunt devices) the quiescent current must be 1.06A to achieve the peak current of 3.535A.

Table B1 uses a spreadsheet to automate the above equations. Row 1 is a repeat of the lateral MOSFET example above for the Sub-Squarelaw Class-A amp (no shunt stage).

	# fets	Rs	Po-8Ω	Vmax	Imax	Fetβ	Fetθ	Fetλ	EqRs	Vb	Iq	gm0	D3%
1	2	0	50	28.28	3.536	1.6	0.1	3.0E-3	0.063	1.17	1.06	3.44	1.69
2	2	0	50	28.28	3.536	1.6	0.1	0.0E+0	0.063	1.17	0.98	3.17	1.13
3	1	0	50	28.28	3.536	0.8	0.1	3.0E-3	0.125	1.72	1.1	2.36	2.03
4	1	0.22	50	28.28	3.536	0.8	0.1	3.0E-3	0.125	2.22	1.32	1.93	3.35
5	1	0.11	50	28.28	3.536	1.6	0.1	3.0E-3	0.063	1.4	1.23	3.02	2.87
6	1	0	50	28.28	3.536	8	0.1	3.0E-3	0.013	0.49	1	7.96	1.16
7	1	0.22	50	28.28	3.536	8	0.1	3.0E-3	0.013	1.04	1.59	4.12	4.17

Table B1: Calculations for quiescent current, gm & HD3 for 7 practical 50 watt cases (lateral & DMOS FETs with & without external source resistors)



The gm_0 and distortion D3% columns are discussed separately in the next section.

- Row 2 is with the Early parameter (λ) set to zero to show the change in distortion due to the Early effect.
- Row 3 is with the normal Early parameter but one lateral MOSFET rather than 2.
- Row 4 is Row 3 with a 0.22Ω source resistor added to the MOSFET.
- Row 5 is Row 4 with two MOSFETs in parallel each with a 0.22Ω source resistor.
- Row 6 is with DMOS FETs like IRF640's in a non-complementary Class-A amp with no source resistor.
- Row 7 is with DMOS FETs in Class-A amp with 0.22Ω source resistors. My simulation of the Zen V5 showed the current in each MOSFET is quite close to linear over most of the current range. DMOS FET parameters used are summarised in Table 3 of the main article.

Step 2: Calculating the distortion in Square-law Class-A The SPICE MOSFET Level-3 current equation can be differentiated so the amount of gain drop can be found at full output swing. Since this gain drop gives predominantly 3_{rd} harmonic distortion it can be calculated using

$$D_{3rd} = \frac{1}{12} \left(\frac{\Delta G}{G} \right)$$

Differentiating I_d (eq. 1 above) gives

$$gm(Vin) = \frac{\beta V_b}{1 + \theta(Vin + V_b)} \left(1 - \frac{1}{2} \theta \frac{Vin + V_b}{1 + \theta(Vin + V_b)} \right)$$

The maximum gain is when $Vin=0$ so $gm(0) = \frac{2\beta V_b}{1 + \theta V_b} \left(1 - \frac{1}{2} \frac{\theta V_b}{1 + \theta V_b} \right) (1 + \lambda V_{dd})$.

The factor of 2 appears because both MOSFETs contribute equal gains when $Vin \sim 0$. Also note the Early effect does not contribute a significant factor to the gain at full swing. The distortion can now be calculated

$$D_{3rd} = \frac{1}{12} \left(\frac{\Delta G}{G} \right) = \frac{gm(0) - gm(Vb)}{gm(0)}$$

$$D_{3rd} = \frac{1}{12} \left(1 - \frac{1 + \theta V_b}{1 + 2\theta V_b} \frac{1 - \frac{\theta V_b}{1 + 2\theta V_b}}{1 - \frac{1}{2} \frac{\theta V_b}{1 + \theta V_b}} \frac{1}{(1 + \lambda V_{dd})} \right)$$



Since the gain drop follows a parabola proportional to $(V_{in}/V_b)^2$ the amount of distortion can be found in general

$$D_{3rd}(V_{in}) = \frac{1}{12} \left(1 - \frac{1 + \theta V_b}{1 + 2\theta V_b} \frac{1 - \frac{\theta V_b}{1 + 2\theta V_b}}{1 - \frac{1}{2} \frac{\theta V_b}{1 + \theta V_b}} \frac{1}{(1 + \lambda V_{dd})} \right) \left(\frac{V_{in}}{V_b} \right)^2$$

Using the same lateral MOSFETs as Row 1 in Table B1 above: $\beta=1.6$, $\theta=0.1$, $\lambda=3.5m$, $V_{dd}=34V$. From above $V_b=1.17V$ and $I_q=1.06A$. The small-signal gain is

$$g_m(0) = \frac{2 \cdot 1.6 \cdot 1.17}{1 + 0.1 \cdot 1.17} \left(1 - \frac{0.1}{2} \frac{1.17}{1 + 0.1 \cdot 1.17} \right) (1 + 3m \cdot 28) = 3.44 \text{ S}$$

and

$$D_{3rd}(V_{in})\% = 100 \times \frac{1}{12} \left(1 - \frac{1 + 0.1 \cdot 1.17}{1 + 2 \cdot 0.1 \cdot 1.17} \frac{1 - \frac{0.1 \cdot 1.17}{1 + 2 \cdot 0.1 \cdot 1.17}}{1 - \frac{1}{2} \frac{0.1 \cdot 1.17}{1 + 0.1 \cdot 1.17}} \frac{1}{(1 + 3m \cdot 28)} \right) \left(\frac{V_{in}}{V_b} \right)^2$$

and thus

$$D_{3rd}(V_{in})\% = \frac{100}{12} 0.21 \left(\frac{V_{in}}{V_b} \right)^2 = 1.69\% \left(\frac{V_{in}}{V_b} \right)^2$$

Table B1 above includes calculations of open loop gain g_m and open loop distortion for 7 variations. Row 1 repeats the manual calculations above at full output power giving an open loop distortion (D_{3rd}) of 1.69%. At 1 watt distortion falls by the factor $(2.8/20)^2$ giving $0.02 \times 1.69\%$ or 0.033% at 1 watt in open loop. This relationship was observed in the measured distortion as shown in Figure 7 of the main article.

Row 2 shows that the Early Effect is responsible for 1/3rd of the distortion in practical lateral MOSFET Square-law Class-A amplifiers.

Row 3 shows that halving the number of parallel MOSFETs only increase the distortion by 1.2 times. The use of two MOSFETs in parallel does not change distortion by much.



In Row 4 adding 0.22Ω source resistors to Row 3 nearly doubles the distortion, which seems quite counter-intuitive!

Row 6 shows matched DMOS FETs without source resistors can halve distortion compared to one pair of lateral MOSFETs (Row 3). This assumes the DMOS FETs are well matched, but this is not usually the case unless the Olsson [10] non-complementary topology is used.

Row 7 shows adding 0.22Ω source resistors increases distortion by about 4 times, as well as halving the g_m giving a net distortion increase of about 8 times when operated as a voltage follower. This shows just how disastrous source resistors are in MOSFET Class-A amplifiers, and especially vertical MOS Class-A amplifiers. Lateral MOSFETs are not as sensitive to the inclusion of this source resistor, but then, there is no need to add them to lateral MOSFETs when paralleled since they have a negative temperature coefficient (unlike DMOS FETs in saturation).

Even a small amount of local negative feedback from these resistors increases distortion and significantly reduces Class-A efficiency. This is demonstrated by the Zen V5 where source degeneration effectively doubles the heatsink size for Class-A and increases distortion by about 8 times simply by adding the 0.22Ω source resistors!

Step 3: Calculating voltage-follower closed loop distortion and damping factor As noted in the main article, the proposed amplifier can also be configured as a voltage follower output stage. Third harmonic distortion (D3) can be calculated for a voltage follower using the feedback factor $1/(1+Av_{OL})$ where $Av_{OL} = g_m \cdot R_L$ and $g_m \sim g_{m0}$. For Row 1 as a follower distortion would be $D_{CL} = 1.69\% / (1+3.44 \times 8) = 1.69\% / 28.5 = 0.06\%$ and at 1 watt becomes $0.033\% / 28.5 = 0.001\%$. For DMOS Row 6 $D_{CL} = 1.16\% / (1+7.96 \times 8) = 1.16\% / 64.7 = 0.018\%$ and at 1 watt becomes 0.0036% . A similar distortion of 0.02% was previously calculated in my Square Law Rules article [11] for similar DMOS FETs but using a more approximate method (using $g_m \sim \theta V_{bias}$).

It is of interest to note that DMOS FETs give about twice the open loop gain as lateral MOSFETs, and as voltage followers DMOS FETs give about $\frac{1}{4}$ the distortion assuming they are well matched. In practice complementary DMOS FETs are not well matched, so their distortion advantage is diminished compared to lateral MOSFETs, unless Bengt Olsson's non-complementary totem pole or OTL configuration (with only n-channel DMOS FETs) is used [10]. Olsson's DMOS design was 0.015% as a voltage follower [12].

As a voltage follower in Class-A (Row 6) and at 1 watt, Square-law Class-A DMOS distortion is 0.002% . Similarly, for lateral MOSFETs Row 1 gives 0.0035% distortion at 1 watt.

With such low distortion figures in open loop it is possible to make a practical audio power amplifier



using a pair of lateral MOSFETs or DMOS FETs. The just noticeable level for 3rd harmonic distortion is around 0.1% so for a Row 1 amplifier the level needs to be below $0.1/1.69 \times 50W = 0.06 \times 50W$ or 3 watts (which corresponds to around $\frac{1}{4}$ of the full output voltage swing).

At normal listening levels music spends most of its time in the first few watts with occasional peaks of up to 50 watts so the Row 1 amplifier distortion was very hard to hear in open loop unless the volume is turned up a little more than usual. By applying just 6dB of negative feedback the power for 'just noticeable distortion' can be increased by 4 times to 12 watts (which corresponds to around $\frac{1}{2}$ the full output voltage swing of a 50 watt amplifier). This amount of feedback was found to be adequate in practice providing a modest distortion margin as well as lowering the amplifier's output resistance for sufficient speaker damping for the speakers I used.

The output resistance as a voltage follower is $1/gm_0$ and since $DF=RL/R_{out}$, for a voltage follower we get $DF = gm_0 * RL$. Note this figure is the same as the open loop voltage gain. For Row 1 as a voltage follower we expect to get a damping factor of 28.5, and for the DMOS Row 6 case the damping factor is 64.7. Interestingly, Row 7 damping factor as a voltage follower will be about half that of Row 6 when source resistors are added.

