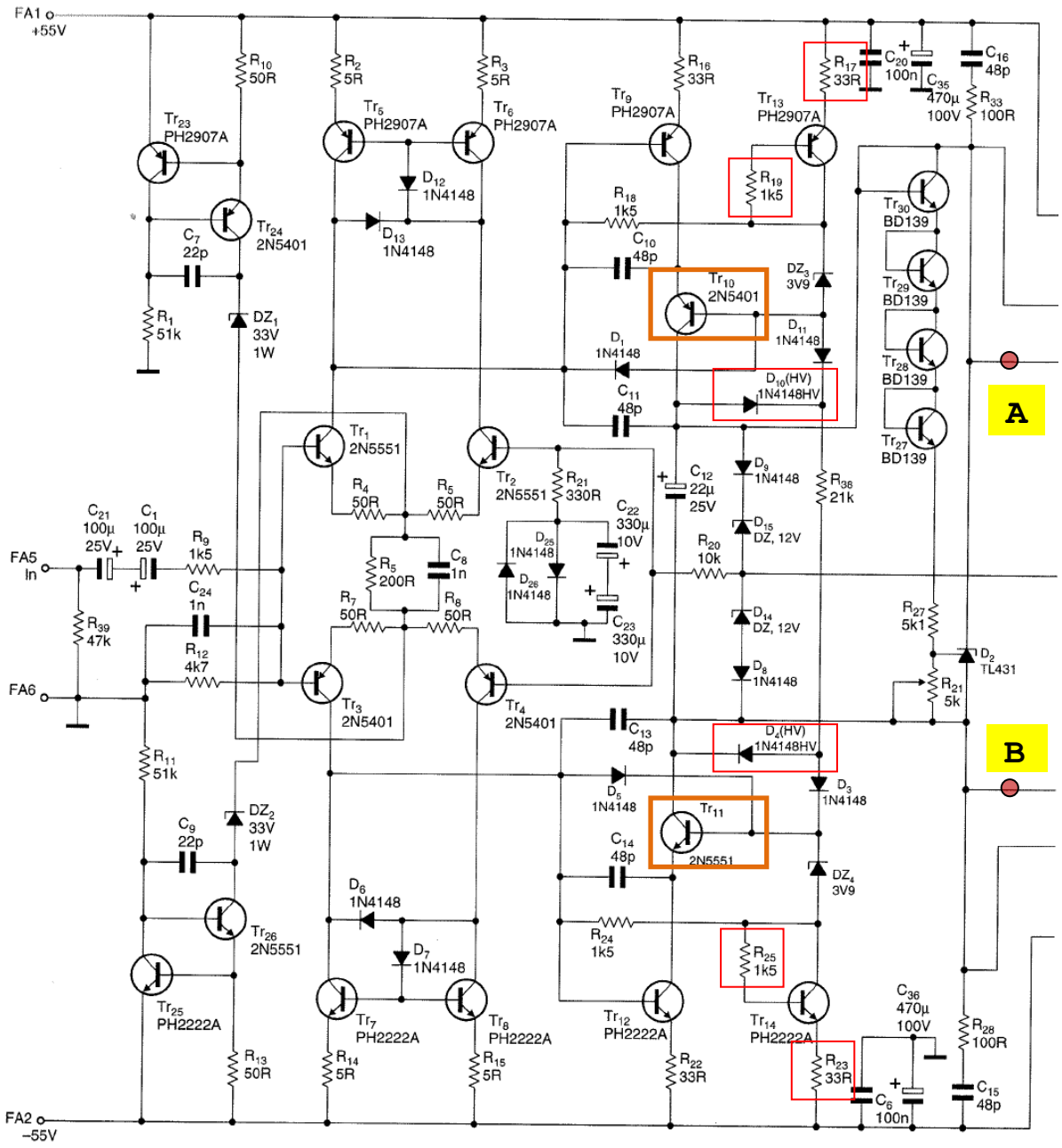
Recommendations for powering the Ultra-fast Amplifier by a single dual supply voltage ranging from ± 60V to ±65V (mainly for new PCB's)



case V_{os} is limited to few hundred millivolt. This represents an acceptable level of output offset.

Filtering added. Another change made to increase flexibility is to allow the possibility of incorporating an input passband filter, via components C_1 and C_{21}, together with R_{12} for the high-pass section and R_9+C_{24} for the low-pass section.

In the following analysis, C_1 and C_{21} are considered equal to $2C_H$. With component value shown, the –3 dB bandwidth is 1Hz to 120kHz. Assuming that the signal source resistance, which is usually lower than 300Ω, has no influence, high-pass and low-pass frequency corners are given by

$$f_H = \frac{1}{2\pi R_H C_H}$$

and

$$f_L = \frac{1}{2\pi R_L C_{24}}$$

respectively, where R_H is the sum R_{12}+R_9, and R_L is the parallel R_{12}//R_9. They are easily adapted, and the low-pass section can be bypassed by omitting C_{24} and shorting R_9.

Improved temperature sensing. The temperature-sensing network *TS* incorporates an additional transistor. This adds

Fig. 1. Detailed circuit diagram of the chosen practical implementation of the 100W/8Ω audio-power amplifier, featuring a speed higher than 300V/µs and rated power thd figures of 0.002% and 0.018% at 1kHz and 20 kHz, respectively. All diodes are 1N4448 Diodes D_4 and D_{10} marked 1N4448HV are still 1N4448, but selected for a reverse voltage higher than 120V. This selection is made by applying a reverse voltage of 130V via a resistor of 10kΩ and measuring the current, which has to be less than 10mA. The yield is normally higher than 50%.

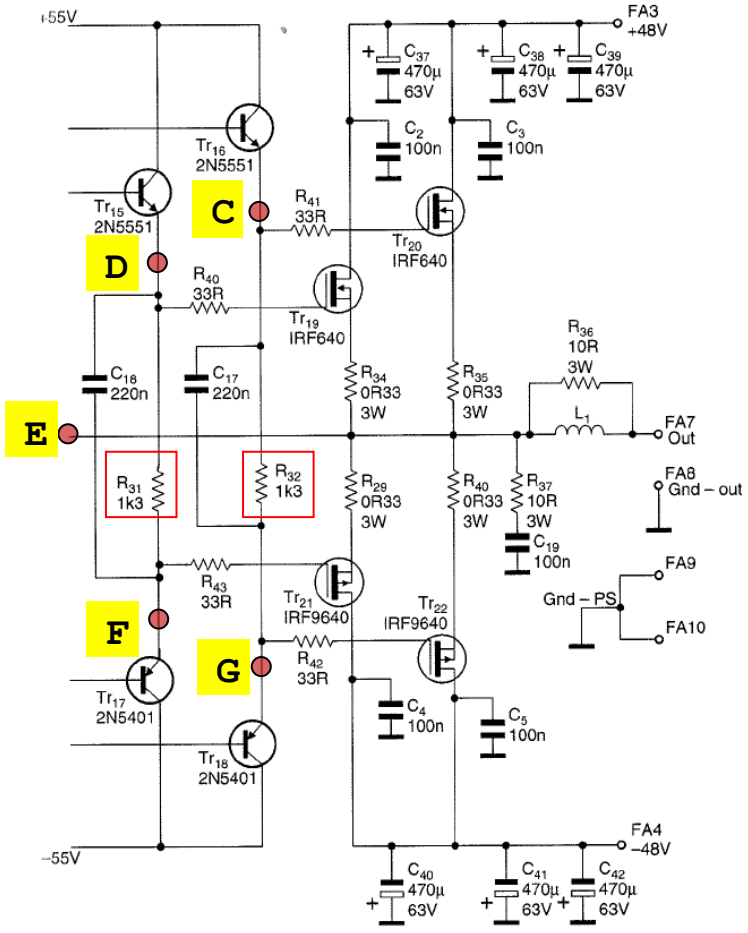


Table 2. Slewing performance of the audio power amplifier for a source resistance of 50Ω and an 8Ω load. Pulse input was 6V peak, as in Fig. 4 of my previous article.[1]

Characteristic results	Measurement
Positive slew-rate	+320V/µs
Negative slew-rate	–300V/µs

Table 3 . Total harmonic distortion figures of the final 100W/8Ω audio power amplifier for a source resistance of 50Ω and an 8Ω load. Quiescent current was 150mA and bandwidth 80kHz.

V_{out}, pk-pk	1kHz	20kHz
5	0.0030%	0.0043%
10	0.0028%	0.0047%
20	0.0023%	0.0061%
40	0.0028%	0.0110%
80	0.0026%	0.0170%

Note: Total harmonic distortion remains virtually constant when source impedance R_s varies in the range 50Ω to 5kΩ. The instrumentation limit, thd+noise, was 0.002% at 1kHz; 0.003% at 20kHz.

extra flexibility to the mounting mode of the temperature-sensing network relative to the power output devices $Tr_{19\text{-}22}$.

In my original prototype, the three sensing transistors were mounted very close to output power mosfets. A total $\Delta V_{TS}/\Delta T$ of –6mV/°C was adequate.

However, when a more practical scheme for mounting the temperature-sensing network on the heat sink is needed, like the one presented here, you have to allow a looser thermal coupling with power devices. Because of this, $\Delta V_{TS}/\Delta T$ will be higher and it may turn out that a greater number of temperature sensing transistors will be needed.

In the layout scheme proposed, four transistors providing a $\Delta V_{TS}/\Delta T$ of –8mV/°C were x found adequate to provide a fairly stable – within 20% – output power mosfets bias setting under a wide range of operating conditions.

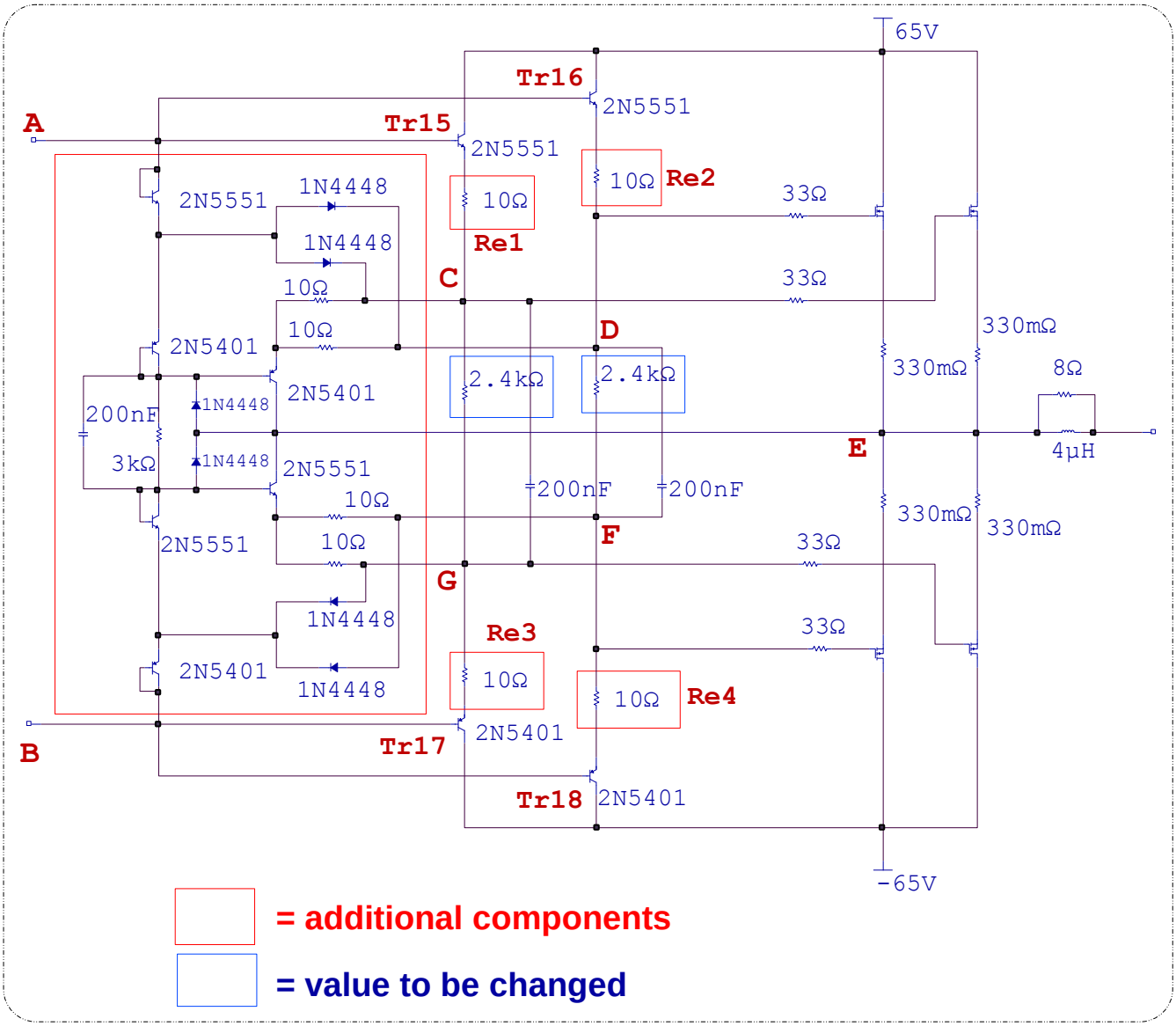
The quiescent current of output devices has been set to 150mA, which further contributes to the thermal stability of the operating point of the output mosfets. The

Table 1. Main characteristics of the fast audio power amplifier for 150mA quiescent current and 80kHz bandwidth.

Characteristic	Measurement results
Measured output offset voltage	+32mV
DC open-loop gain	110dB
Low-frequency closed loop gain	32dB
Small-signal bandwidth before the output filter (–3dB)	20Hz (–0.1dB), 1.3MHz
Unity gain frequency before the output filter	22MHz
Open-loop gain at 20kHz	66dB
Closed-loop amplifier phase margin before the output filter	+76°
Output noise (BW=80kHz, input terminated with 50Ω)	42µV rms
Slew rate	See Table 2
Total harmonic distortion (thd)	See Table 3

Figure below shows the full schematic diagram of the recommended driver with current limiter for powering the ultra-fast amplifier with a single dual supply voltage up to ± 65V.

Main feature: peak emitter current of Tr_{15}-Tr_{18} is limited (by four additional diodes) to about $Imax=V_{be(on)}/Re$, i.e. about 60mA with Re=10Ω.



Details of the recommended solution

Table 1(B)

step	component	current value	replace with	desired effect/comments
1	R_{17}, R_{23}	33Ω	5Ω	reduce Tr_{10}-Tr_{11} idle current I_Q(IS) to about 6-7mA (if needed)
2	R_{19}, R_{25}	1.5kΩ	1.5kΩ...5Ω	to be done **only if step 1 is not enough**: I_Q(IS) about 6-7mA
3	Tr_{10}	2N5401	2 x 2N5401 (*)	**recommended action** with power supply higher than ±55V (penalty: slew-rate slightly reduced)
4	Tr_{11}	2N5551	2 x 2N5551 (*)	
5	R_{31}, R_{32}	1.3kΩ	2.4kΩ	Tr_{15},Tr_{17}, Tr_{18},Tr_{19} idle current (power!) reduced to 3-4mA
6	D_4-D_{10}(HV)	1N4148(HV)	BAV21	avoid selection of 1N4148 (BAV21 is a 200V fast diode)
7	Tr_{15}, Tr_{16}	2N5401	2 x 2N5401 (#)	**optional action**, see note.
8	Tr_{17}, Tr_{18}	2N5551	2 x 2N5551 (#)	

NOTES:

(*) transistors matched within ΔVbe ≦ 10mV @ Ic=5mA

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b) add an emitter resistor (Re) to MOSFET driver BJT's (Tr15-Tr18) as shown here below, in order to distribute the high emitter peak current and peak power, and reduce the risk of failure.
A suitable value for Re is comprised between 12Ω and 24Ω, which correspond to a total maximum emitter current Ie_{peak} limited to about 100mA and 50mA, respectively.
With Re=15Ω, Ie_{peak} = 80mA.