# UGS for Dummies.

- The ins and outs of UGS Buffer -

*This document is a translation from French to English, the grammar is therefore not perfect.*

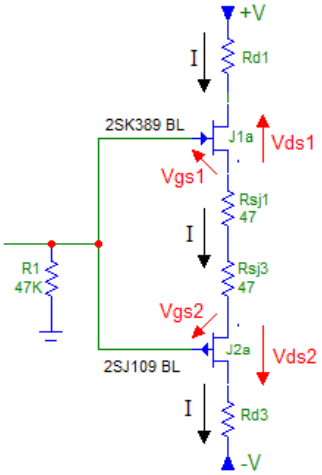
**- How does it work?**

If the diagram looks simple, then that's because it is, but only on the surface. However, spite all the equations you will see and encounter, you will be able to realize the circuit. In the end, it is not as complex as it might seem. As the main tool, you will need Ohm's law and Kirchhoff's law of current, which is mostly it.

We will look at the function step by step. Take this paper as a modest tutorial and as a background analyze and you will realize that the circuit can be applied to other designs.

**- At rest.**

We will start by looking at what happens at rest, which is to say in the absence of applied signal. So we'll start by looking at what happens at rest (in the absence of signal). For this, we will simplify the scheme so as not to get confused. If you take care of first from the input, and removing cascodes, current mirrors and counter reaction ($R_{IN}$ and $R_{FB}$), we get:




For what we are interested in, it is equivalent to more complex editing. J2a source resistance (Rsj3) includes the VR2 trimpot (its half in fact) and the 22Ω resistance for clarity, but overall, it must be said that all JFet source resistances are the same. In addition, the second half of the differential amp, is exactly the same thing (at rest).

Image: "I" is the current that flows through the JFets. It enters through the drain of J1a, exits through its source with the same value, enters the source of J2a, and exits through the drain to the least of the power supply. The two grids JFets are to ground, because of R1 and the current infinitesimal grid.

Equation for signal input:

(1)

$$V_{GS1} + 2R_S I - V_{GS2} = 0$$

The current in the JFETs are:

(2)

$$I = \frac{V_{GS2} - V_{GS1}}{2R_S}$$

If we consider that the JFets N and P are identical, it means, among other things, that $V_{GS1} = -V_{GS2} = V_{GS}$ (these are JFets of opposite polarity). So it simplifies the equation, and we end up with:

(3)

$$I = -\frac{V_{GS}}{R_S} \quad \text{in other words} \quad V_{GS} = -R_S I$$

In parentheses, beware of these $V_{GS}$: for a JFet N, grid voltage is less than the source voltage ($V_{GS} < 0$) and for a JFet P, it is obviously the reverse ($V_{GS} > 0$). It can be a bit disturbing at first, but you get used to it soon enough.

If you take a closer look at the JFets, you can find in all the books that a good approximation of the drain current is given by:

(4)

$$I = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GSOff}}\right)^2$$

Where $I_{DSS}$ is the max current of the JFet (saturation), and $V_{GSOff}$ is the pinch off voltage, in other words, the tension between grid and source for which the drain current is no. These values can be found in JFETs datasheets. These are two intrinsic characteristics of the JFets, linked to their construction. Then you think you're smart, so you replace in this last equation $V_{GS}$ with $-R_S I$ (equation 3), and you end up with something complicated in the second order:

(5)

$$\frac{I_{DSS} R_S^2}{V_{GSOff}^2} I^2 + \left(\frac{2 I_{DSS} R_S}{V_{GSOff}} - 1\right) I + I_{DSS} = 0$$

So not to lose face, we plunge back into his second classes, we fight with the discriminating, and finally we get to:

(6)

$$I = \frac{V_{GSOff}^2}{2I_{DSS}R_S^2}\left[\left(1-\frac{2R_SI_{DSS}}{V_{GSOff}}\right)-\sqrt{1-\frac{4R_SI_{DSS}}{V_{GSOff}}}\right]$$

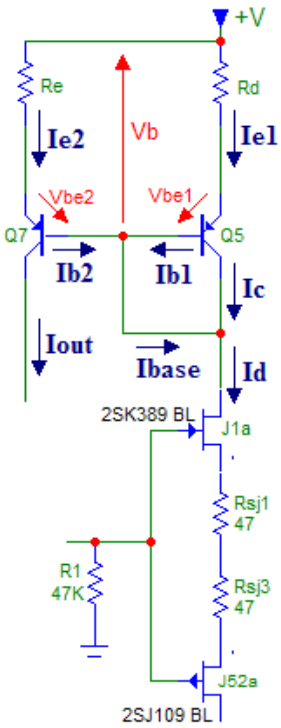
**- Beuark…**

For the case we are interested in, if we take the datasheet of the 2SK389, we can see that for an $I_{DSS}$ of 8mA, the $G_{SOff}$V is about 0.6V. With a source resistance $R_S$ = 47Ω, we then obtain the polarization current of the JFets of 3.8mA. And that's basically what we actually have.

All this to get to this point... I know we could have made it simpler by tracing the input and load rights etc... But I have every right to have fun, right? And then it's a valid equation in a lot of configurations, and it allows, if you take the trouble to draw the curve, to get an idea of the value of the current rest according to the source resistance.

In parentheses, you can also guess here why you can't make a UGS module with bipolar transistors as input, at least with this particular topology... No volunteer? Well simply because bipolar scanning themselves in this way. They will have to ancillary current sources so that they can go into conduction, while there, a beast source resistance and a mass reference on the grid are enough to polarize a JFet. The precious give it the name of "economic polarization", since it requires only a minimum number of components.

But back to our gigots. For the moment, we know that at rest the JFets are traversed by a current $I_D$ that have been calculated by (6).




Now we're going to go step by step to the entire schematic of the bazaar. We're going to do for the time being the impasse on cascodes. They serve, so to speak, no purpose in calculating the rest configuration. Same goes for the counter-reaction. But by however, we will have to be interested in current mirrors.

We're only going to look at one quarter of the editing before we go any further.

$I_D$ is the current in the JFets that we have just calculated so painfully. And now we're going to try to figure out what's going on in the two bipolar transistors.

We start by looking at what the tension between the positive power rails is worth and the common bases of the two bipolars. One can obviously write this tension $V_B$ as:

$V_B = R_DI_{E1} - V_{BE1}$ but also $V_B = R_EI_{E2} - V_{BE2}$ from here we can deduce that:

$$R_DI_{E1} - V_{BE1} = R_EI_{E2} - V_{BE2}$$

To simplify our lives, we now assume that our two transistors are identical to the silicone maximum operation, which leads us to admit that $V_{BE1} = V_{BE2}$. Indeed, the basic tension emitting a bipolar is a "basic" characteristic - funny, that -- of these components. To simplify, we will say that it is constant and that it is worth in the 0.6V-0.7V, but it serves no purpose.

(7)

From there, it's easy to see that:

$$I_{E1} = \frac{R_E}{R_D}I_{E2}$$

Well, we got a smooth relationship between the transmitter currents of the two bipolars, but what interests us in the end is rather the $I_{OUT}$ collector current, and how it is connected to the current $I_D$ in the JFets.

We're going to ask Gustav Kirchhoff for a little help, because according to him $I_D = I_C+I_{BASE}$ and $I_{BASE} = I_{B1}+I_{B2}$, which leads us to:

(8)

$$I_D = I_C + I_{B1} + I_{B2}$$

On the other hand, in a bipolar transistor, transmitter, collector and base currents are bound by the relationship:

$$I_{EMITTER} = I_{COLLECTOR} + I_{BASE}$$

This means that in the equation (8), the term $I_C$ - $I_{B1}$ is actually the transmitter current of the first transistor, $I_{E1}$. So we get:

(9)

$$I_D = I_{E1} + I_{B2}$$

We are very lucky, because the equation (7) allows us to replace $I_{E1}$ with an equivalence in $I_{E2}$, so that (9) can be written as:

(10)

$$I_D = \frac{R_E}{R_D} I_{E2} + I_{B2}$$

It is time here to call to the rescue the gain by running of transistors, the famous $\beta$, which allows to link the different currents of a transistor between them:

(11)

$$I_{Collector} = \beta I_{Base} \quad \text{and} \quad I_{Emitter} = (\beta + 1) I_{Base}$$

So in our case we can write:

(12)

$$I_D = \frac{R_E}{R_D}(\beta+1) I_{B2} + I_{B2} = I_{B2}\left((\beta+1)\frac{R_E}{R_D} + 1\right)$$

But by the grace of (11), we also have $I_{B2} = I_{OUT}/\beta$, so that in the end, you end up with:

(13)

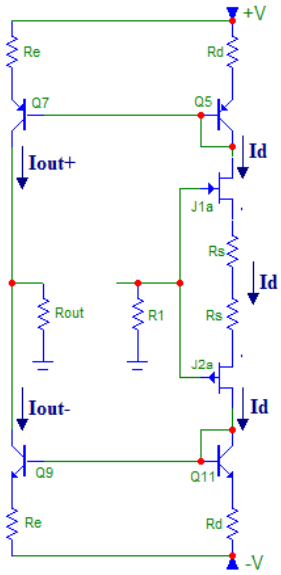
$$I_D = \left(\frac{\beta+1}{\beta}\frac{R_E}{R_D} + \frac{1}{\beta}\right) I_{OUT}$$

If we use transistors with a gain β - large enough, we can safely say that the ratio (β+1)/ $\beta$ is very close to 1 and that the term 1 becomes negligible in front of the other, which ultimately brings us back to:

(14)

$$I_{OUT} = \frac{R_D}{R_E} I_D$$

So the current "mirror" output current is simply equal to the input current multiplied by the ratio of the two transmitter resistances. Some would say that I could have gone much faster by saying that the transmitter currents are almost equal to the collector currents, and apply (7) directly to the collector currents... But why make it simple when you can make it complicated?




But it's time to make a little point about where we stand exactly. If we summarize the situation briefly, we saw that the source resistances allow us to fix (for given JFets) the current circulating at rest in the JFets. And the ratio of bipolar transmitter resistances allows us to know the exit current of the mirror in relation to this JFets resting current. So far only a small part of the entire scheme has been considered, but it is exactly the same for all the other quadrants in the scheme, at least at rest. If we only look at the left half of the entire scheme (without the cascodes or the counter reaction), we get:

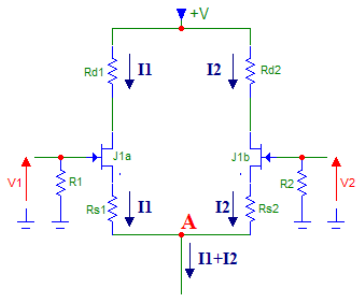
The $I_D$ current is therefore fixed by the JFets source resistances, and it is the same for both J1a and J2a FETs. If we assume that all bipolar transistors have the same characteristics, they will react in the same way, and as a result the current mirrors will behave in the same way.

It means that being driven by the same current, the currents out of the mirrors are going to be the same. More precisely, the current provided by the top mirror ($I_{OUT}^+$) will be hair pile equal to the required current (incoming) by the bottom mirror ($I_{OUT}^-$).

The result of all this is that the current circulating in the $R_{OUT}$ resistance will be zero, since everything provided by Q7 is fully eaten by Q9, and no crumbs of current are allowed to escape through $R_{OUT}$. And who says running zero in a resistance means zero tension at its limits. Thank you Herr Ohm. This makes the module output voltage zero at rest. This famous zero offset.

Well, so far, we've assumed - correctly - that exactly the same thing is happening in the other part of the circuit, the one on the right. Everything is strictly the same, the offset output is zero, etc... But now, we're going to have to roll up our sleeves and tackle the differential, we're not going to be able to do without.

**- Things are moving... A little.**




We're just going to do a little simplified reminder about what's going on in these mysterious differential pairs. That the purists forgive me, but we will not go into too much detail, it is not necessary here. And then we ate enough equations for now.

On the small diagram, a sleek version of the differential pair, more than enough to understand.

At rest (without signal, $V_1 = V_2 = 0$), the two JFets being identical, the values of the resistances also, the two currents $I_1$ and $I_2$ are equal.

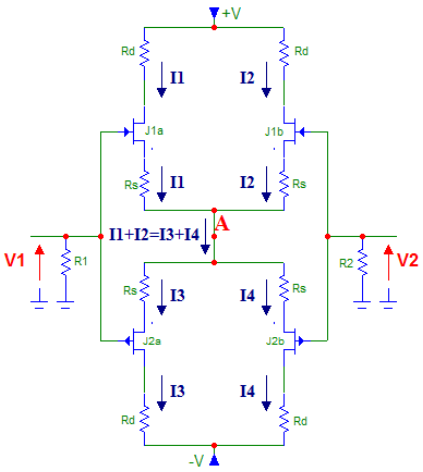
If now we apply a non-zero $V_1$ voltage (positive for example), and $V_2$ remains the same (no to simplify), we will decrease the $V_{GS}$ of J1a (I remind you that $V_{GS}$ is negative for a JFet N, and therefore $V_{GS}$ becomes less negative if $V_G$ increases). In doing so, we will automatically increase the current of drain $I_1$ (refer to the equation (4)...)

If we increase $I_1$, the voltage at the $R_{S1}$ terminals ($R_{S1}I_1$) will change, and therefore change the voltage on $R_{S2}$ where it is connected to $R_{S1}$ (point A on the diagram). And since we didn't touch $V_2$, the second JFet J1b must manage to pass on this change of balance. And the only way he knows for this is to change the current that crosses it ($I_2$) so that the voltage drop between his grid and point A, or ($V_{GS2}$ -$R_{S2}I_2$) catches up with the change that has just taken place. And so, the second JFet has no other resource than to decrease $I_2$ to restore the balance of potentials. And since we assume that we are in linear operation of the differential pair, what the current $I_1$ has gained in relation to its resting position, is exactly what $I_2$ has just lost ... In other words, $I_1$ changes to $I_1$ - $I$ and $I_2$ to $I_2$ - $I$, but the sum $I_1$ - $I_2$ remains constant.

In summary - and simplifying - if the current in one branch of the differential pair increases, the current in the other branch decreases, and vice versa, but the total current ($I_1$ - $I_2$) remains constant (one is linear, at least we hope...) Okay, it's electronics with your hands, but it's more than enough for us to understand what's next.

So back to our UGS, with its pair of differential pairs. Well it's almost the same, with a few more gadgets ... If we take a simplified diagram of the first section (still no cascodes, mirrors, or counter reaction), we can see it like:

We start as usual now with the situation at rest, in the absence of an entry signal ($V_1 = V_2 = 0$).




It is still assumed that transistors and resistances are the same. We are then obliged to think that all currents are equal in each of the branches ($I_1 = I_2 = I_3 = I_4$).

In addition, we have just seen that the current passing through point A was constant ($I_1 + I_2$ *or* $I_3 - I_4$), but this is also valid if one is not at rest (in the presence of signal).

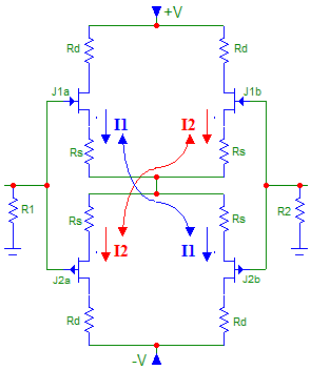
Let's take a little care of what happens when we apply a signal. We will assume as before that we change $V_1$ to make it become slightly positive, and that $V_2$ remains wisely at 0.

If $V_1$ thus becomes positive, we saw that the current $I_1$ was going to increase, and that therefore $I_2$ would decrease, while keeping the amount $I_1$ - $I_2$ constant. But if $V_1$ increases, it will also have an influence on the lower differential pair, since it shares the same input.

Indeed, $V_1$ increasing, the $V_{GS}$ of J1a will imbuing (the gap between $V_G$ and $V_S$ - the latter is positive, I remind you - decreases for the JFet J1a), but the $V_{GS}$ of J2a will increase ($V_S$ is negative compared to $V_G$ for the JFet), but the $V_{GS}$ of J2a will increase ($V_S$ is negative compared to $V_G$ for the JFet J2a, and so we increase the difference between the two). So the $I_3$ current in J2a will also decrease. And to conform to its differential pair destiny, J2b will increase the current crossing it, and thus $I_4$ increases.

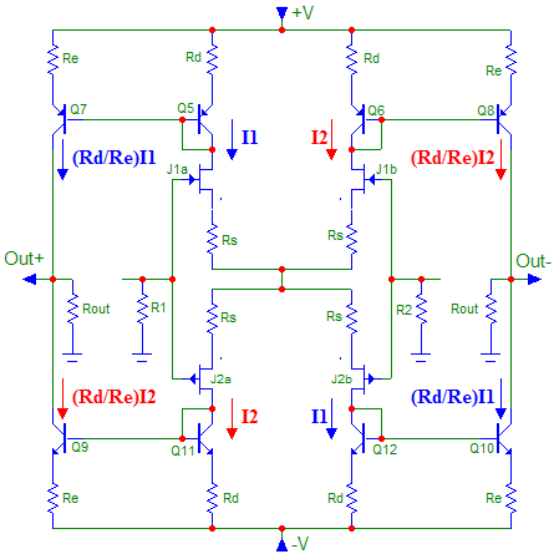
So we find ourselves in front of the next diabolical "chain". Is $V_1$ going up? Is $I$ up? $I_2$ decreases? Is $I_3$ also decreases? And $I_4$ increases? (The term "chaining" is a bit abusive, since in reality everything happens at the same time. But if you find me a better picture, I'm a taker).

But since $I_3$ - $I_4$ must remain constant, and there is no other solution than to keep this sum equal to $I_1$ - $I_2$ , one can only arrive at the result that the diametrically opposed currents (on the diagram) are the same: ***$I_1 = I_4$ and $I_2 = I_3$***.




So in short, we find exactly the same currents in each of the branches of the two differential pairs, but the branches in which they circulate are inverted between the "top" and the "bottom," as in the diagram opposite.

This will have interesting consequences for the UGS. Indeed, if we go back to the whole scheme, always without the cascodes and counter-reactions.




It may seem a bit complex at first glance, but nothing scary. We find our currents crossed out, just to the amplification factor of the current mirrors close.

So what happens on the way out, you'll tell me... At rest, as we have seen, all currents in the branches are equal ($I_1 = I_2$).

Now, if as usual it is assumed that $V_1$ increases, $I_1$ will increase too and $I_2$ will decrease. This means that, for example, the current provided by Q7 is going to be larger than what Q9 demands. And this is where R OUT intervenes, to take charge of the difference between these two currents and create tension from this difference of currents:

(15)

$$V_{OUT}^{+} = R_{OUT}\frac{R_D}{R_E}(I_1 - I_2)$$

One of the beauties of the thing is that on the other side of the UGS, it happens exactly the same, but reversed:

(16)

$$V_{OUT}^{-} = R_{OUT}\frac{R_D}{R_E}(I_2 - I_1) = -V_{OUT}^{+}$$

Each exit of the UGS therefore reproduces the same thing, but what is positive on the one hand becomes negative on the other, and High School of Versailles (vice versa for young people ...). Or in other words, the output signals are out of phase by 180 degrees. So we actually made a nice little symmetry, starting from three times nothing.

Okay, it's really overwhelming, but if you've pretty much followed everything so far, you should be able to find yourself there without too much trouble, or else it's time to take an aspirin and break before attacking the sequel.

**- Gain to grind.**

So far, we've mostly focused on the resting point of the device, and we haven't really talked about winning, although we're starting to get a little idea. But for the operation of the differential pair, we began to vary a little the voltages of inputs, which will naturally lead us to the behavior of the assembly in the presence of a signal.

This input signal will be symbolized by a small variation in the grid spring voltage around the resting point. So we're going to write *UGS* = $V_{GS}$ + $v_{gs}$ where UGS is the total grid-source voltage, consisting of the overlay of the $V_{GS}$ rest voltage and the signal to be amplified $v_{gs}$.

If we introduce all this beautiful world into the equation (4) we will get for the drain current of a JFet:

$$I_D = I_{DSS}\left(1 - \frac{U_{GS}}{V_{GSOff}}\right)^2 = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GSOff}} - \frac{v_{gs}}{V_{GSOff}}\right)^2$$

In other words:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GSOff}}\right)^2 - 2\frac{I_{DSS}}{V_{GSOff}}\left(1 - \frac{V_{GS}}{V_{GSOff}}\right)v_{gs} + \frac{I_{DSS}}{V_{GSOff}^2}v_{gs}^2$$

We find with an undisguised surprise our current at rest:

$$I_{DSS}\left(1-\frac{V_{GS}}{V_{GSOff}}\right)^2$$

but also a term that contains our input signal:

$$-2\frac{I_{DSS}}{V_{GSOff}}\left(1-\frac{V_{GS}}{V_{GSOff}}\right)v_{gs}+\frac{I_{DSS}}{V_{GSOff}^2}v_{gs}^2$$

It is therefore safe to write that the total drain current $I_D$ is also the overlay of an $I_{DR}$ resting current and a variable current depending on the input signal $i_d$:

$$I_D = I_{DR} + i_d$$

Thanks to our unmatched performance in mathematics, we now know the first, so we will take care of the second:

(17)

$$i_d = -2\frac{I_{DSS}}{V_{GSOff}}\left(1-\frac{V_{GS}}{V_{GSOff}}\right)v_{gs}+\frac{I_{DSS}}{V_{GSOff}^2}v_{gs}^2$$

The terms $V_{GSOff}$ and $I_{DSS}$ are constituent parameters of the JFet, and the $V_{GS}$ quantity is fixed by the polarization of the mount (resting point), so that the terms involving them can be considered constants ($i_d$ - $A.v_{gs}$ - $B.v_{gs}^2$). But we find ourselves right away in front of a bug ... The term in $v_{gs}^2$ is very em... betant for us, fanatics of linearity and zero distortion, since it is precisely the term that will introduce distortion.

Indeed, imagine that $v_{gs}$ is a beautiful sinusoidal signal, like Again, $sin(2\pi f_o t)$ refer to your favorite trigonometry formulas, but raising this sine signal squared means that we will see a double frequency of input frequency in the drain current: . The JFet has therefore $sin(4\pi f_o t)$ the signal and created harmonic distortion (or 2nd order).

Fortunately, if one keeps a relatively small $v_{gs}$ excursion, the term in $v_{gs}^2$ remains negligible in front of the first order, so that one can approximate the drain current of the JFet as:

$$i_d = -2\frac{I_{DSS}}{V_{GSOff}}\left(1-\frac{V_{GS}}{V_{GSOff}}\right)v_{gs}$$

To avoid overly manipulating terms, we will reduce this equation in the much simpler form of:

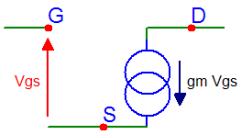
(18)

$$I_d = g_m v_{gs}$$

Where $g_m$ is the famous transconductance of the JFet… ta da. For the record, $i_d$ is a variation of current around the resting point, and $v_{gs}$ a variation in input voltage around the same resting point. This transconductance therefore translates the variation of the current passing through the transistor according to the variation of grid/source voltage. That's it.

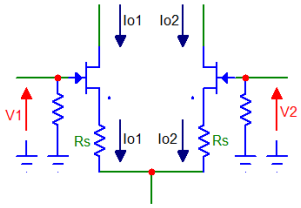
That's fine. What do we do now?

Well, we'll start by saying that finally, with signals of low amplitude, the equation (18) shows us that the JFet behaves like a current generator (the drain-source current) controlled in voltage (grid-source voltage). We will therefore simplify the JFet to give its simplified equivalent "small signals" scheme, which looks roughly like this:

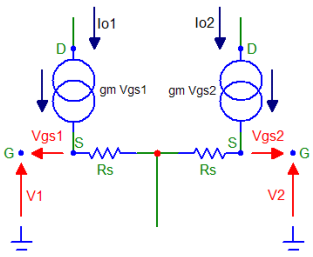



There are the three Grid/Drain/Source connections, and the power generator controlled by your grid/source voltage. This type of pattern is only valid with variable (alternative) signals of low amplitude, and presupposes that the circuit is properly polarized and everything and everything. Again, there is no continuous component on this scheme, just alternative signals, or music, as you prefer. We're well advanced, aren't we?

Well, I do, though. If we take the diagram of the upper input differential pair of our favorite UGS (as usual, we ignore the mirrors and cascodes).




We replace the JFets with their equivalent model to finally arrive at the right diagram ... It was assumed here that all JFets were the same (the same $g_m$ everywhere) so as not to get emberlificoter in the equations.




Good eh... We will try to find the currents Io1 and Io2 depending on the tensions of input V1 and V2 ... We roll up our sleeves, and we start with the easiest of course:

$$I_{O1} = g_m V_{GS1} \quad \text{And} \quad I_{O2} = g_m V_{GS2}$$

so much so that:

(19)

$$I_{O1} - I_{O2} = g_m (V_{GS1} - V_{GS2})$$

Now, if we go through the "simplified" diagram from one grid to another - attention to the meaning of currents - we can write:

$$V_1 = V_{GS1} + g_m V_{GS1} R_S - g_m V_{GS2} R_S - V_{GS2} + V_2$$

As a result:

(20)

$$V_1 - V_2 = (V_{GS1} - V_{GS2})(1 + g_m R_S)$$

If we now make the relationship between the difference between differential output currents and differential input voltages, and thus the ratio (19)/(20), we find, to a few things, the equation of differential gain of a pair at JFet:

(21)

$$G_D = \frac{I_{O1} - I_{O2}}{V_1 - V_2} = \frac{g_m}{1 + g_m R_S}$$

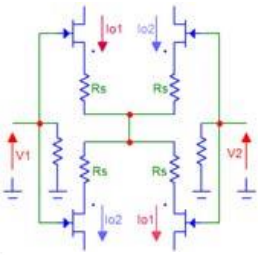
Now, as it has been assumed that the two JFets are identical, it is reasonable to assume that the two currents are evenly distributed, half each. And what does that mean, that convoluted phrase? Well, we have the following relationships:

(22)

$$G_1 = \frac{I_{O1}}{V_1 - V_2} = \frac{1}{2} \frac{g_m}{1 + g_m R_S} \quad \text{and} \quad G_2 = -\frac{I_{O2}}{V_1 - V_2} = \frac{1}{2} \frac{g_m}{1 + g_m R_S} \quad \text{with} \quad G_D = G_1 + G_2$$

$G_1$ and $G_2$ are $G_D$ asymmetric gains and differential gain.

We have therefore just obtained a relationship between the currents circulating in each of the "top" JFets and the differential tension of entry. This is what I have miscalled gain, but in fact it is a transconductance (in A/V). But we still don't know what's going on in the bottom JFets.




Well, yes, actually. If we take a look at page 7, we will see that the current in the top left branch is the same as that in the branch of the bottom right, and vice versa (the famous shot of the cross currents). So we end up with the simplified diagram against it.

Based on the relationships just above (22), we have:

$$I_{O1} = G_1 (V_1 - V_2) = \frac{1}{2} \frac{g_m}{1 + g_m R_S} (V_1 - V_2) \quad \text{and} \quad I_{O2} = -G_2 (V_1 - V_2) = -\frac{1}{2} \frac{g_m}{1 + g_m R_S} (V_1 - V_2)$$

When we got there, we did the hard part. We know that these two currents will pass through the current mirrors and the ROUT resistance to give rise to exit tensions. So we go back a few pages, until the equations (15) and (16), which give us a relationship between the currents in the JFets and the output tension on one side of the UGS, as being proportional to the difference in currents in JFets from the top and bottom:

$$V_{OUT}^{+} = R_{OUT}\frac{R_D}{R_E}(I_{O1} - I_{O2}) \quad \text{and} \quad V_{OUT}^{-} = -R_{OUT}\frac{R_D}{R_E}(I_{O1} - I_{O2})$$

So we replace $I_{O1}$ and $I_{O2}$ by their values, and we get:

(23)

$$V_{OUT}^{+} = R_{OUT}\frac{R_D}{R_E}\frac{g_m}{1+g_m R_S}(V_1 - V_2) \quad \text{and} \quad V_{OUT}^{-} = -R_{OUT}\frac{R_D}{R_E}\frac{g_m}{1+g_m R_S}(V_1 - V_2)$$

Which brings us to:

$$V_{OUT}^{+} - V_{OUT}^{-} = 2R_{OUT}\frac{R_D}{R_E}\frac{g_m}{1+g_m R_S}(V_1 - V_2)$$

or finally in this form:

(24)

$$A_D = \frac{V_{OUT}^{+} - V_{OUT}^{-}}{V_1 - V_2} = 2R_{OUT}\frac{R_D}{R_E}\frac{g_m}{1+g_m R_S}$$

What we have here is the differential gain formula of the UGS. Attention, it is an open loop gain, that is to say without any resistance of counter-reaction. To be concrete, the *gm* of the JFets is in the order of 25mS in the ladle - your mileage may vary, and with the resistance values used, we arrive at an open loop differential gain of the order of 46 V/V, or 33.25 dB. This is very low compared to modern operational amps for example, for which this gain turns around 100,000 V/V at least ...

Just one last word before complicating things. We started on the fact that the two $R_{OUT}$ resistances are equal. However, we do not have to do so, and for the sake of generality, we can assume that these two resistances are different. By posing that one has a resistance $R_{OUT}$ - and on the side of the positive output and $R_{OUT}$ - for the negative output, one can rewrite the relationship (23) as:

(25)

$$A^{+} = \frac{V_{OUT}^{+}}{V_1 - V_2} = R_{OUT}^{+}\frac{R_D}{R_E}\frac{g_m}{1+g_m R_S}$$

And

(26)

$$A^{-} = -\frac{V_{OUT}^{-}}{V_1 - V_2} = R_{OUT}^{-}\frac{R_D}{R_E}\frac{g_m}{1+g_m R_S}$$

where $A^{+}$ and $A^{-}$ are the two asymmetrical open loop gains (these are positive numbers), which gives us for the open loop differential gain:

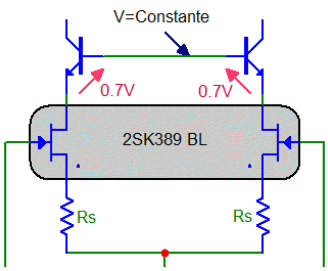
(27)

$$A_D = A^{+} + A^{-} = \frac{V_{OUT}^{+} - V_{OUT}^{-}}{V_1 - V_2} = (R_{OUT}^{+} + R_{OUT}^{-})\frac{R_D}{R_E}\frac{g_m}{1+g_m R_S}$$

**- Cascode Break?**

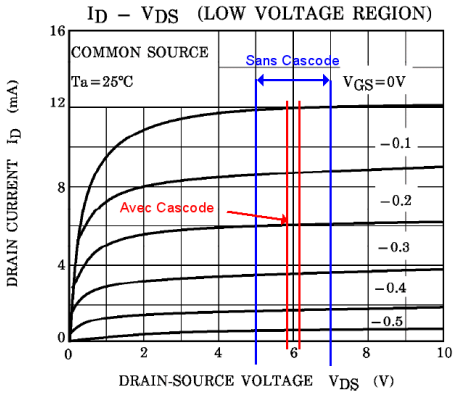
Before going any further, we will open a small bracket to get past the cascodes in a hurry, and without dwelling, otherwise it's going to be too hot ... There is no ideal place to talk about it, because they intervene both at the resting point and during the operation in the presence of the signal, so we might as well get rid of them now...

Cascodes, therefore, are "just" transistors (bipolar here) serially inserted into the drains of the JFets. Their base is maintained at a constant potential across a divider bridge (refer to the full diagram). As the potential of the base is constant (and in the order of 10V for the UGS), the potential of the transmitters will also be fixed, and will be worth in the 0V7 less than the potential of the bases. This ultimately means that the drains of the JFets will be at a constant potential. The $V_{GS}$ of the JFets in normal operation is relatively low (well below the volt), so it will be said quickly that the $V_{DS}$ voltage at the JFets terminals remains stable, or at least varies very little.




This little thing of nothing at all is going to have three very interesting consequences. First, as the voltage at the JFets terminals remains within 10V, it means that we have decreased the power dissipated in the JFets: At rest for example, for a current of 3.5mA, a JFet will dissipate 35mW, while without cascode, it should dissipate more than 65mW. So we gained overall thermal stability.

On the other hand, as the $V_{DS}$ is almost constant, this will have the effect of linenizing the behavior of the JFet. If we extract from the datasheet of 2SK389 the following graph:




This represents the current drain according to the voltage $V_{DS}$, and this for several voltages of $V_{GS}$ . On this graph I assumed for convenience that the cascode voltage was around 6V (compared to 10V in reality). For an ideal transistor, the different "straight" $V_{GS}$ =cste would be parallel and zero slope. In reality, they are not, and the slope is not zero. This means that if the voltage of the JFet drain varies, the jFet's drain current will also vary... And what's the problem, you'll tell me? Well, it is that we would like the drain current of the JFet to depend only on the input voltage, and not anything else. (I remind you that we were asked $i_d = g_m . v_{gs}$)

The cascode, by fixing the drain potential, thus minimizes this "non-linearity" and works on a much narrower part of these curves (in the red zone), where one can consider that one will have a variation of the negligible drain current in $V_{DS}$ function.

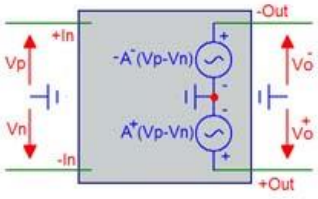
Ok then. Purists will tell me that it is $V_{DS}$ that must be maintained constant, not just the drain voltage, as we do in the hope that the source voltage does not move too much. It's true. But I didn't want to break my head, and you're free to try both versions, after all.

With all this, I was going to forget to tell you about the latest beneficial effect of cascode, the extension of bandwidth. Be is about the same phenomenon as what we just saw, except that there, instead of the current drain, it is the parasitic abilities of the JFet that depend on the V DS (take the datasheet). By minimizing the variation in drain-source voltage, non-linearities due to these variable voltage abilities are reduced. Because these capas are weak, they occur mainly at the top of the spectrum, and by making them less involved, the high-frequency behavior of the JFet is improved. Okay, again it's outrageously simplified, but it improves our general culture and our understanding of editing at the same time.

So to end the break, what if we go back to our sheep?

**- Counter-Reaction Engine.**

Just before letting the UGS coddle with the counter-reactionary powers, we will drop the transistors and simplify the scheme by establishing an equivalent of open loop assembly, which could give us that for example:



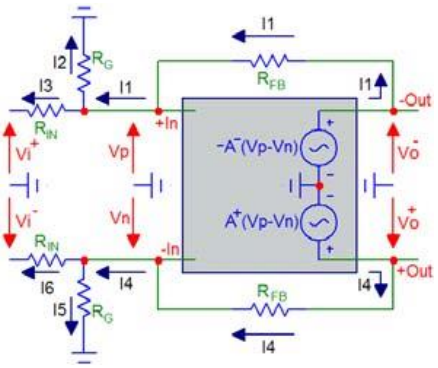

It's hard to make it any simpler. Two entry tensions, two exit tensions, and gain. The tensions shown here are referenced in relation to the mass, and they are linked by the following relationships:

(28)

$$\begin{cases} V_O^+ = A^+\left(V_p - V_n\right) & A^+ > 0 \\ V_O^- = -A^-\left(V_p - V_n\right) & A^- > 0 \\ V_O^+ - V_O^- = A_D\left(V_p - V_n\right) \end{cases}$$

where $A_D$ is the famous open loop differential gain, given by the equation (27). On the other hand, it is assumed - with good reason - that the currents entering the UGS are zero, which is far from being far-fetched given the enormous impedance of entry of the JFets (the grid current is negligible). It is also worth noting the two grid resistances (those between the JFets grids and the mass) are not included in the equivalent scheme. We're going to need it later.

We are now ready to put the counter-reaction in place. With the simplified pattern of the open loop UGS, it's going to get us pretty much topology opposite:




First of all, let's put things back: $R_{FB}$ and $RI_N$ are counter-reaction resistances, and RG is the grid resistance of the JFets, (47K at home). $V_i^+$ and $V_i^-$ are our input tensions, what we actually send into the editing, and $V_o^+$ and $V_o^-$ are of course our output tensions. A quick reminder: no current enters the UGS...

So let's go ... We already know that by definition:

(29)

$$V_O^+ - V_O^- = A_D\left(V_p - V_n\right), \quad \text{In other words} \quad V_p - V_n = \frac{V_O^+ - V_O^-}{A_D}$$

One can also write:

$$V_p + R_{FB} I_1 = V_O^-$$

and

$$V_n + R_{FB} I_4 = V_O^+$$

From this it is easy to conclude with:

$$V_p - V_n = \left(V_O^- - V_O^+\right) + R_{FB}\left(I_4 - I_1\right)$$

If we replace $V_p$-$V_n$ by the relationship given by (29), we finally get:

(30)

$$I_4 - I_1 = \frac{1 + A_D}{R_{FB} A_D}\left(V_O^+ - V_O^-\right)$$

Another ladle from Ohm/Kirchhoff to write several little things we're going to need:

$$I_2 = V_n / R_G \quad \text{and} \quad I_3 = I_1 - I_2 = I_1 - V_n / R_G$$

Similarly

$$I_5 = V_p / R_G \quad \text{and} \quad I_6 = I_4 - I_5 = I_4 - V_p / R_G$$

We will now travel the LED circuit out to the entrances:

$$V_O^- = R_{FB} I_1 + R_{IN} I_3 + V_I^+$$

and

$$V_O^+ = R_{FB} I_4 + R_{IN} I_6 + V_I^-$$

A term-to-term difference and a few manipulations later, and we arrive at:

$$V_O^+ - V_O^- = \left(R_{FB} + R_{IN}\right)\left(I_4 - I_1\right) + \frac{R_{IN}}{R_G}\left(V_p - V_n\right) + V_I^- - V_I^+$$

Again, $V_p$-$V_n$ is replaced by (29). I'm making you thanks from the intermediate steps, but using the few equations above, you finally get:

(31)

$$I_4 - I_1 = \frac{V_O^+ - V_O^-}{R_{FB} + R_{IN}} \frac{A_D R_G - R_{IN}}{A_D R_G} + \frac{V_I^+ - V_I^-}{R_{FB} + R_{IN}}$$

Replacing $I_1$-$I_4$ of (31) with its value given by the equation (30), we finally end up with something like:

$$V_I^+ - V_I^- = \left(V_O^+ - V_O^-\right) \frac{R_{IN}\left(R_{FB} + R_G + A_D R_G\right) + R_G R_{FB}}{A_D R_G R_{FB}}$$

And to the joy of victory against mathematical adversity, one gets the differential gain of the UGS counter-reactioned, i.e:

(32)

$$G_D = \frac{V_O^+ - V_O^-}{V_I^+ - V_I^-} = \frac{A_D R_G R_{FB}}{R_{IN}\left(R_{FB} + R_G\left(A_D + 1\right)\right) + R_G R_{FB}}$$

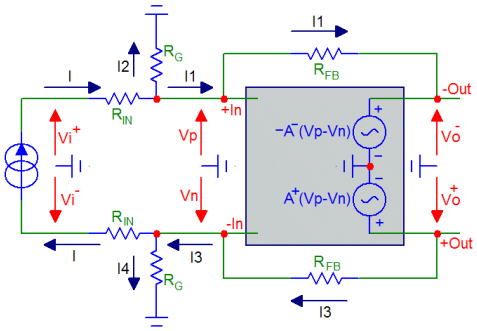
With the values used in our application, and by counting on open loop gain (A) of 46, we get a differential gain of 3.3, or 10.4 dB. The gain in asymmetric (tension of an output on the differential voltage of input) is half $G_D$ , or 1.65 or 4.4 dB.

We've done a lot of work, right? But don't rest too fast, there's still work to be done. We are very hot and there are still a lot of things to calculate Like the impedances of entry and exit, for example. Are you interested?

**- Impedance (Angl.) impedio, -ire, impediui, impeditum: obstructing, preventing.**

A little discouraging, as a start…

Don't panic, everything's going to be fine. And we'll start with the simplest, the input impedance. For this we will need a small diagram to visualize what we do.




We haven't changed much since the last time. We just added a power generator as an input. What for? Well to do what you do in real life, when you use an ohmmeter. Indeed, when one measures a resistance to the multimeter, the same thing happens: the multi injects a known current into the resistance, and it measures the tension developed at the limits of the resistance. As the current we send is known, a simple law of Ohm allows to find this damn resistance (R-V/I). And well, it's the same: we're going to inject into our circuit an imposed current whose value we contradict, and "measure" the voltage at the generator terminals.

This tension is ($V_i^+$ - $V_i^-$), which gives us input impedance like:

$$Z_{IN} = \frac{V_I^+ - V_I^-}{I}$$

As usual, we have the relationships now classic:

(33)

$$V_O^+ = A^+\left(V_p - V_n\right) \qquad V_O^- = -A^-\left(V_p - V_n\right) \qquad V_O^+ - V_O^- = A_D\left(V_p - V_n\right)$$

We start by involving Mister Ohm for tensions:

$$I_2 = \frac{V_p}{R_G} \quad \text{and} \quad I_4 = \frac{V_n}{R_G}$$

And then we'll have to think about paying A Few Extra Hours to Mr. Kirchhoff, since again he's going to step in:

$$I = I_1 + I_2$$

and

$$I = I_3 - I_4$$

Which, of course, makes it, given the relationships just above:

(34)

$$I_1 + I_3 = 2I + \frac{1}{R_G}\left(V_n - V_p\right)$$

Starting from the exits and going to the mass, we can also write:

$$V_O^- = -R_{FB}I_1 + V_p \quad \text{and} \quad V_O^+ = -R_{FB}I_3 + V_n$$

Where:

$$V_O^+ - V_O^- = R_{FB}\left(I_1 + I_3\right) + \left(V_n - V_p\right)$$

The term ($I_1$+$I_3$) is replaced by the relationship (34), which leads us to:

$$V_O^+ - V_O^- = \frac{R_{FB} + R_G}{R_G}\left(V_n - V_p\right) + 2R_{FB}I$$

and if we replace ($V_o^+$-$V_o^-$) with its equivalent drawn from (33), it gives us:

(35)

$$V_p - V_n = \frac{2R_{FB}R_G}{R_{FB} + R_G\left(A_D + 1\right)}I$$

If we now attack the problem from the west side:

$$V_i^+ = R_{IN}I + V_p \quad \text{and} \quad V_i^- = -R_{IN}I + V_n$$

Where:

$$V_p - V_n = V_i^+ - V_i^+ - 2R_{IN}I$$

So we take back our equation (35) and replace $V_n$-$V_p$ with what we just found just above, and we can easily get that out of it:

$$V_i^+ - V_i^- = \left(2R_{IN} + \frac{2R_{FB}R_G}{R_{FB} + R_G\left(A_D + 1\right)}\right)I$$

This relationship between the differential tension of entry and the current, well that's just what we're looking for: our differential input impedance. And more precisely it's worth:

(36)

$$Z_{IN\,D} = 2R_{IN} + \frac{2R_{FB}R_G}{R_{FB} + R_G\left(A_D + 1\right)}$$

Interestingly, this differential impedance depends on the open loop differential gain ($A_D$), but does not depend on asymmetric gains, so the input impedances seen between any input and mass will be equal, no matter what asymmetrical gains:

(37)

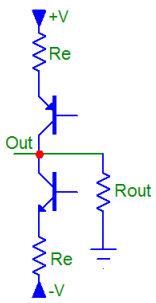
$$Z_{IN\,A} = R_{IN} + \frac{R_{FB}R_G}{R_{FB} + R_G\left(A_D + 1\right)}$$

For the digital application, it goes by itself, and with our values, we find a differential $Z_{IN}$ of about 32k, and therefore an impedance of input on each branch of 16k. The second term of the equation (36) is small in front of $R_{IN}$, even with our "low" gain value an open loop, so we can approximate the differential input impedance by $2R_{IN}$. All for that...

And finally, you see that you've followed, and that it doesn't break three legs to a transistor, these calculations. Will it be the same for the output impedance? Of course. You'll see.

**- Damn dice $Z_{out}$**

Before tackling this piece, we will have to go back to the bowels of the UGS. Indeed, we need to know his impedance of open loop output. We're not going to go too deep into the thing, but if we look at one of the exit floor of the UGS, we can equate it with two bipolar transistors mounted in a common transmitter and put head spade.



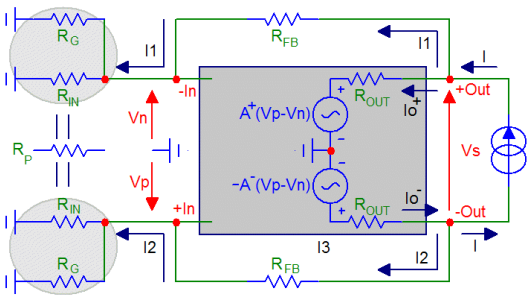

The impedance of exit of a floor with a common transmitter in the absence of charge is grossly given by the reverse of its admittance of output $h_o$, namely:

$$Z_{OEC} \approx \frac{\left|V_A\right|}{I_C}$$

Where I C is the collector current and V Has early voltage. This last parameter is determined by the construction of the bipolar transistor, and is worth between a few dozen and a few hundred Volts.

The collector current being in the order of a few mA, we immediately see that the output impedance of this type of stage is very large (nearly 40K in our case). Okay, alternatively, the two floors in common transmitter are found in parallel, which divides the output impedance by two. So we've got about 20 K's output impedance in Rout's absence. If we add this famous $R_{OUT}$, we come to put it in parallel on these 20 K, and as $R_{OUT}$ is low compared to these 20K, we do not make a big mistake saying that the output impedance of the UGS open loop is equal to $R_{OUT}$, or 1K. This value is the asymmetrical output impedance, and the symmetrical (or differential) output impedance is therefore doubled, which makes us a $Z_{OUT}$ of 2K.

Now we have everything we need to calculate the output impedance in the presence of counter-reaction. All we need is a diagram to visualize what we are doing. So here it is:




We took the equivalent pattern of the UGS, and we just changed one or two things by the way. For example, tensions on each exit were abandoned in favour of differential tension $V_S$ . The $R_{OUT}$ resistances that appear in series with the equivalent voltage generators (Thevenin) of the UGS are the two asymmetrical output impedances in open loop, as we have just seen. There is also the counter-reaction network ($R_{FB}$, $R_{IN}$ and $R_G$ ) that we have seen previously. However, the entries have been linked to the mass, but this is simply due to the definition of output impedance:

$$Z_O \equiv \left.\frac{V_S}{I}\right|_{V_{IN}=0}$$

And the current generator is exactly the same technique as for input impedance, the ohmmeter method: you inject an I current into the circuit and measure the $V_S$ voltage at the impedance terminals. No more complicated than that.

So let's go for the equations. To simplify the writing, we will first define an $R_P$ resistance that is equal to the paralleling of $R_{IN}$ and $R_G$:

$$R_P = \frac{R_G R_{IN}}{R_G + R_{IN}}$$

We start by going from the $OUT^+$ terminal to the mass by two different paths:

$$(R_{FB} + R_P)I_1 = V_S + (R_{FB} + R_P)I_2$$

And that brings us to:

(38)

$$I_1 - I_2 = \frac{V_S}{R_{FB} + R_P}$$

Ohm's law again between the terminals 'IN' or 'IN', we write:

$$V_n = R_P I_1$$

and

$$V_p = R_P I_2$$

so, logically it becomes:

$$V_p - V_n = R_P(I_2 - I_1)$$

We re-inject the equation (38) in there to get:

(39)

$$V_p - V_n = -\frac{R_P V_S}{R_{FB} + R_P}$$

Kirchhoff is still annoyed on the currents at the nodes -OUT and -OUT:

(40)

$$I_1 = I - I_O^+ \quad \text{and} \quad I_2 = I_O^- - I$$

Kirchhoff still, but in tension to go from the out bound to the mass:

$$A^+\left(V_p - V_n\right) + R_{OUT} I_O^+ = \left(R_{FB} + R_P\right) I_1$$

In the expression above, we replace both $I_1$ with its equivalent given by (40) and $V_p$-$V_n$ by (39), which gives us:

$$-\frac{A^+ R_P V_S}{R_{FB} + R_P} + R_{OUT} I_O^+ = \left(R_{FB} + R_P\right)\left(I - I_O^+\right)$$

We put all the terms together in the right order, and finally we get to:

(41)

$$I_O^+ = \frac{1}{R_{OUT} + R_{FB} + R_P}\left[\left(R_{FB} + R_P\right) I + \frac{A^+ R_P}{R_{FB} + R_P} V_S\right]$$

The exact same thing is now being done for the tension between THE OUT and the mass:

$$-A^-\left(V_p - V_n\right) - R_{OUT} I_O^- = \left(R_{FB} + R_P\right) I_2$$

Again, we replace in this expression both $I_2$ by its equivalent given by (40) and $V_p$-$V_n$ by (39), which gives us:

$$\frac{A^- R_P V_S}{R_{FB} + R_P} - R_{OUT} I_O^- = \left(R_{FB} + R_P\right)\left(I_O^- - I\right)$$

Re-manipulation and new equation:

(42)

$$I_O^- = \frac{1}{R_{OUT} + R_{FB} + R_P}\left[\left(R_{FB} + R_P\right) I + \frac{A^- R_P}{R_{FB} + R_P} V_S\right]$$

We are almost there, but before, a final step: we express the tension between the knot and the mass through the paths that we have not already explored, that is to say through the interior of the UGS:

$$A^+\left(V_p - V_n\right) + R_{OUT} I_O^+ = V_S - A^-\left(V_p - V_n\right) - R_{OUT} I_O^-$$

Where:

$$V_S = \left(A^+ + A^-\right)\left(V_p - V_n\right) + R_{OUT}\left(I_O^+ + I_O^-\right) = A_D\left(V_p - V_n\right) + R_{OUT}\left(I_O^+ + I_O^-\right)$$

Using the value of $V_p$-$V_n$ given in (39) and the values of currents $I_O$ of (41) and (42), one finds after many efforts:

$$V_S\left(R_{OUT} + R_{FB} + R_P\left(A_D + 1\right)\right) = 2R_{OUT}\left(R_{FB} + R_P\right) I$$

Well, we're almost there, aren't we? The $V_S/I$, ratio is the output impedance we are looking for. And zou, quickly, we find:

$$Z_{OUT} = \frac{2R_{OUT}\left(R_{FB} + R_P\right)}{R_{OUT} + R_{FB} + R_P\left(A_D + 1\right)} \qquad \text{with} \qquad R_P = \frac{R_G R_{IN}}{R_G + R_{IN}}$$

If we replace $R_P$ by its value according to $R_G$ and $R_I$, we finally arrive at:

(43)

$$Z_{OUT} = \frac{2R_{OUT}\left(R_{FB} R_G + R_{FB} R_{IN} + R_G R_{IN}\right)}{\left(R_{OUT} + R_{FB}\right)\left(R_G + R_{IN}\right) + R_G R_{IN}\left(A_D + 1\right)}$$

and the asymmetrical output impedances are equal to half of $Z_{OUT}$.

A little complicated certainly ... With our values, we get a differential output impedance of 228Ω. That is pretty much what has been measured, so it is not silly. The output impedance of each branch (asymmetrical) is worth half of the differential impedance, or 114Ω. Well, here we go pretty much around the thing, and you've got everything you need to have fun experimenting. But as we are curious, we can still try to take a look at how the values of the various resistances of counter-reaction influence the different parameters that we have just established.

**- What does what?**

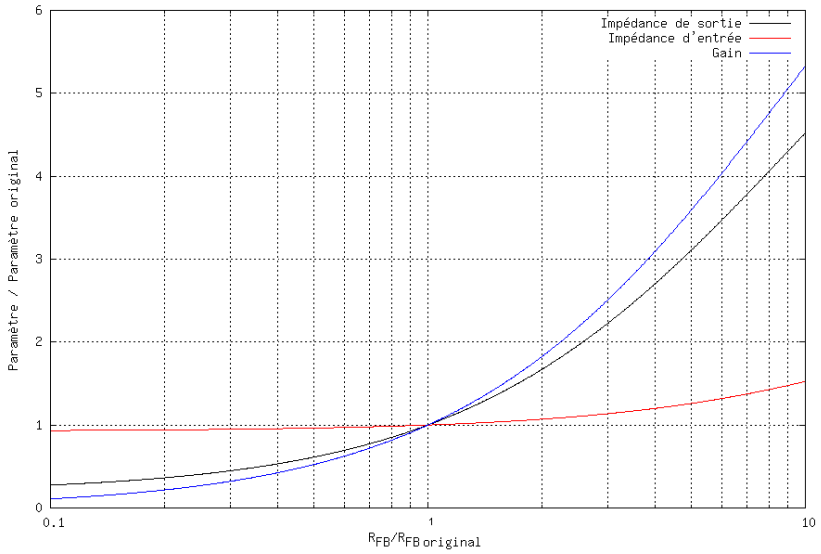
By taking up the equations of output impedance and gain (all differential), we can have fun varying one of the resistance values $R_G$, $R_{IN}$, $R_{FB}$ and $R_{OUT}$ , and look at what happens to our parameters.

The procedure is as follows: we take our starting values ($R_G$ = 47k Ω , $R_{IN}$ - 15kΩ, $R_{FB}$ - 56k Ω, $R_{OUT}$ -1kΩ), and we calculate the parameters $G_D$, $Z_{IN}$ and $Z_{OUT}$ for these starting values. One of these resistance values is exchanged from 1/10 th of the original value to 10 times the value, with the other resistances retaining their original value. For $R_{IN}$, for example, its value will vary between 1.5kΩ and 150k Ω, and we calculate $G_D$, $Z_{IN}$ and $Z_{OUT}$ that we normalize compared to the original value. OK, it's a bit convoluted as a technique, but it allows for more direct comparisons.

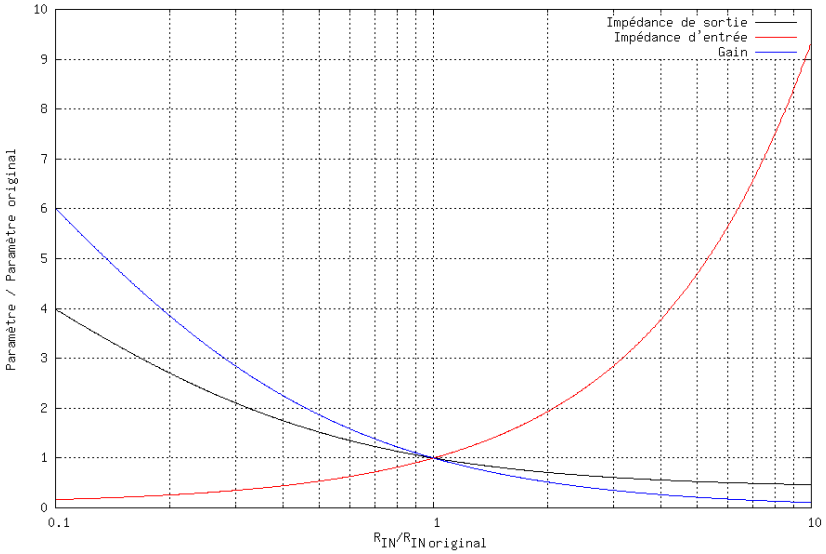
Simone, first candidate please. It's $R_{FB}$ that shows up, and it gives the next figure.

First, $R_{FB}$ has very little influence on input impedance, but it was already suspected. We also suspected that if we increased $R_{FB}$, we would do the same for the gain. But we see there that it is done at the expense of the output impedance that also increases, and quite similar to the gain: if you quadruple $R_{FB}$, the gain triples, but the output impedance is multiplied by 2.5 ... That's not good.

If we decrease $R_{FB}$, it drops the output impedance, but even more the gain. We're in trouble...

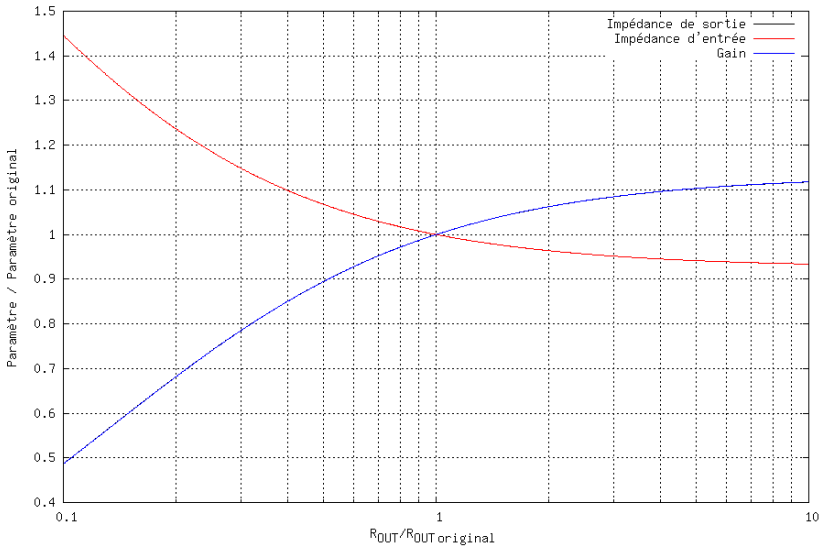



If now we vary $R_{IN}$, we get this



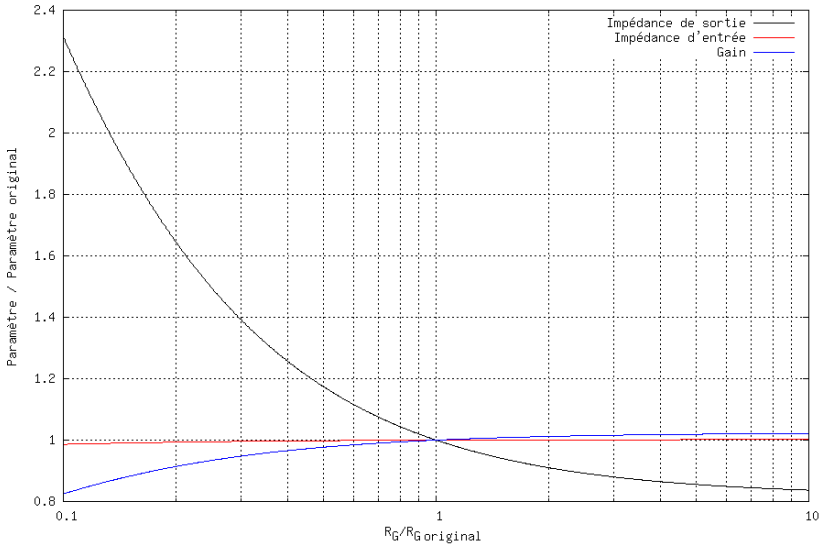
This obviously shows that if $R_{IN}$ increases, input impedance follows the movement, and gain follows the opposite trend. Exit impedance also follows the good trend, namely that if you increase the input impedance by increasing $R_{IN}$, the output impedance decreases. But we must not get up the mess, it is not in huge reports, and the decrease in the gain observed is not worth the candle. In addition, too much input impedance will have negative consequences in terms of noise sensitivity...

We still haven't found a miracle recipe. Could a variation of $R_{OUT}$ help us? Let's see...




It still seems lost... The earnings variation and output impedance curves are perfectly confused, and given the relatively small range of variation, the $R_{OUT}$ effect does not look obvious. One of the surprises (for me at least) comes from the low $R_{OUT}$ dependence of output impedance: If you increase $R_{OUT}$ tenfold, the output impedance increases only by 10%. Not bad, after all. And another interesting thing, by the way. If you look for little gain, you can halve the output impedance by dividing the $R_{OUT}$ by 10. Admittedly the gain drops by half too, but to make a good buffer, it is perhaps a way to follow, especially since a decrease in $R_{OUT}$ increases the stability of the offset ...

Well, we still have $R_G$ to test:

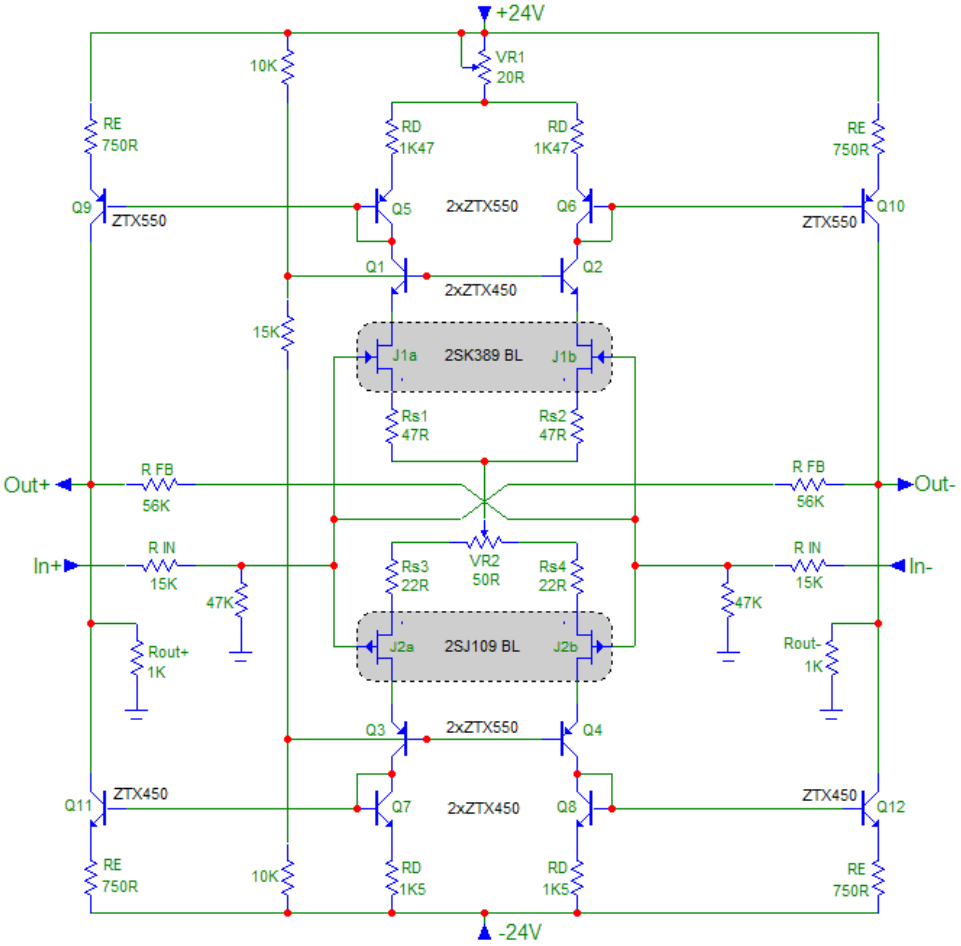



A good point: the grid resistance at the entrance plays very little on the gain and impedance of input. And contrary to what one could imagine (it is placed as an entrance ...), it has a nice influence on the output impedance. Okay, it's not huge there either: If we increase it tenfold, we reduce the output impedance by fifteen percent ... It's not much in the end...

These few curves are rather there to show trends, and I will not draw rules, seen as all the parameters are interwoven, But free to you to make your setting. Beoualà... We've pretty much gone around this. Well, it's not exhaustive, it's simplified, but if it helped you get into the arcane of this crincrin, I would not have wasted my time.

- End of Article -

With that behind us, the circuit is now fully realized and explained.




*UGS V.3 by Flat/Flatlabs ca 2006.*

# What is hFE of a Transistor?


hFE of a transistor is the current gain or amplification factor of a transistor.

hFE (which is also referred to as β) is the factor by which the base current is amplified to produce the amplified current of the transistor. The unamplified current is the base current, which then undergoes amplification by a factor of hFE to produce an amplified current which flows through the collector and emitter terminals.

A transistor works by feeding a current into the base of the transistor. The base current is then amplified by hFE to yield its amplified current. The formula is below:

$IC = h_{FE}I_B = \beta I_B$

So if 1mA is fed into the base of a transistor and it has a hFE of 100, the collector current will be 100mA.

Every transistor has its own unique hFE. The hFE is normally seen to be a constant value, normally around 10 to 500, but it may change slightly with temperature and with changes in collector-to-emitter voltage.

Check the transistor's datasheet for the hFE value in its specifications.

Note that hFE may refer to DC or AC current gain. Many datasheets may just specify one value, such as the DC gain. The datasheets will normally specify whether the hFE value is for DC or AC current gain.

Also, note that as the hFE value is highly variable, many datasheets will specify a minimum and maximum hFE for the transistor. It is very hard for transistors to be produced with a precise hFE value during the manufacturing process. Therefore, manufacturers generally specify a range that hFE may be within.

Because hFE is so widely variable and unpredictable in nature, good transistor circuit design is important to give stable, predictable amplification for transistor circuits to account for this unpredictability.

Source: http://www.learningaboutelectronics.com/Articles/What-is-hfe-of-a-transistor