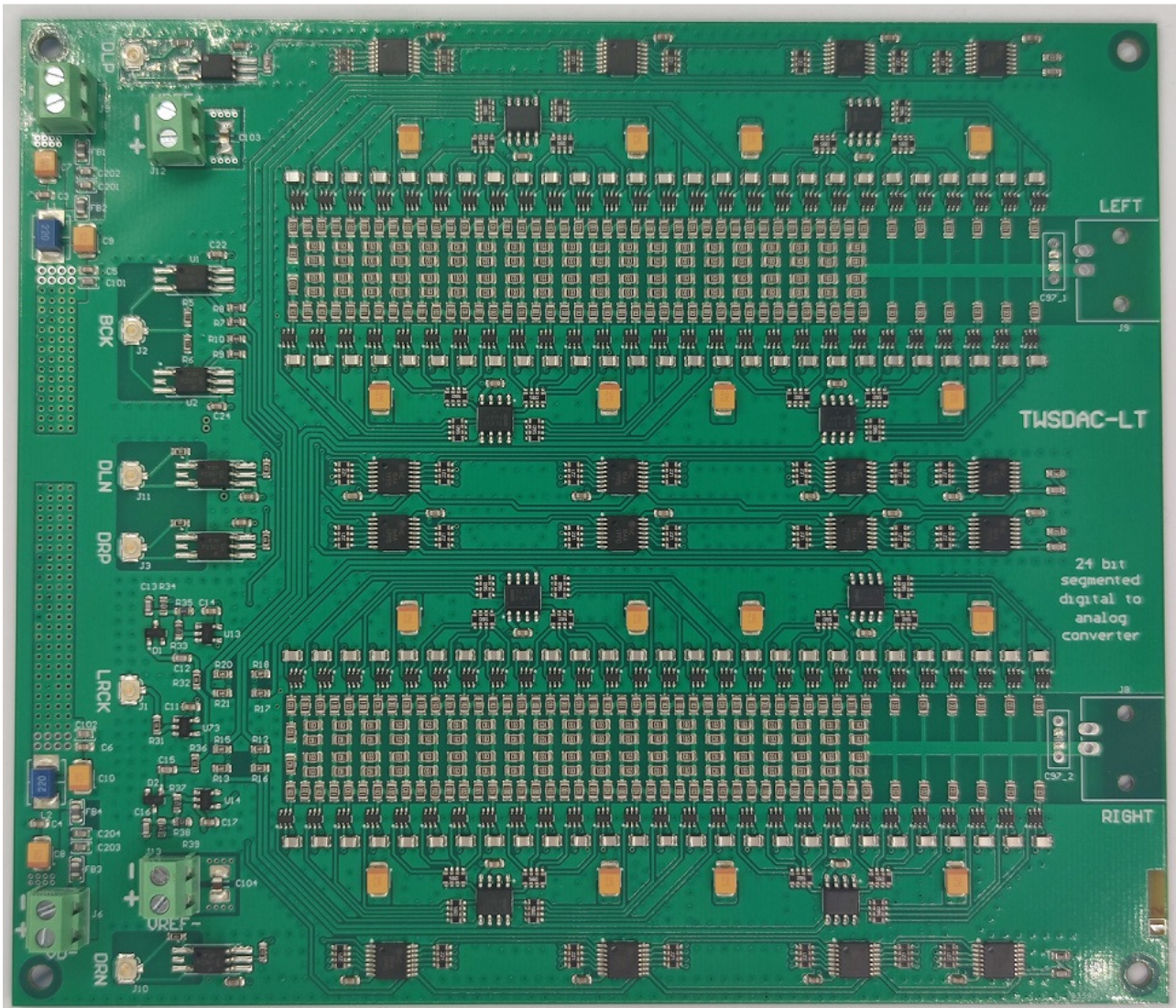


## TWSDAC-LT The Well Segmented DAC (Lite)



The TWSDAC-LT is 24 bit 384kHz segmented/sign magnitude discrete DAC with digital calibration.

The TWSAFB-LT FIFO buffer provides the custom protocol to feed the DAC in sign magnitude architecture. This architecture avoids the DAC to switch the MSB every zero crossing in order to decrease the glitch.

The TWSAFB-LT FIFO buffer also applies the DAC calibration in order to correct the accuracy error due to the tolerance of the resistors used in the ladder.

The resistor ladder of the DAC is segmented to get lower glitch and better performance. First 3 MSBs are thermometer decoded, so only one resistor is switched at a time. The remaining 20 LSBs are R2R decoded.

The DAC works with sign magnitude notation, so the MSB never switches at zero crossing. In fact there are 2 x 23 bit DAC for each channel, one manages the positive rail and the other manages the negative rail.

The dirty part of the incoming signals are optically isolated to avoid any interference with the crucial signal for the DAC, which is the LRCK.

The DAC works in stopped clock mode. This way the bit clock is stopped as soon as the shift registers are loaded with data, avoiding any interference with the LRCK. Practically, when the DAC latches a new word the bit clock has been previously stopped.

The DAC Lite operates in NOS mode, so oversampling must be done in the software if necessary.

The output impedance is 625 ohm, it can easily drive the most preamplifiers and amplifiers. To drive heavy load (below 20k) an optional output buffer is available (TWTSSB).

Digital (VDD) and analog (Vref) power supplies are separated to get better isolation between the digital and the analog parts of the DAC.

The TWSDAC-LT needs a custom data format. It does not work when not driven by the TWSAFB-LT FIFO Lite.

5.6448 MHz and 6.144 MHz DRIXO oscillators (TWTMC-DRIXO) are recommended to get the best performance from the DAC Lite.

Features:

**Inputs:** 24 bit PCM custom protocol (provided by the TWSAFB-LT FIFO buffer)

**Format:** up to 24 bit 384kHz

**Architecture:** segmented thermometer (first 3 MSBs) / R2R discrete ladder with sign magnitude notation

**Clock mode:** stopped clock

**Master clock:** 5.6448/6.144 MHz up to 176.4/192 KHz, 11.2896/12.288 MHz up to 352.8/384KHz

**Isolation:** BCK and DATA signals optically isolated

**Calibration:** the DAC can be calibrated for maximum accuracy, the TWSAFB-LT FIFO buffer applies the necessary corrections

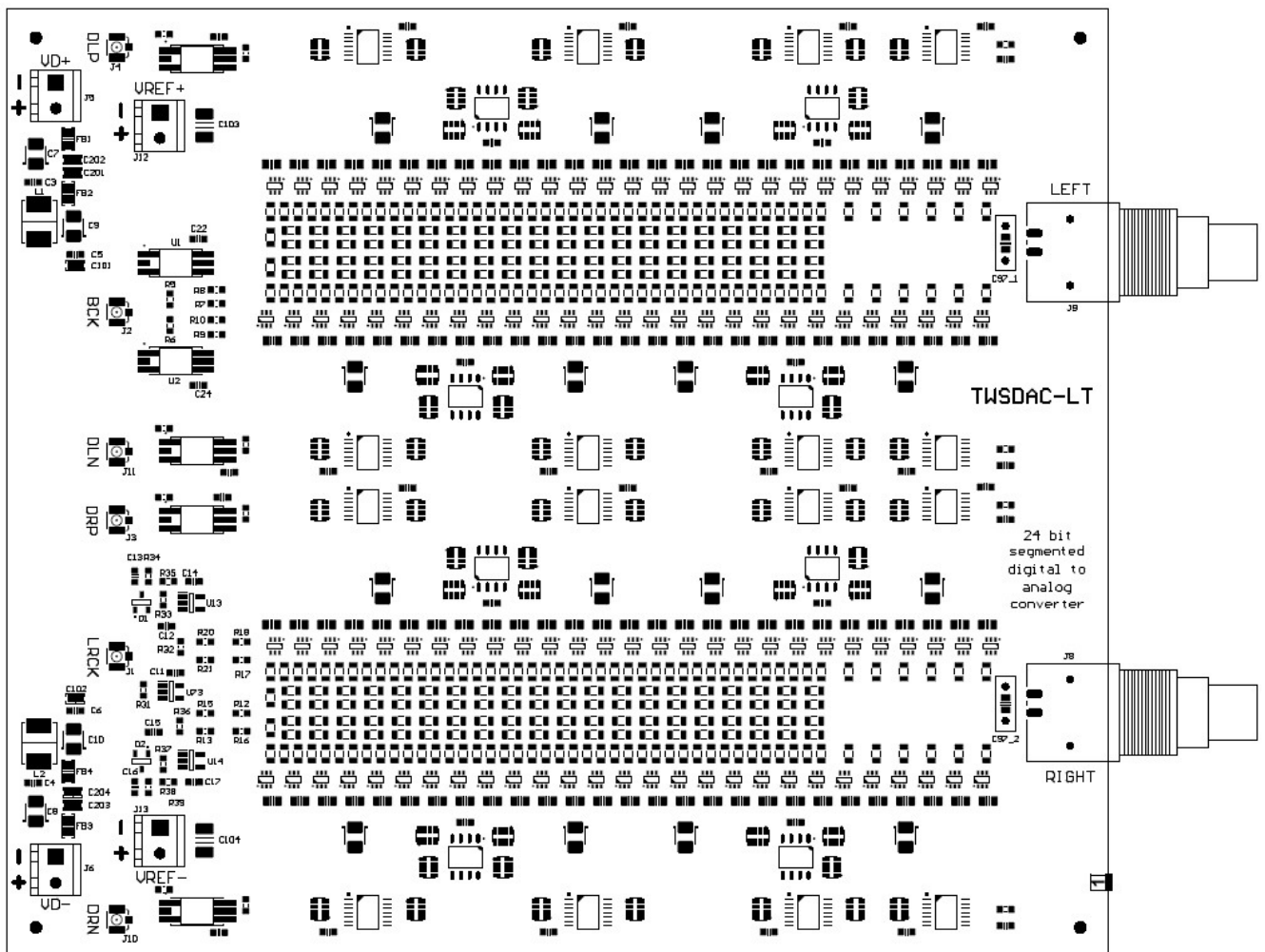
**Output:** voltage output 1.2V to 1.8V rms

**Power supply:** digital VDD +/- 3.3VDC to +/- 5VDC 50 mA, analog Vref +/- 3.3VDC to +/- 5VDC 30 mA

**Board size:** 163 x 140 mm

**Note:** finished board without RCA connector (stereo).

## PCB layout



## Connectors

**J1:** LRCK, latch input

**J2:** BCK, bit clock

**J3:** DRP, right channel serial positive rail data input

**J4:** DLP, left channel serial positive rail data input

**J10:** DRN, right channel serial negative rail data input

**J11:** DLN, left channel serial negative rail data input

**J8:** Right analog output

**J9:** Left analog output

**J5-J6:** VDD Digital power supply, +/- 3.3VDC to +/- 5VDC 50 mA

**J12-J13:** Vref Analog power supply, +/- 3.3VDC to +/- 5VDC 30 mA

There is 1 available option for this board: finished stereo board without RCA connectors

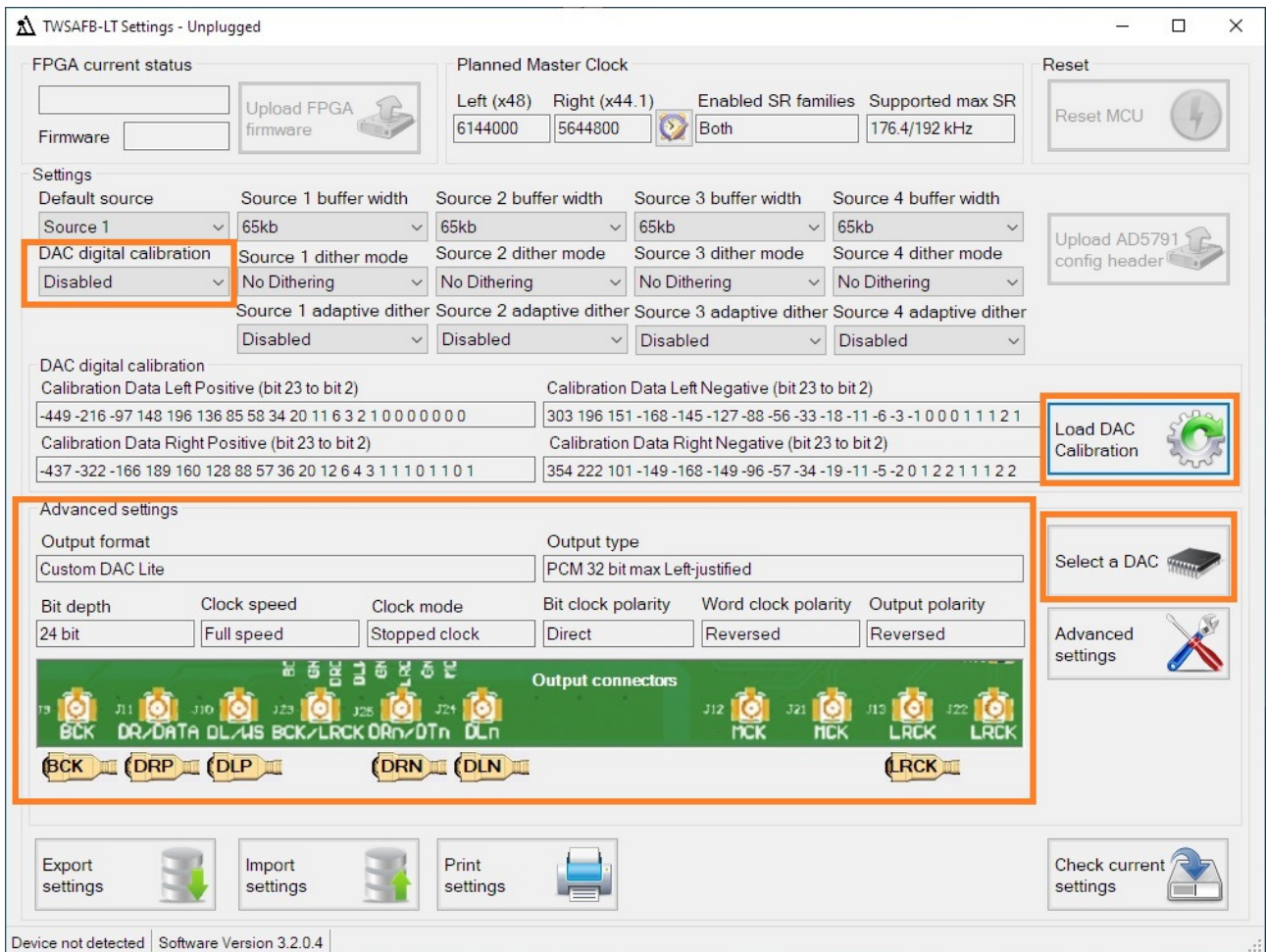


## Settings

No settings are needed.

## Configuring and connecting to the TWSAFB-LT (FIFO Lite)

In order to get the DAC working, the TWSAFB-LT has to be configured as below:



1. Download, install and open the TWSAFB-LT Settings Windows application
2. Connect the TWSAFB-LT to a PC by USB
3. Wait until the device is detected
4. Press "Select a DAC" and select the " TWSDAC-LT 24 bit 384kHz segmented/sign magnitude discrete DAC" from the DAC database
5. Press "Load DAC calibration" to upload the calibration file (if provided), then set "DAC digital calibration" to "Enabled"
6. Press "Save in EEPROM" to store the settings in the TWSAFB-LT memory
7. Disconnect the USB from the TWSAFB-LT
8. Connect the DAC board as in the above picture using short u.fl cables
9. Connect a I2S source to the selected "Default source"

**Warning**

The DAC does not include any low pass filter at its output. You can install 1nF do 4.7nF capacitors on the footprints named C97\_1 and C97\_2 to add a simple 6dB/octave low pass filter.

VDD power supply has to be equal or greater than  $0.75 \times V_{ref}$ . For example, if  $V_{ref}$  is powered by  $\pm 4.5\text{VDC}$  then VDD has to be powered by at least 3.4 VDC. In this case, even the clean side of the TWSAFB-LT (J18) has to be powered by the same 3.4 VDC.