



TPS7A470x 36-V, 1-A, 4- μ V_{RMS}, RF LDO Voltage Regulator

1 Features

- Input Voltage Range: +3 V to +36 V
- Output Voltage Noise:
4 μ V_{RMS} (10 Hz, 100 kHz)
- Power-Supply Ripple Rejection:
 - 82 dB (100 Hz)
 - \geq 55 dB (10 Hz, 10 MHz)
- Two Output Voltage Modes:
 - ANY-OUT™ Version (User-Programmable Output via PCB Layout):
 - No External Feedback Resistors or Feed-Forward Capacitors Required
 - Output Voltage Range: +1.4 V to +20.5 V
 - Adjustable Version (TPS7A4701 only):
 - Output Voltage Range: +1.4 V to +34 V
- Output Current: 1 A
- Dropout Voltage: 307 mV at 1 A
- CMOS Logic Level-Compatible Enable Pin
- Built-In Fixed Current Limit and Thermal Shutdown
- Available in High-Performance Thermal Package:
5-mm x 5-mm QFN
- Operating Temperature Range:
–40°C to 125°C

2 Applications

- Voltage-Controlled Oscillators (VCO)
- Frequency Synthesizers
- Test and Measurement
- Instrumentation, Medical, and Audio
- RX, TX, and PA Circuitry
- Supply Rails for Operational Amplifiers, DACs, ADCs, and Other High-Precision Analog Circuitry
- Post DC-DC Converter Regulation and Ripple Filtering
- Base Stations and Telecom Infrastructure
- +12-V and +24-V Industrial Buses

3 Description

The TPS7A47 is a family of positive voltage (+36 V), ultralow-noise (4 μ V_{RMS}) low-dropout linear regulators (LDO) capable of sourcing a 1-A load.

The TPS7A4700 output voltages are user-programmable (up to 20.5 V) using a printed circuit board (PCB) layout without the need of external resistors or feed-forward capacitors, thus reducing overall component count.

The TPS7A4701 output voltage can be configured with a user-programmable PCB layout (up to 20.5 V), or adjustable (up to 34 V) with external feedback resistors.

The TPS7A47 is designed with bipolar technology primarily for high-accuracy, high-precision instrumentation applications where clean voltage rails are critical to maximize system performance. This feature makes the device ideal for powering operational amplifiers, analog-to-digital converters (ADCs), digital-to-analog converters (DACs), and other high-performance analog circuitry in critical applications such as medical, radio frequency (RF), and test-and-measurement.

In addition, the TPS7A47 is ideal for post dc-dc converter regulation. By filtering out the output voltage ripple inherent to dc-dc switching conversions, maximum system performance is ensured in sensitive instrumentation, test-and-measurement, audio, and RF applications.

For applications where positive and negative low-noise rails are required, consider TI's [TPS7A33](#) family of negative high-voltage, ultralow-noise linear regulators.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS7A470x	VQFN (20)	5 mm x 5 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

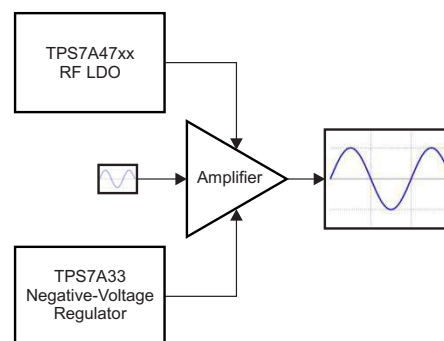


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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (January 2014) to Revision F	Page
Added <i>Handling Rating</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section	1
Reworded ninth bullet in <i>Features</i> list	1
Changed polarity of op amp shown on right side of the functional block diagram	12
Reworded second paragraph in <i>Soft-Start And Inrush Current</i> section	13
Revised <i>Capacitor Recommendations</i> section	16
Changed paragraph 2 of <i>Dropout Voltage (V_{DO})</i> section for clarity	17
Revised paragraph 1 of <i>Startup</i> section	17
Rewrote paragraph 1 of <i>Power-Supply Rejection Ratio (PSRR)</i> section to eliminate confusion	18
Changed paragraph 1 of <i>Power Supply Recommendations</i> section	20
Changed paragraph 1 and paragraph 4 of <i>Power Dissipation (P_D)</i> section	20
Revised paragraph 2 of <i>Layout Guidelines</i> section	21
Changed second paragraph of <i>Thermal Protection</i> section	22

Changes from Revision D (December 2013) to Revision E	Page
Changed Output Voltage Noise value from 4.17 μ V to 4 μ V in three instances on front page.....	1
Changed 2nd and 3rd paragraphs of <i>Description</i> section.....	1
Added "Thermal Pad" to pin configuration drawing.....	4
Changed EN pin description.....	4
Changed SENSE/FB pin to be for TPS7A4701 only.....	5
Added new row to Pin Descriptions table for SENSE pin (for TPS7A4700 only).....	5
Added new row to Pin Descriptions table for thermal pad	5
Added V _{REF} parameter.....	7

• Added TPS7A4701 device to test conditions for V_{NR} parameter.....	7
• Added Feedback Pin Current parameter to Electrical Characteristics	7
• Deleted Dropout Voltage vs Output Current graph	8
• Added EN pin to Functional Block Diagram	12
• Added sentence to ANY-OUT Programmable Output Voltage section to clarify ANY-OUT is for both devices	13
• Changed last two paragraphs of <i>Adjustable Operation</i> section	14
• Added "TPS7A4701 Only" to <i>Adjustable Operation</i> section title	14
• Deleted equation in Figure 23	14
• Changed Equation 3	14

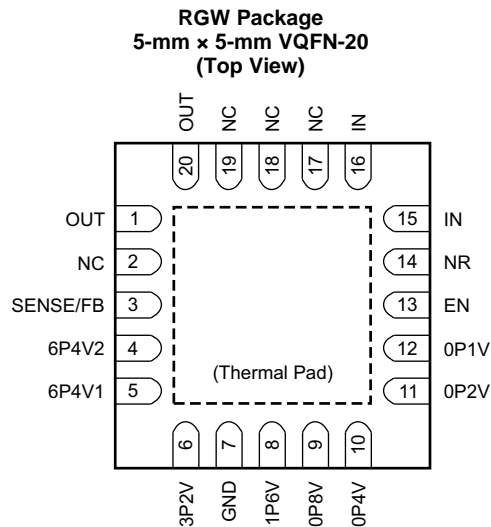
Changes from Revision C (July 2013) to Revision D	Page
• Changed data sheet status from production mix to production data.....	1
• Changed TPS7A4701 ESD rating from > 1 kV to 2.5 kV	1
• Changed noise reduction pin voltage parameter to show both devices	7
• Added text clarifying V_{REF} typical value to last paragraph on page.....	14

Changes from Revision B (April 2013) to Revision C	Page
• Deleted TPS7A4702 preview device from data sheet.....	1

Changes from Revision A (July 2012) to Revision B	Page
• Changed TPS7A47 to TPS7A4700	1
• Added TPS7A4701 and TPS7A4702 preview devices to data sheet.....	1
• Changed front-page figure.....	1
• Added FB to SENSE pin to Functional Block Diagram	12
• Added new paragraph after Table 1	14
• Added new Table 2	14
• Added <i>Adjustable Operation</i> section	14

Changes from Original (June 2012) to Revision A	Page
• Moved to full production data (changes throughout document)	1

5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
0P1V	12	I	When connected to GND, this pin adds 0.1 V to the nominal output voltage of the regulator. Do not connect any voltage other than GND to this pin. If not used, leave this pin floating.
0P2V	11	I	When connected to GND, this pin adds 0.2 V to the nominal output voltage of the regulator. Do not connect any voltage other than GND to this pin. If not used, leave this pin floating.
0P4V	10	I	When connected to GND, this pin adds 0.4 V to the nominal output voltage of the regulator. Do not connect any voltage other than GND to this pin. If not used, leave this pin floating.
0P8V	9	I	When connected to GND, this pin adds 0.8 V to the nominal output voltage of the regulator. Do not connect any voltage other than GND to this pin. If not used, leave this pin floating.
1P6V	8	I	When connected to GND, this pin adds 1.6 V to the nominal output voltage of the regulator. Do not connect any voltage other than GND to this pin. If not used, leave this pin floating.
3P2V	6	I	When connected to GND, this pin adds 3.2 V to the nominal output voltage of the regulator. Do not connect any voltage other than GND to this pin. If not used, leave this pin floating.
6P4V1	5	I	When connected to GND, this pin adds 6.4 V to the nominal output voltage of the regulator. Do not connect any voltage other than GND to this pin. If not used, leave this pin floating.
6P4V2	4	I	When connected to GND, this pin adds 6.4 V to the nominal output voltage of the regulator. Do not connect any voltage other than GND to this pin. If not used, leave this pin floating.
EN	13	I	Enable pin. The device is enabled when the voltage on this pin exceeds the maximum enable voltage, $V_{EN(HI)}$. If enable is not required, tie EN to IN.
GND	7	—	Ground
IN	15, 16	I	Input supply. A capacitor greater than or equal to 1 μ F must be tied from this pin to ground to assure stability. A 10- μ F capacitor is recommended to be connected from IN to GND (as close to the device as possible) to reduce circuit sensitivity to printed circuit board (PCB) layout, especially when long input traces or high source impedances are encountered.
NC	2, 17-19	—	This pin can be left open or tied to any voltage between GND and IN.
NR	14	—	Noise reduction pin. When a capacitor is connected from this pin to GND, RMS noise can be reduced to very low levels. A capacitor greater than or equal to 10 nF must be tied from this pin to ground to assure stability. A 1- μ F capacitor is recommended to be connected from NR to GND (as close to the device as possible) to maximize ac performance and minimize noise.

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
OUT	1, 20	O	Regulator output. A capacitor greater than or equal to 10 μ F must be tied from this pin to ground to assure stability. A 47- μ F ceramic output capacitor is highly recommended to be connected from OUT to GND (as close to the device as possible) to maximize ac performance.
SENSE/FB	3	I	Control-loop error amplifier input (TPS7A4701 only). This is the SENSE pin if the device output voltage is programmed using ANY-OUT (no external feedback resistors). This pin must be connected to OUT. Connect this pin to the point of load to maximize accuracy. This is the FB pin if the device output voltage is set using external resistors. See the Adjustable Operation section for more details.
SENSE	3	I	Control-loop error amplifier input (TPS7A4700 only). This is the SENSE pin of the device and must be connected to OUT. Connect this pin to the point of load to maximize accuracy.
Thermal Pad		—	Connect the thermal pad to a large-area ground plane. The thermal pad is internally connected to GND.

6 Specifications

6.1 Absolute Maximum Ratings

Over junction temperature range, unless otherwise noted.⁽¹⁾

		MIN	MAX	UNIT
Voltage ⁽²⁾	IN pin to GND pin	–0.4	+36	V
	EN pin to GND pin	–0.4	+36	V
	EN pin to IN pin	–36	+0.4	V
	OUT pin to GND pin	–0.4	+36	V
	NR pin to GND pin	–0.4	+36	V
	SENSE/FB pin to GND pin	–0.4	+36	V
	0P1V pin to GND pin	–0.4	+36	V
	0P2V pin to GND pin	–0.4	+36	V
	0P4V pin to GND pin	–0.4	+36	V
	0P8V pin to GND pin	–0.4	+36	V
	1P6V pin to GND pin	–0.4	+36	V
	3P2V pin to GND pin	–0.4	+36	V
	6P4V1 pin to GND pin	–0.4	+36	V
	6P4V2 pin to GND pin	–0.4	+36	V
Current	Peak output	Internally limited		
Temperature	Operating virtual junction, T _J	–40	125	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability..

- (2) All voltages are with respect to network ground terminal.