



TPS7A33 –36-V, 1-A, Ultralow-Noise Negative Voltage Regulator

1 Features

- Input Voltage Range: –3 V to –36 V
- Noise:
 - 16 μV_{RMS} (10 Hz to 100 kHz)
- Power-Supply Ripple Rejection:
 - 72 dB (10 kHz)
- Adjustable Output: –1.18 V to –33 V
- Maximum Output Current: 1 A
- Stable With Ceramic Capacitors $\geq 10 \mu\text{F}$
- Built-In Current-Limit and Thermal Shutdown Protection
- Available in an External Heatsink-Capable, High Thermal Performance TO-220 Package
- Operating Temperature Range: –40°C to 125°C

2 Applications

- Supply Rails for Operational Amplifiers, DACs, ADCs, and Other High-Precision Analog Circuitry
- Audio
- Post DC-DC Converter Regulation and Ripple Filtering
- Test and Measurement
- Medical
- Industrial Instrumentation
- Base Stations and Telecom Infrastructure
- 12-V and 24-V Industrial Buses

3 Description

The TPS7A33 series of linear regulators are negative voltage (–36 V), ultralow-noise (16- μV_{RMS} , 72-dB PSRR) linear regulators capable of sourcing a maximum load of 1 A.

The TPS7A33 series include a complementary metal oxide semiconductor (CMOS) logic-level-compatible enable pin (EN) to allow for user-customizable power management schemes. Other features available include built-in current limit and thermal shutdown features to protect the device and system during fault conditions.

The TPS7A33 family is designed using bipolar technology primarily for high-accuracy, high-precision instrumentation applications, where clean voltage rails are critical to maximize system performance. This feature makes it ideal to power operational amplifiers, analog-to-digital converters (ADCs), digital-to-analog converters (DACs), and other high-performance analog circuitry.

In addition, the TPS7A33 family of linear regulators is suitable for post DC-DC converter regulation. By filtering out the output voltage ripple inherent to DC-DC switching conversion, maximum system performance is ensured in sensitive instrumentation, medical, test and measurement, audio, and RF applications.

For applications where positive and negative high-performance rails are required, consider the [TPS7A4700](#) positive high-voltage, ultralow-noise, low-dropout linear regulator as well.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS7A33	TO-220 (7)	10.17 mm × 8.38 mm
	VQFN (20)	5.00 mm × 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic

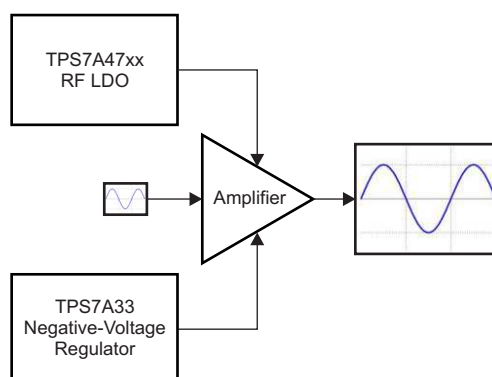


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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (February 2013) to Revision D	Page
Added ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section	1
Corrected title of data sheet to show accurate maximum output current; changed "–1 A" to "1-A"	1
Changed front-page figures and deleted note stating that RGW package was product preview.....	1
Changed Pin Configuration and Functions section; updated table format and deleted footnote about RGW product-preview status.....	4
Deleted footnote from Pin Functions table indicating RGW product-preview status.....	4
Deleted footnote (2) from Absolute Maximum Ratings table.....	5
Deleted note from Thermal Information table stating that RGW package was product preview	5
Corrected condition values for Figure 23	9
Corrected condition values for Figure 24	9
Corrected condition values and trace indicators for Figure 25.....	10
Corrected condition values and trace indicators for Figure 26.....	10
Changed C _{SS} value from 1 μ F to 10 nF in Figure 27	10
Deleted Parametric Measurement Information section	12
Revised Functional Block Diagram.....	12
Changed first paragraph of Adjustable Operation section stating the device output voltage range	15
Changed Equation 2 for clarity	15
Changed last sentence of Capacitor Recommendations section	16
Changed noise reduction capacitor value from 1 μ F to 10 nF in first paragraph of Power-Supply Rejection section.....	17
Revised last paragraph of Power-Supply Rejection section.....	17
Changed noise reduction capacitor value from 1 μ F to 10 nF in second paragraph of Output Noise section.	17
Added footnote (1) to Figure 32	18
Changed title for Figure 41	23
Changed title for Figure 42.....	23

Revision History (continued)

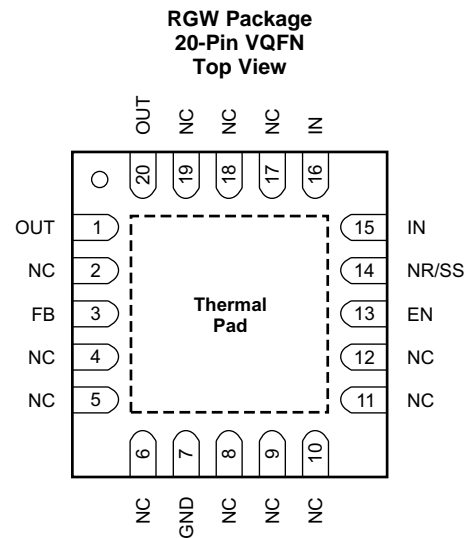
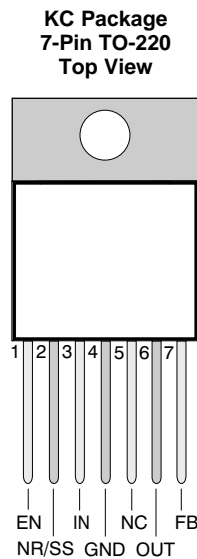
- Changed *Power Dissipation* section title to *Layout Guidelines for Thermal Performance and Heat Sink Selection* 24
- Revised wording in *Layout Guidelines for Thermal Performance* section for clarification 24

Changes from Revision B (March 2012) to Revision C	Page
• Changed product status from Mixed Status to Production Data	1
• Added last paragraph in <i>Description</i> section.....	1
• Changed typical application block diagram	1
• Updated Figure 31	17

Changes from Revision A (December 2011) to Revision B	Page
• Changed product status from Production Data to Mixed Status	1
• Added RGW pinout drawing	1
• Added RGW pinout drawing to <i>Pin Configuration and Functions</i> section	4
• Added RGW and footnote 1 to Pin Functions table	4
• Added RGW column to <i>Thermal Information</i> table.....	5

Changes from Original (December 2011) to Revision A	Page
• Changed product status from Product Preview to Production Data	1

5 Pin Configuration and Functions



Pin Functions

NAME	PIN		I/O	DESCRIPTION
	TO-220	VQFN		
EN	1	13	I	This pin turns the regulator on or off. If $V_{EN} \geq V_{EN(+HI)}$ or $V_{EN} \leq V_{EN(-HI)}$, the regulator is enabled. If $V_{EN(+LO)} \geq V_{EN} \geq V_{EN(-LO)}$, the regulator is disabled. The EN pin can be connected to IN, if not used. $ V_{EN} \leq V_{IN} $.
FB	7	3	I	This pin is the input to the control-loop error amplifier. It is used to set the output voltage of the device. TI recommends connecting a 10-nF capacitor from FB to OUT (as close to the device as possible) to maximize AC performance.
GND	4	7	—	Ground
IN	3	15, 16	I	Input supply. A capacitor greater than or equal to 10 nF must be tied from this pin to ground to assure stability. It is recommended to connect a 10- μ F capacitor from IN to GND (as close to the device as possible) to reduce circuit sensitivity to printed-circuit-board (PCB) layout, especially when long input traces or high source impedances are encountered.
NC	5	2, 4-6, 8-12, 17-19	—	This pin can be left open or tied to any voltage between GND and IN.
NR/SS	2	14	—	Noise reduction pin. A capacitor connected from this pin to GND controls the soft-start function and allows RMS noise to be reduced to very low levels. TI recommends connecting a 1- μ F capacitor from NR/SS to GND (as close to the device as possible) to filter the noise generated by the internal bandgap and maximize ac performance.
OUT	6	1, 20	O	Regulator output. A capacitor greater than or equal to 10 μ F must be tied from this pin to ground to assure stability. TI recommends connecting a 47- μ F ceramic capacitor from OUT to GND (as close to the device as possible) to maximize ac performance.
Thermal Pad	Tab	—	—	Connect the thermal pad to a large-area ground plane. The thermal pad is internally connected to GND. An external heatsink can be installed to provide additional thermal performance.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	UNIT
Voltage	IN pin to GND pin	–36	0.3	V
	OUT pin to GND pin	–33	0.3	
	OUT pin to IN pin	–0.3	36	
	FB pin to GND pin	–2	0.3	
	FB pin to IN pin	–0.3	36	
	EN pin to GND pin	–36	10	
	NR/SS pin to IN pin	–0.3	36	
	NR/SS pin to GND pin	–2	0.3	
Current	Peak output	Internally limited		
Temperature	Operating virtual junction, T _J	–40	150	°C
	Storage temperature, T _{stg}	–65	150	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD) Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±1000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _{IN}	Input supply voltage	–35		–3	V
V _{EN}	Enable supply voltage	V _{IN}		10	V
V _{OUT}	Output voltage	–33.2		V _{REF}	V
I _{OUT}	Output current	0		1	A
R ₂ ⁽¹⁾	R ₂ is the lower feedback resistor			240	kΩ
C _{IN}	Input capacitor	10	47		μF
C _{OUT}	Output capacitor	10	47		μF
C _{NR}	Noise reduction capacitor		1		μF
C _{FF}	Feed-forward capacitor		10		nF
T _J	Operating junction temperature	–40		125	°C

- (1) This condition helps ensure stability at no load.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS7A33		UNIT
		KC (TO-220)	RGW (VQFN)	
		7 PINS	20 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	31.2	33.7	°C/W
R _{θJC(top)}	Junction-to-case(top) thermal resistance	40	30.4	
R _{θJB}	Junction-to-board thermal resistance	17.4	12.5	
Ψ _{JT}	Junction-to-top characterization parameter	6.4	0.4	
Ψ _{JB}	Junction-to-board characterization parameter	17.2	12.5	
R _{θJC(bot)}	Junction-to-case(bottom) thermal resistance	0.8	2.4	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).