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Basic Thermal Management of Power Semiconductors

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Thermal management of power semiconductors is often overlooked by design engineers, either through oversight, misconception, inexperience, or even perceived unimportance. Then it is only addressed when the system is ready for packaging and by that time, it may be too late. Because of the need in maintaining the junction temperature of these semiconductors as low as possible to ensure increased reliability, understanding thermal management becomes very important. Thus it is the intent of this article to provide the basics of thermal management, its meaning, significance, characteristics and measurements.

Reliability, service life and performance of a semiconductor device is a direct function of its junction temperature. A rule of thumb is that for every 10°C rise above 100°C, the operating life of the device will be halved. It is imperative that the device run as cool as possible, within cost-performance constraints; the heat sink cannot be unlimitedly large nor excessively expensive.

STEADY STATE THERMAL RESISTANCE

Power ratings of semiconductors are based on the maximum junction temperature which in turn, is dictated by its thermal resistance. When power is applied to the semiconductor, the junction temperature will rise to a value based on the power dissipated at the junction and the ability of the device and its heat sink to conduct this heat away. A steady-state (average) condition is reached when the heat generated equals the heat conducted away. Thermal resistance is thus a measure of the ability of the semiconductor device and its package for removing heat away from the junction. It can be expressed by the equation:

$$T_J - T_R = P_D R_{\theta JR}$$

where:

T_J = Junction Temperature

T_R = Temperature at reference point

P_D = Power dissipated at the junction

$R_{\theta JR}$ = Thermal resistance from junction to the temperature reference point.

Figure 1 describes the basic steady-state thermal resistance model showing the thermal to electrical analogy. Note the similarity to Ohm's Law: temperature "T" could be thought of as voltage, thermal resistance as electrical resistance, power dissipation "P_D" as current and the ambient temperature "T_A" as a battery.

The temperature at any reference point in the loop can be determined when the individual thermal resistances are known. For example, if the reference is the semiconductor case, all related subscripts become "C" (for case), and the equation for junction temperature becomes:

$$T_J = P_D R_{\theta JC} + T_C$$

If the reference is the ambient temperature T_A, then:

$$T_J = P_D R_{\theta JA} + T_A$$

where $R_{\theta JA}$ is the sum of all the thermal resistances:

$$T_J = P_D (R_{\theta JC} + R_{\theta CS} + R_{\theta SA}) + T_A,$$

$R_{\theta JC}$ is the semiconductor thermal resistance junction to case,

$R_{\theta CS}$ is the interface thermal resistance case to heat sink,

$R_{\theta SA}$ is the heat sink thermal resistance sink to ambient.

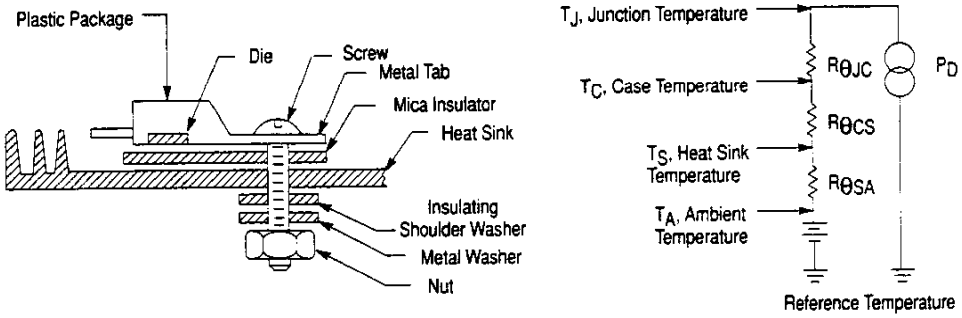

Figure 1. Basic Thermal Resistance Model Showing Thermal to Electrical Analogy For a Semiconductor

MAXIMUM RATINGS				
Rating	Symbol	MJE13008	MJE13009	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	300	400	Vdc
Collector-Emitter Voltage	V_{CEV}	600	700	Vdc
Emitter Base Voltage	V_{EBO}	9		Vdc
Collector Current - Continuous	I_C	12		Adc
- Peak (1)	I_{CM}	24		
Base Current - Continuous	I_B	6		Adc
- Peak (1)	I_{EM}	12		
Emitter Current - Continuous	I_E	18		Adc
- Peak (1)	I_{EM}	36		
Total Power Dissipation @ T_A = 25°C,	P_D	2		Watts
Derate above 25°C		16		mW/°C
Total Power Dissipation @ T_C = 25°C,	P_D	100		Watts
Derate above 25°C		800		mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	− 65 to +150		°C

THERMAL CHARACTERISTICS			
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.25	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JA}$	62.5	°C/W
Maximum Lead Temperature for Soldering Purposes 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

Figure 2A. Thermal Specifications For the MJE13009

Each thermal resistance must be minimized if the lowest junction temperature is to be achieved at a given power level. Although each element might be thought of as a constant, that's not quite the case. $R_{\theta JC}$ is the value specified on the device data sheet, presumably worst case, with enough margin built in to accommodate a production spread of devices. Even for the same transistor, the thermal resistance $R_{\theta JC}$ derived from a constant power dissipation but different voltage-current products can vary by as much as 10%. Normally the bias for a transistor (V_{CE} and I_C) is chosen where the current density is uniform (i.e. low V_{CE}, high I_C); for higher V_{CE}, the current density becomes less uniform and higher $R_{\theta JC}$ can result.

The interface thermal resistance $R_{\theta CS}$ can also vary due to different mounting pressures, heat sink surface finish, non-flatness of the semiconductor case and non-uniformity of the insulator, if used.

Heat sink thermal resistance is affected by the orientation of the sink (horizontal or vertical) and the ambient temperature ($R_{\theta SA}$ decreases somewhat as T_A increases).

BIPOLAR POWER TRANSISTOR THERMAL CHARACTERISTICS

Once the thermal resistance $R_{\theta JC}$ and/or $R_{\theta JA}$ is known, the power dissipation P_D of the package can be calculated. Take the example of the plastic package TO-220, NPN power transistor MJE13009 specification shown in Figure 2A. Perhaps one of the most misunderstood parameters is the total power dissipation P_D spec. For this device, whose maximum operating temperature is 150°C, the P_D is specified at 100 W when the case temperature T_C is maintained at 25°C. What this implies is that the transistor is mounted on an infinite sink, certainly not a realistic or practical situation. The second P_D spec is where the ambient temperature T_A is 25°C and P_D is rated at only 2 W. This condition implies a free-air mounting and would be the maximum power capability of the device if it were soldered into a printed circuit board without a heat sink. The real world is usually somewhere in between. Both specifications are derated with temperature at 800 mW/°C and 16 mW/°C respectively. Figure 2B shows the typical thermal derating curve being derated down to zero at a case temperature of 150°C.

At a case temperature of 100°C, for example, the transistor can dissipate 40 W and still maintain T_J at 150°C. Recall that P_D is derived from a measured (and derated) $R_{\theta JC}$ (or $R_{\theta JA}$). For this transistor, $R_{\theta JC}$ is specified as 1.25°C/W. P_D thus becomes:

$$P_D = \frac{T_J - T_C}{R_{\theta JC}} = \frac{150°C - 25°C}{1.25°C/W} = 100\ W$$

In actuality, P_D is rounded off to the nearest whole number and the $R_{\theta JC}$ specified is based on that number; the result of 1.25°C/W shows three figure accuracy. As will be shown later, the measured thermal resistance is accurate and repeatable at the best to only two figures.

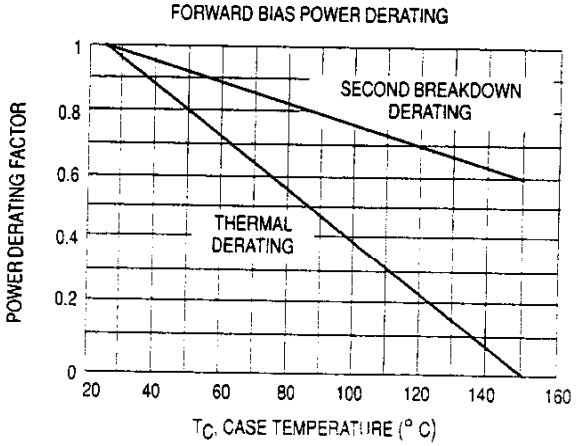

Figure 2B. Thermal Derating Curve For the 100 W MJE13009 TO-220 High Voltage Transistor

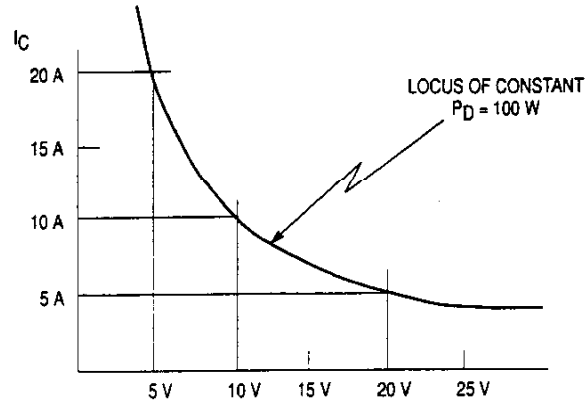

Figure 3A. Linear-Linear Plot of Constant P_D

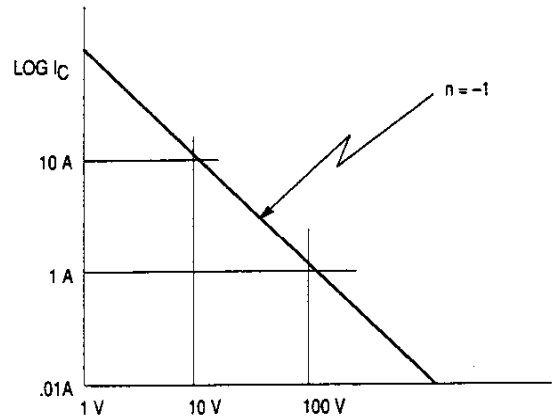

Figure 3B. Log-Log Plot of Constant P_D

Figure 3A shows the locus of constant DC power dissipation on a linear-linear plot resulting in the hyperbolic function:

$$I_C = \frac{P_D}{V_{CE}}$$

When this curve is replotted on a log-log scale, Figure 3B, the constant power curve results in a straight line with a slope n of −1. The example of Figure 3 describes a transistor with a power dissipation of 100 W (10 V, 10 A; 100 V, 1 A). In actuality, this constant P_D seldom extends to the high voltage rating of a bipolar power transistor, as shown by the Active Region Safe Operating Area curves of Figure 4 (also known as Forward Bias Safe Operating Area, FBSOA). The dashed portion of the DC curve and the 1 ms and 100 µs pulsed curves represent the locus of constant power when the case temperature is maintained at 25° C. Under these conditions, these portions of the curves are the thermal limits whereby the junction temperature T_J is 150° C, the maximum operating temperature.

Second breakdown limits – shown by the solid lines – occur at the higher voltage, lower current portion of the curves and will greatly reduce the power handling capability of the transistor. These empirically derived curves are obtained through destructive testing of many transistors to determine their V_{CE}, I_C limits. Simply stated, FBSOA second breakdown results from current crowding around the periphery of the emitter finger when the transistor is turned on. Under these extreme bias conditions, a hot spot is created which ultimately burns through the transistor die, destroying the device.

Note that there are no thermal limits for the 100 µs pulse, that it is only second breakdown limited. Of interest is that these second breakdown curves were generated from a common-base configuration where V_{CE}, I_C and the pulse width are made variable. This configuration is also used in measuring thermal resistance.

The other two limits shown in Figure 4 are the maximum voltage rating V_{CEO} of the transistor and the maximum collector current I_C. The current is both a bonding wire limit for the DC curve and h_{FE} limit for the pulsed curves.

POWER MOSFET THERMAL CHARACTERISTICS

Since power MOSFETs are, in theory, immune to second breakdown their FBSOA curves are somewhat different than bipolars: there are no second breakdown limitations, only the thermal limits of the constant P_D curves. Consequently, all curves will be the constant P_D slope of −1, straight lines extending to the voltage breakdown rating BV_{DSS}.

For some power MOSFETs, at the high voltage, low current portion of FBSOA, the parasitic transistor second breakdown susceptibility might lower the curve. There is however, an $r_{DS(on)}$ limit which truncates the low voltage, high current portion of FBSOA. It is simply due to $V_{DS(on)}$ being equal to I_D ($r_{DS(on)}$), thus limiting the FET's on-voltage.

The maximum current limits, like the bipolar power transistor are dictated by the bonding wire and gain of the device.

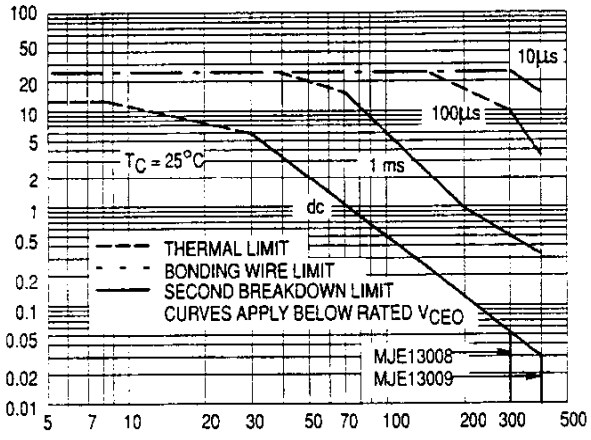

Figure 4. Forward Bias Safe Operating Area

Example:

A transistor rated at $\mathbf{P_{D(max)} = 200W}$, (for $\mathbf{T_j = 150^oC}$ and $\mathbf{T_c = 25^oC}$), is only allowed to dissipate $\mathbf{P_D = 40W}$.

1. Find $\mathbf{T_j}$ assuming $\mathbf{T_c = 70^oC}$.

2. Find maximum permissible dissipation at $\mathbf{T_c = 70^oC}$.

Solution:

1. $$\mathbf{R_{(j-c)}} = \frac{\left(\mathbf{150^oC - 25^oC}\right)}{\mathbf{200W}} = \mathbf{0.625^oC/W}$$

$\Rightarrow$

$$\mathbf{T_j} = \left(\mathbf{0.625^oC/W \times 40W}\right) + \mathbf{70^oC} = \mathbf{95^oC}$$

2. $$\mathbf{P_{D(max)}}\Big|_{\mathbf{T_c = 70^oC}} = \frac{\left(\mathbf{150^oC - 70^oC}\right)}{\mathbf{0.625^oC/W}} = \mathbf{128W}$$