

THD modeling exercise

1) Start MATLAB, open the file THDCalc.m, and run it

4 plots are generated:

- the output FET I/V characteristic
- transfer characteristic errors from Conduction states (unit V*s)
- transfer characteristic errors from Switching transitions (unit V*s)
- THD curve

These 4 plots can be switched on and off individually in lines 25-28

Locate the SYSTEM PARAMETERS section (line 32). The parameters are set for a BTL output stage running at 30V with a 4Ω load, providing approx. 90W output power. System parameters are set for near-zero transfer characteristic errors, so the only THD contribution is background noise (-100dB), causing THD+N vs. Power to decrease by first order.

2) Conduction state errors: $R_{DS(ON)}$ influence

Turn off the Switching error plot, and let $R_{DS(ON)}$ run from 100 to 300m Ω :

```
(line 27) PLOT_AREAS_SWITCH= 0;  
(line 30) for run=0:4,  
(line 33) RDSon=0.100+run*0.050;
```

Run the file.

FET I/V characteristics are clamped to approx. -0.8V by FET body diode

Larger $R_{DS(ON)}$ causes a larger conduction nonlinearity, starting from lower power.

Remove the $R_{DS(ON)}$ change again

```
(line 33) RDSon=0.100;
```

3) Switching errors: Dead time

Turn off the FET I/V and the Switching error plots, turn on Conduction error plot.

Let dead time (DT) run from 3 to 7 ns

```
(line 25) PLOT_FETIV= 0;  
(line 26) PLOT_AREAS_COND= 0;  
(line 27) PLOT_AREAS_SWITCH= 1;  
(line 40) DT=(3+run)*1e-9;
```

Run the file.

At low power, dead time does not cause distortion.

As power increases, two nonlinearities occur

1) Forced commutation transitions occur when I_{SPKR} starts exceeding I_{RIP} (see figure 3). This happens at a power level determined by the ripple current, independent of dead time.

2) The hyperbolic nonlinearity is excited when $I_{RIP}+I_{SPKR}$ exceeds I_{LIM} . When dead time increases, I_{LIM} decreases, and this nonlinearity onsets at lower power (seen at dead time 6 and 7ns).

4) Switching errors: Finite turn-on speed

In practice, forced commutation switching transitions (LH transitions with positive I_L and vice versa) are delayed with increasing $|I_L|$. This can be modeled to a first order by simply delaying the transition by a fixed number of ns per additional A of current:

Set this delay to 2ns/A :

```
(line 42) nsA_LH=2e-9;
```

Run the file.

Minimum THD now occurs for finite dead time (5ns). This value causes the best overall linearity of the transfer characteristic (figure 3).

Note that this distortion model is still very simple, and contains only a small selection of the nonlinearities present in an output stage. When additional nonlinearities are included, conclusions may change.