USEFUL INFORMATION FOR USERS OF TEKTRONIX INSTRUMENTS

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FIELD EFFECT TRANSISTORS

(Unipolar Transistors)

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At last we have what amounts to a backward vacuum tube—a p-channel FET. In this device, electron current goes from drain (plate) to source (cathode).

The Field Effect Transistor (FET) is a comparatively new device whose operation differs radically from the more familiar n-p-n and p-n-p types of transistors. The FET is a single-junction *majority-carrier* device while the n-p-n and p-n-p transistors are double-junction *minority-carrier* devices.

FET manufacturers have settled on a new series of names for the three basic leads of this device; so, once again we encounter a change in terminology. Figure 1 compares an FET, a conventional transistor and the familiar vacuum-tube triode to show this change in basic-lead terminology.

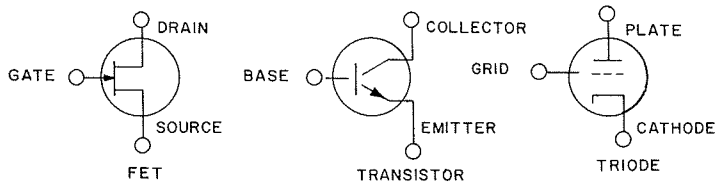

Figure 1. Comparison of basic lead terminology of FET's, transistors, and vacuum tubes.

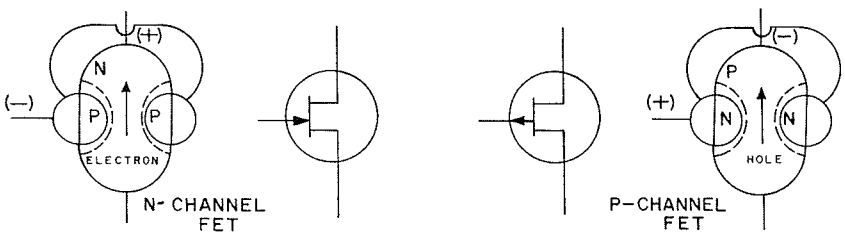

Figure 2. Comparison of an n-channel FET and a p-channel FET.

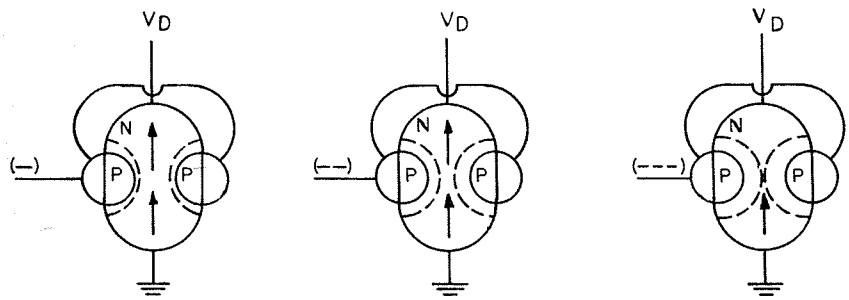

Figure 3. Illustration of how the voltage applied as back-bias can control the flow of current in an n-channel FET.

As with conventional transistors, which are represented by two types of devices (n-p-n and p-n-p), the FET is also represented by two types of devices. These are designated the n-channel and the p-channel types of devices (see Figure 2).

The electron in "n" material has a faster mobility than the hole in "p" material. Thus, the n-p-n transistor has a faster mobility than the p-n-p transistor and consequently a higher frequency response. A similar condition exists with the new FET's. The n-channel FET promises a greater frequency response than the p-channel device. This does not mean that the p-channel device is not being manufactured.

The FET is a single-junction device made up with the Source-to-Drain material (the majority-carrier path) doped in either the "n" or the "p" direction and with the Gate material doped in the opposite direction. By applying voltage so as to oppose the majority carriers in the channel (a negative voltage applied to the gate opposes electron flow in n-channel material—a positive voltage opposes hole flow in p-channel material) the device is back biased. Under these conditions, the n-channel or p-channel material becomes a constrictive layer of dielectric material past which majority carriers must flow and can thus be controlled. See Figure 3.

For a given voltage setting between the gate and the source (bias, if you will), the FET rapidly reaches a point of saturation in the source-to-drain majority-carrier path. This region of the curve gives the FET an effective R_D approaching infinity. This is where an increase in drain voltage (V_D) does not result in an increase in drain current (I_D). This area of the curve is spoken

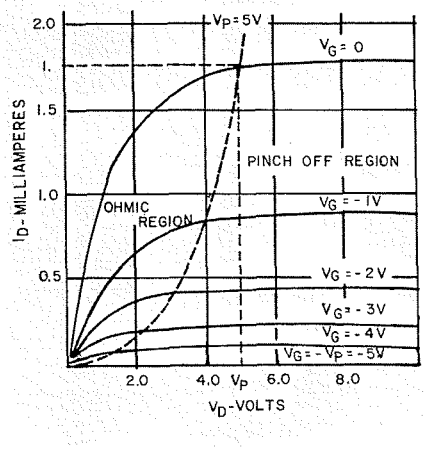

Figure 4. A chart of V_D vs I_D curves of an FET showing the pinch off region and Ohmic region at different values of bias voltage.

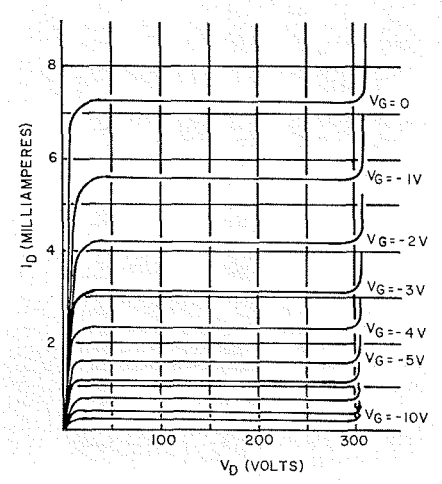

Figure 5. A chart of the V_D vs I_D curves of another FET showing Zener-knee breakdown of Gate-to-Drain back-biased diode. An extension of the curves shown in Figure 4 would reveal a similar tendency of this FET to avalanche at some certain V_D voltage.

of as the "Pinch-Off Region". See Figure 4. The area to the side of this (where an increase in V_D results in an increase in I_D—close to the graph axis) is termed the "Ohmic Region".

A study of the V_D vs I_D curves (see Figure 5) shows that with a given load line, the resultant transfer curve is non-linear. This non-linearity is relative to the deviation in the resistance represented in the majority-carrier path as controlled by the biasing voltage. The best "g_m" occurs under zero bias conditions and the forward voltage at which saturation of this path occurs is called V_p (pinch-off voltage). V_p is counted as a characteristic of the individual device. Thus, in order to find the active g_m at a bias different than zero, we must multiply the zero-bias g_m by the factor one minus the ratio of gate voltage-to-pinch-off voltage raised to the two-thirds power.

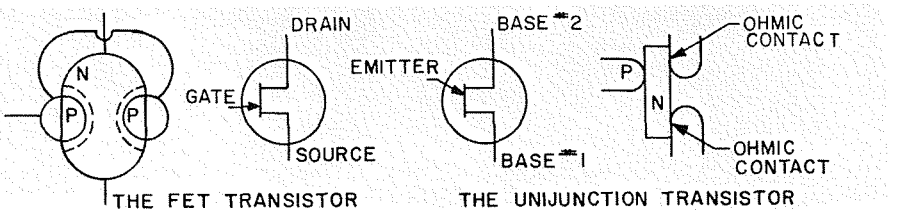

Figure 6. Comparison of an FET and a Unijunction transistor.

Operational $g_m = g_m$ (at zero bias) $\left[1 - \left(\frac{V_G}{V_p}\right)^{2/3}\right]$

Now, with a truly representative g_m available, one can closely predict the voltage gain of the device in a circuit by using the Pentode A_v formula:

A_v = operational $g_m \times R_L$.

Noting that the input to the device is a back-biased diode, one can see that it offers a high input impedance and that this back-biased junction will show a capacitative effect from gate-to-source and from source-to-drain. The latter also gives a miller effect. Note also, that the input-impedance will decrease with increasing frequencies at which the product $\frac{1}{2\pi f C_{GS}}$ becomes comparable to the input resistance. Also, the gain-bandwidth product will be approximately:

$$\text{Gain Bandwidth} = \frac{g_m}{2\pi\ (C_{in} + C_{out})}.$$

Again, similar to the vacuum tube pentode. This dictates the usual compromise between gain and bandwidth when using this device.

The FET should not be confused with the Unijunction Transistor. The theory of operation is totally different, although at first glance, the unijunction transistor looks almost like an n-channel FET. See Figure 6 for a comparison.

The unijunction transistor operates as a current-driven device with a *forward-biased* junction of p-to-n material injecting holes into the n material between the emitter and base #1 thus reducing the ohmic resistance of the contact. The FET operates with a voltage-driven gate and the resultant back-biased junction with the field restricting the majority-carrier flow through the body of the device. The FET, like a vacuum tube, is a normally "ON" device and must be turned "OFF". Conversely, the unijunction transistor is a normally "OFF" device (as a result of the ohmic contacts) and must be turned "ON" by the signal at the emitter—two totally different theories of operation.

To summarize the properties and characteristics of the FET:

A. Input Impedance:

1. The FET is a high-input impedance device, the input terminal is essentially looking into a reverse-biased junction.
2. The FET has input capacitance that varies inversely with V_{SG} (bias). See Figure 7.

B. Mode of operation:

1. The FET is a voltage-controlled device just as a vacuum tube pentode.
2. The FET has a very, very high R_o (R_p) characteristic similar to a vacuum tube pentode.
3. The FET has a consistently non-linear g_m characteristic.

C. Output Impedance:

1. The FET is a high-output impedance device (current source). However, different means of manufacturing

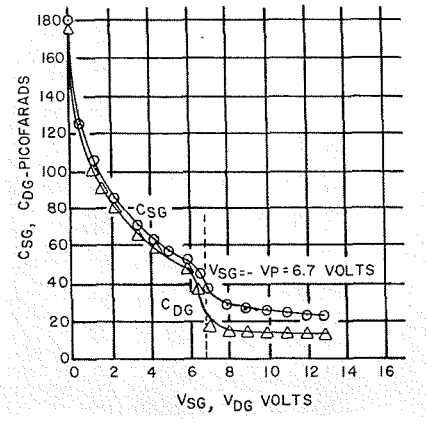

Figure 7. Variation of Source-to-Gate and Drain-to-Gate capacitance with voltage.

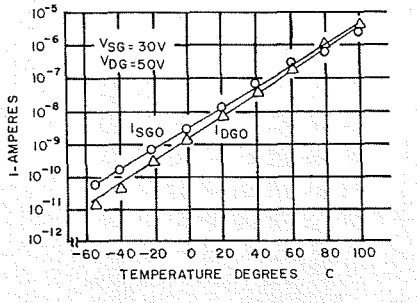

Figure 8. Plot showing leakage current from Source - to - Gate (I_{SGO}) and Drain - to - Gate (I_{DGO}) against temperature under zero bias conditions.

may result in relatively low ratings of this characteristic in comparison with the vacuum tube pentode.

Another noteworthy characteristic of FET's is their built-in protection against thermal run away. Because the input is a back-biased diode, the thermal-sensitive backward current (leakage current) flows from both the source-to-gate (I_{SGO}) and drain-to-gate (I_{DGO}). Plotting this linear current against temperature under zero bias conditions of the other element gives two straight line projections as shown in Figure 8.

This increase in leakage current in the gate junction has a resistive effect on the majority-carrier path resulting in a lower saturation current for a given bias voltage. For a graph of this action under zero bias conditions, and with the forward voltage from the drain to the source set at 50 volts, see Figure 9 (a). A cross graph of g_m and output resistance plotted against temperature is shown in Figure 9 (b). The combination

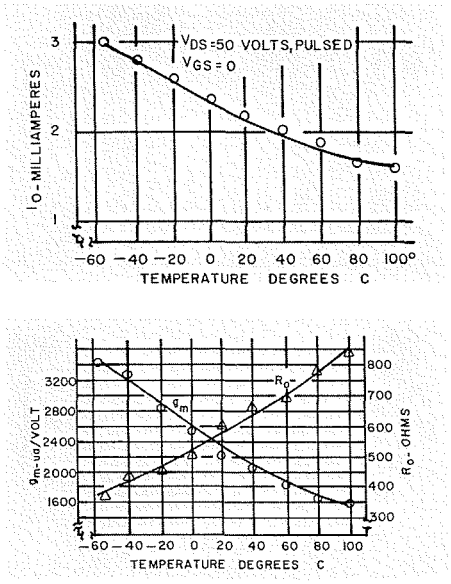

Figure 9. (a) Graph of saturation current under zero bias conditions and with the forward voltage from Drain-to-Source set at 50 volts. (b) Cross graph of g_m and output resistance plotted against temperature.

of these two reactions to temperature is such that as temperature goes up, g_m goes down and R_o (counterpart of R_p in vacuum tubes) goes up. In other words, as the gate starts to lose control of the drain current, a greater portion of the actual drain current will be passed on to the load resistor thus tending to maintain the same change of voltage at the output. This is what we mean when we say that FET's have built-in protection against thermal run away. This statement is not wholly true in the case of MOS (Metal-Oxide-Insulated) FET's.

The MOS FET's separate the gate and channel with a layer of intrinsic material. As temperature increases on this device, the channel apparently increases also as it starts to include some of the insulating layer into the main channel. The MOS FET reacts more to changes in temperature than the regular FET's even though they do away with leakage currents in the gate circuit.

With standard FET's, leakage currents in the gate lead have been reduced to the neighborhood of 0.001 to 0.0001 mA and this can be tolerated where instability of I_D with temperature change cannot.

Characteristic curves of FET's can be displayed on a Type 575 Transistor-Curve Tracer. The EMITTER-GROUND (SOURCE-GROUND) mode is used with the POLARITY control of the Collector Sweep set to NPN (for n-channel FET's) or PNP (for p-channel FET's). The POLARITY control of the Base Step Generator should be set to MINUS for n-channel and PLUS for p-channel FET's.

FET's that require more than 2.4 volts to drive them to cut off—and the great majority are in this category—will require that a 1 kΩ, 1% resistor be connected between the BASE (GATE) and EMITTER (SOURCE) binding posts on the test panel of the Type 575. This, in order to convert the BASE current, as indicated by the STEP SELECTOR switch in MA, to Gate V_{GS} voltage in volts. Thus, 1 mA per step into 1 kΩ gives 1 volt/step and twelve steps at 1 mA per step can give up to 12 volts—ample in most instances to drive any FET to cut off.

The four waveforms represented in Figures 10, 11, 12, and 13 were obtained in this manner. The FET used in these tests was an Amelco U-1346 field effect transistor.

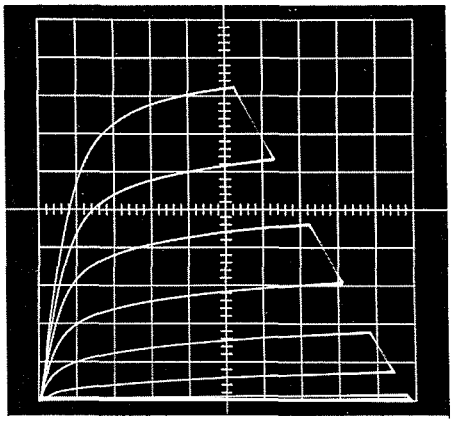

Figure 10. Drain characteristics. V_{DS} (horizontal) = 2 V/cm, I_D (vertical) = 1 mA/cm.

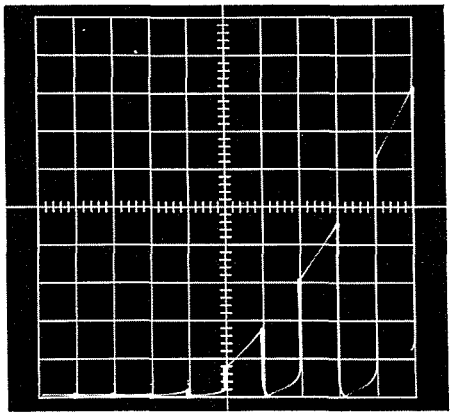

Figure 11. Drain current vs Gate Source Voltage (I_D vs V_{GS} with V_{DS} constant). V_{GS} (horizontal) = 0.5 V/cm, I_{DSS} (vertical) = 1 mA/cm.

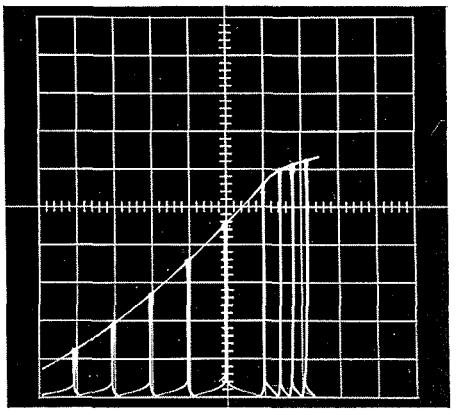

Figure 12. Transfer curve across zero bias. V_{GS} (horizontal) = 0.5 V/cm, I_{DSS} (vertical) = 2 mA/cm. Center vertical graticule line is zero bias. Negative bias to left, positive bias to right of center line. Crowding of markers on right hand side is due to gate drawing current.

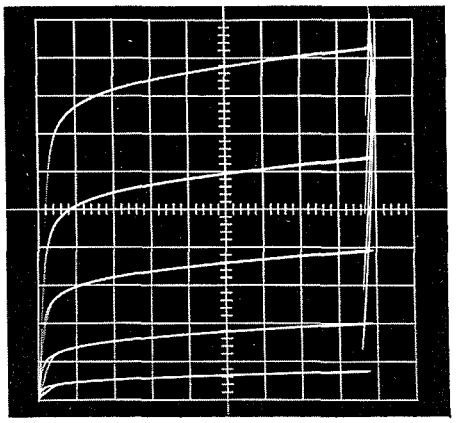

Figure 13. Drain curves showing avalanche (breakover at the Gate-to-Collector Zener Knee). V_{GS} (horizontal) = 5 V/cm, I_{DSS} (vertical) = 0.5 mA/cm.