A Monolithic 14-Bit D/A Converter

RUDY J. VAN DE PLASSCHE AND DICK GOEDHART

Abstract—A monolithic 14-bit D/A converter using "dynamic element matching" to obtain a high accuracy and good long-term stability is described. Over a temperature range from −50° to 70°C the nonlinearity is less that one-half least significant bit ($\frac{1}{2}$ LSB). Dynamic tests show a distortion at a level of about −90 dB with respect to the maximum sine-wave output. Nearly no glitches are found, so the converter can be operated without a deglitcher circuit. The chip, with a size of 3.1 × 3.2 mm, contains all elements needed, except the output amplifier and digital input latches.

A Monolithic 14-Bit D/A Converter

MONOLITHIC D/A converters are the subject of growing interest due to the rapidly expanding market for digital signal-processing systems. The introduction of digital signal processing in sound recording and reproduction systems imposes stringent requirements on the dynamic behavior of the converters. Many of these systems require a 14- to 16-bit resolution to obtain a high signal-to-noise ratio and a good linearity.

In integrated D/A converters an R-$2R$ ladder network with terminating transistors is widely used to generate binary weighted currents. These currents are switched by the bit switches and the conversion form digital information into an analog signal is performed. In Fig. 1 an example of such a converter is shown. There are two main design problems.

The first problem, to which most attention has been paid, is the weighting accuracy problem of the bit currents. The second one, which determines the dynamic performance, is the switching of the accurately weighted currents without glitches. Returning to the accuracy problem, the table in Fig. 1 shows that D/A converters up to 10 bits can be integrated without too many problems. Twelve-bit D/A converters are available on the market [1], but laser trimming of thin-film resistors or Zener zapping techniques are required to achieve the accuracy. How successfully these techniques can be applied to 14- or 16-bit converters is still questionable, and some people have doubts about the long-term stability. Furthermore, in large-volume production, trimming costs cannot be ignored. In this paper a monolithic 14-bit D/A converter is described which uses a different scheme to achieve a high weighting accuracy and good long-term stability. This approach, called "dynamic element matching" [2], needs no trimming and combines a passive division with a time-division concept. Moreover, it is insensitive to element aging.

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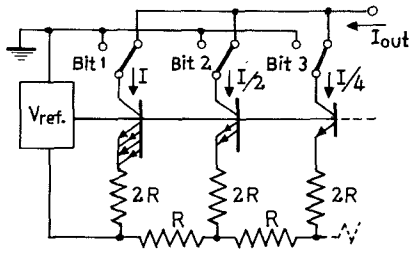

(a)

Fab. process	Matching tolerance			
	σ(%)		mean(%)	
	10μ	40μ	10μ	40μ
Diffusion	0.44	0.23	−0.1	0.07
Thin film	0.24	0.11	−0.1	−0.06
Ion implant	0.34	0.12	0.05	0.05

RESISTOR LINEWIDTH 10μ and 40μ

(b)

Fig. 1. (a) Standard R-$2R$ ladder-network D/A converter. (b) Matching tolerances of different resistor types.

Basic Divider Scheme

A simplified diagram of the divider is shown in Fig. 2(a). It consists of a passive current divider and a set of switches driven by a clock generator f. The total current $2I$ is divided by the passive current divider into two nearly equal parts: $I_1 = I + \Delta I$, $I_2 = I - \Delta I$. The currents I_1 and I_2 are now interchanged during equal time intervals with respect to output terminals 3 and 4. At these terminals currents then flow whose average values are exactly equal and have a dc value I. Fig. 2(b) shows the currents as a function of time. A small ripple current $2\Delta I$ of frequency f is present on the output currents too. This ripple gives a measure of the matching performance of the passive divider. With a simple low-pass filter this ripple can be suppressed and an exact 1-to-2 current ratio is obtained. If the time intervals differ by a value Δt, there is an error in the division ratio equal to:

$$\frac{\Delta I_{3,4}}{I_{3,4}} = \frac{\Delta t}{t} \cdot \frac{\Delta I}{I}.$$

With $(\Delta I/I) \cong 1$ percent and $(\Delta t/t) \cong 0.1$ percent an accuracy of $\cong 10^{-5}$ can be obtained. In a practical circuit a minimum supply voltage of 2 V is needed for good operation of the system. By cascading divider stages an accurate binary weighted current network is formed at the cost of an increase in supply voltage. In a 14-bit current network this leads to an impractically large supply voltage. Therefore, an improved divider scheme must be used to give more weighted currents in one interchanging operation.

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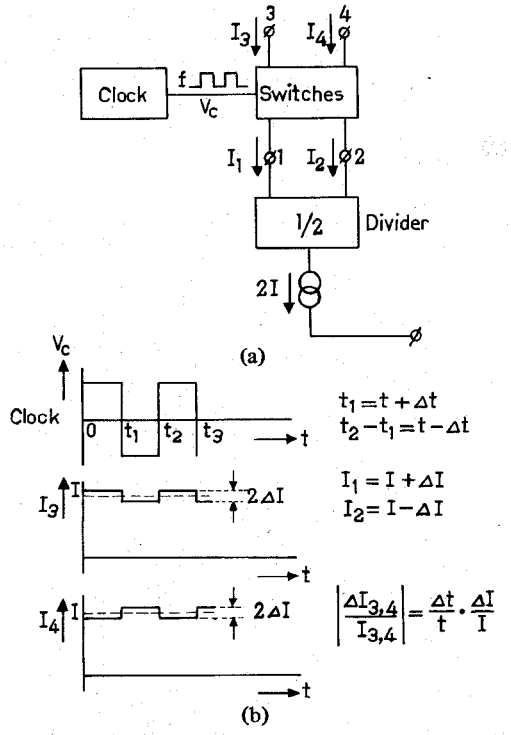

Fig. 2. (a) Basic current divider. (b) Currents as a function of time.

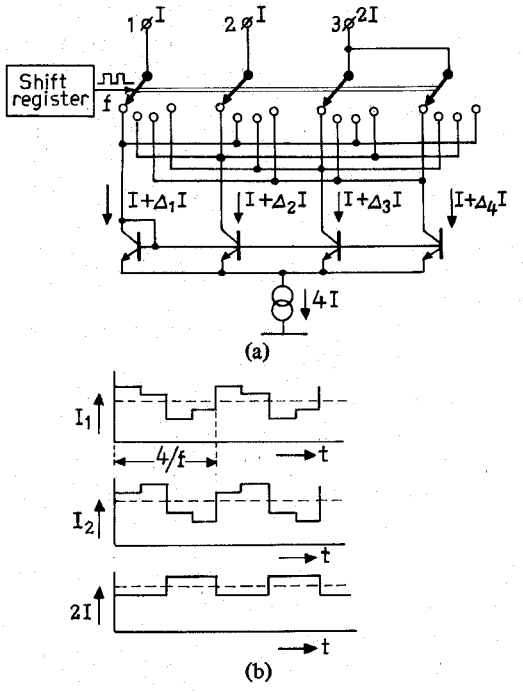

Fig. 3. (a) Improved current divider. (b) Currents as a function of time.

Improved Divider Scheme

In the improved divider circuit the passive current divider is extended to divide a current $4I$ into four nearly equal parts: $I_1 = I + \Delta_1 I$, $I_2 = I + \Delta_2 I$, $I_3 = I + \Delta_3 I$, and $I_4 = I + \Delta_4 I$ [see Fig. 3(a)]. Note that $\Delta_1 + \Delta_2 + \Delta_3 + \Delta_4 = 0$. These currents are now fed into a switching network that interchanges all currents during equal time intervals. These time intervals are generated by a 4-bit shift register. At the output of the switching network, the currents are combined to give values of $2I$, I, and I. The output currents as a function of time are shown in Fig. 3(b). The figure shows that the currents with a value I have a ripple with the same frequency as the clock generator f, while the current with a value $2I$ has a ripple with a frequency $f/2$. Timing errors have the same influence on accuracy as in the system shown in Fig. 2(a).

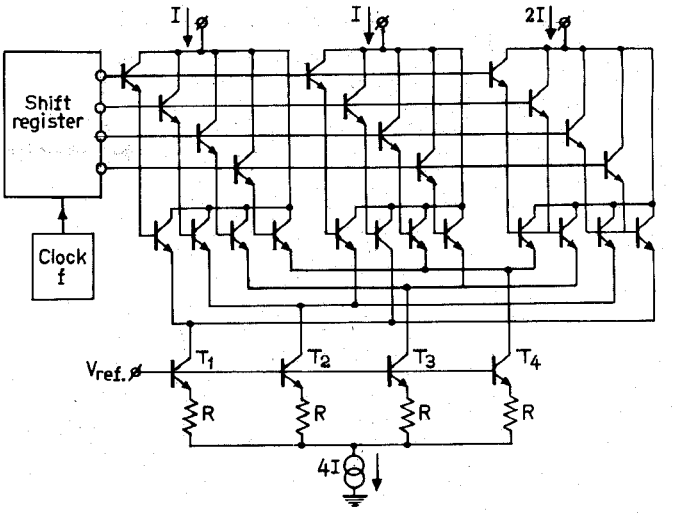

Fig. 4. Practical 2-bit/switching-level current divider.

Fig. 4 shows the circuit diagram of a practical divider. Transistors T_1, T_2, T_3, and T_4, with the resistors R, divide the current $4I$ into four nearly equal currents I. These currents are fed to the interchanging network consisting of Darlington switches to minimize base current loss. In the layout of the circuit, two currents are directly summed by combining the collector islands, which results in an output current $2I$.

A four-stage shift register provides the signals for the interchanging of the currents. The only design criterion for a high division accuracy is a high current gain for the switching transistors.

Binary Weighted Current Network

By cascading current-division stages, a binary weighted current network is formed (see Fig. 5). In the first stage a combination with the reference current source I_{ref} and a current amplifier is used as an accurate current mirror. The reference current itself is used as the most significant bit current (MSB), which has the advantage that filtering is not required. There is a tradeoff between circuit yield and minimum supply voltage. To obtain 14-bit accuracy, a choice between the number of switched and nonswitched current dividers must be made. A high circuit yield is found with five switched stages followed by a 4-bit passive divider using emitter scaling.

Filtering and Switching

How the output currents of a switched divider stage are filtered and switched to the output line is shown in detail in Fig. 6. A first-order filtering operation is used (C_1R_1, C_2R_2) for which external capacitors are added to the chip (C_1, C_2). Additional Darlington cascode stages (T_3, T_4 and T_5,

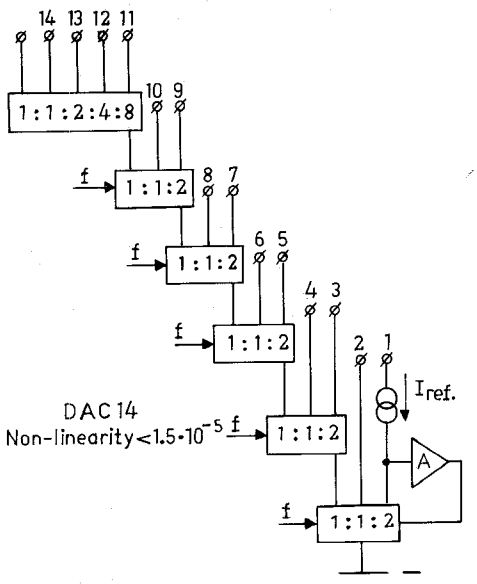

Fig. 5. Binary weighted current network.

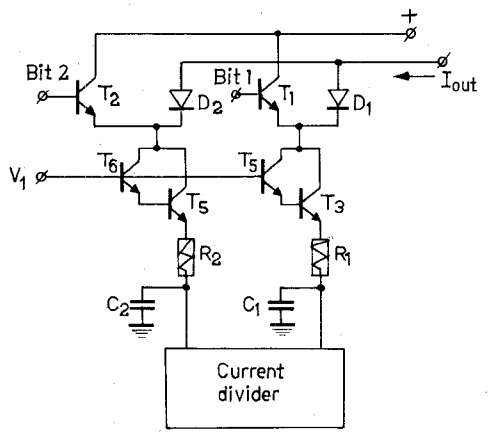

Fig. 6. Detail of the filtering and switching circuit part.

T_6) isolate the filtering operation from the switching of the binary weighted bit currents. The individual filtering of the bit currents minimizes the noise of the converter output current. Bit switching is performed with a diode transistor configuration (T_1, D_1, and T_2, D_2), yielding rather fast and accurate switching with no loss of base currents.

Practical D/A Converter

The circuit diagram of the complete D/A converter is shown in Fig. 7. The 14-bit binary weighted current network, the reference current source, cascode stages with filtering elements, and the bit switches are easily recognized. The shift register for the interchanging consists of a gated master-slave flip-flop driven by an emitter-coupled multivibrator (bottom left side). Provisions are available for obtaining individual filtering of the ripple currents of the most significant bits. When this filtering is used, the conversion speed is determined only by the speed of the bit switches.

Measurements

An important parameter of a D/A converter is the linearity. If the linearity is better than one-half a least significant bit ($\frac{1}{2}$ LSB), the converter is automatically monotonic. Fig. 8

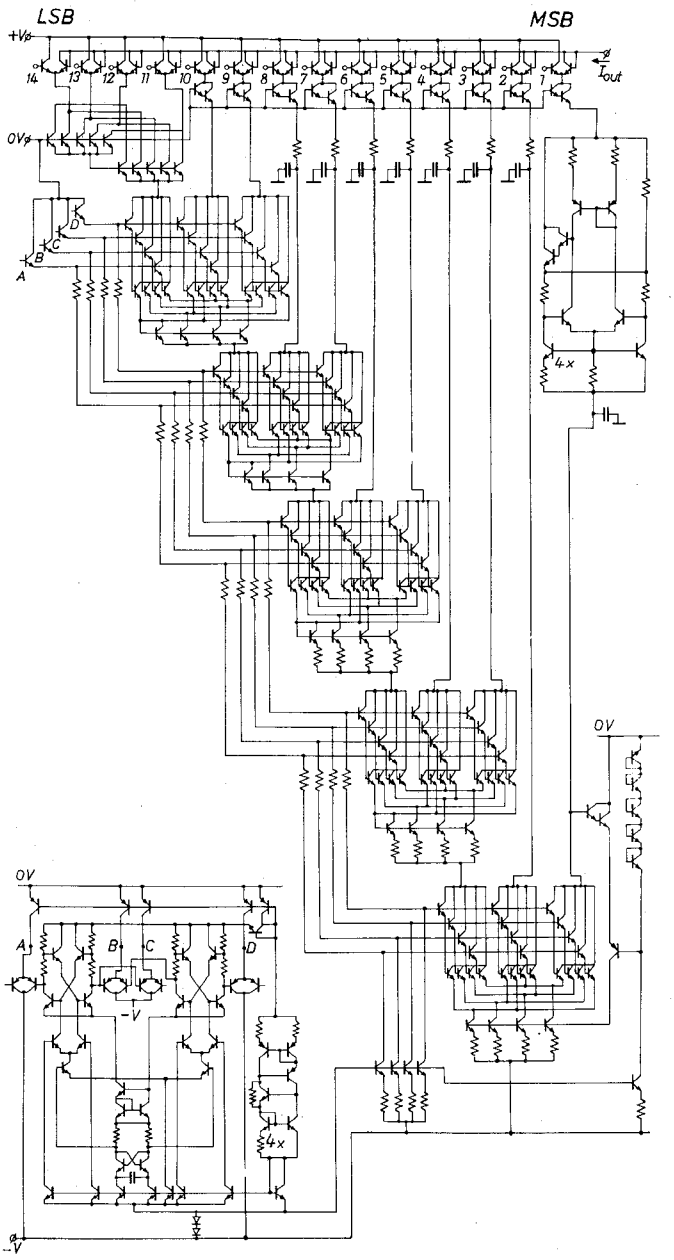

Fig. 7. Complete circuit diagram of a 14-bit D/A converter.

shows the results of a linearity measurement as a function of temperature. Over a temperature range from -50° to 70°C the nonlinearity is less than $3.10^{-5} = \frac{1}{2}$ LSB. With the test scheme in Fig. 9 some dynamic tests were carried out as follows.

Out of a digital sine-wave source 14-bit words at a clock rate of 50 kHz are latched. The outputs of the latches directly drive the switches of the D/A converter. The output current of the converter is converted into a voltage by means of a very high-speed operational amplifier with feedback resistor R. The output signal of the operational amplifier is analyzed with a spectrum analyzer and an oscilloscope. Spectrum analyzer results are shown in Fig. 10(a)-(c). Sine-wave frequencies in these cases are about 600 Hz, 9 kHz, and 18 kHz, respectively. The results show that the distortion is at a level of about -90 dB with respect to the maximum sine-wave output. This -90 dB level corresponds to the limit of the spectrum analyzer, too.

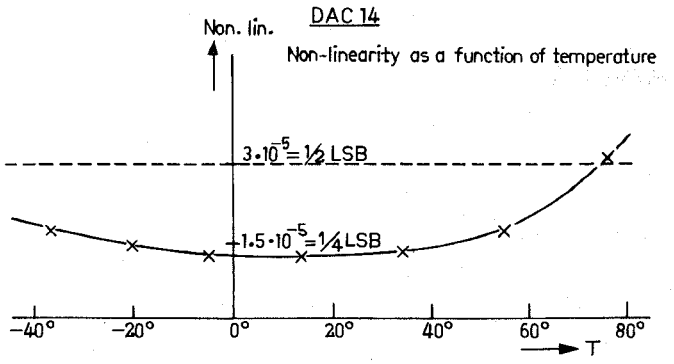

Fig. 8. Nonlinearity of the 14-bit D/A converter as a function of temperature.

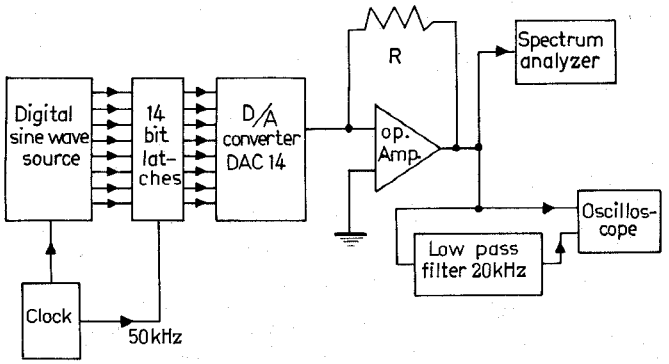

Fig. 9. Measurement scheme to determine distortion and output pulse response.

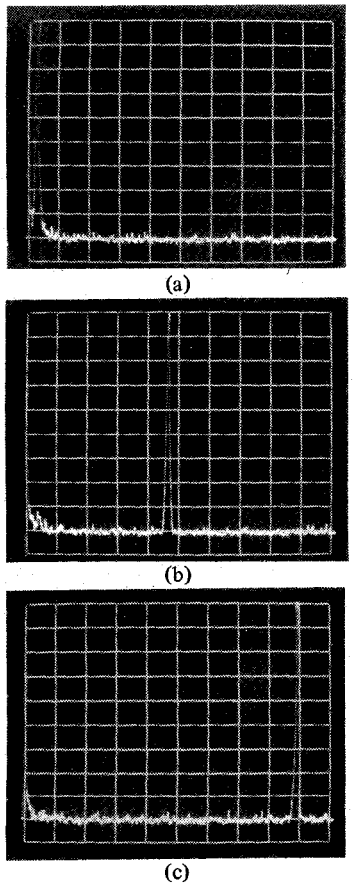

Fig. 10. (a) Distortion of an output sine wave of about 1 kHz. Horizontal 2 kHz/cm. Bandwidth 30 Hz. Vertical 10 dB/cm. (b) Same for an output of about 9 kHz. (c) Same for an output of about 18 kHz.

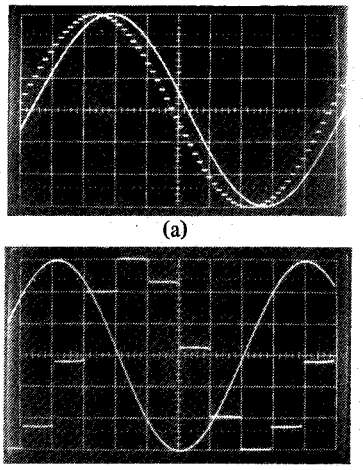

Fig. 11. (a) Filtered and nonfiltered output signals for a 1 kHz output frequency. (b) Same for an output frequency of 6.3 kHz.

TABLE I
D/A CONVERTER SPECIFICATIONS

D/A Converter data :	
Resolution	14 bits
Linearity	±¼ LSB at T = 25°C ±½ LSB −50°<T<70°C
Output current	2 mA
Conversion speed	10 μsec to ½ LSB
Temp. coeff. of output current	5 ppm/°C
Chip size	3.1x3.2 mm
Optimum interchanging freq.	2.5 kHz
Power supply	+5V and −15V

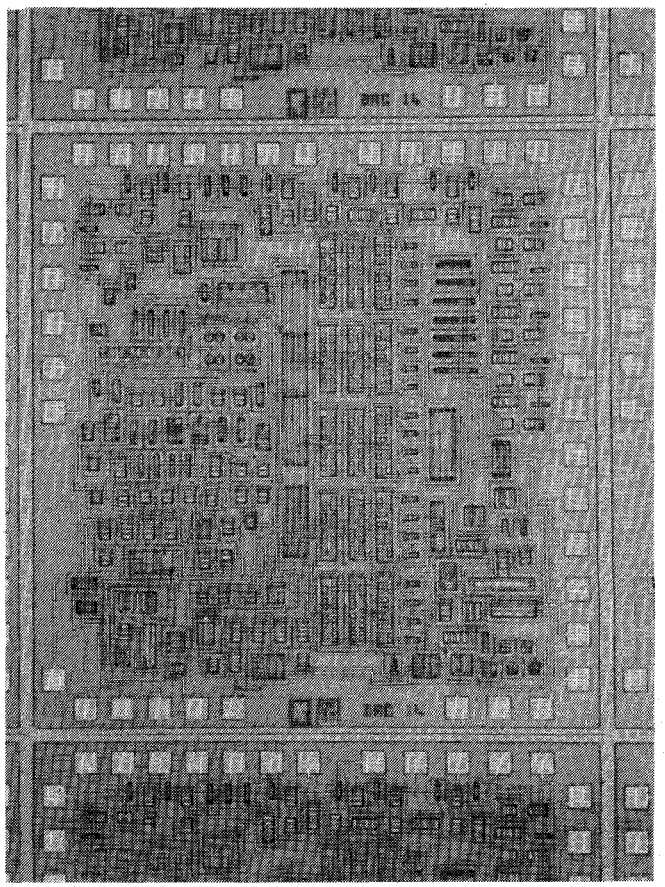

Fig. 12. Photomicrograph of the D/A converter chip.

The results of the oscilloscope display are shown in Figs. 11(a) and (b) for sine-wave frequencies of 1 kHz and 6.3 kHz, respectively. A synchronization mechanism between sine-wave and clock frequency is needed to obtain a stable display. This reduces the number of output frequencies that can be displayed. The delay between the stepped and the filtered sine wave is introduced by the low-pass filter. The photographs show no glitches and a good step response.

D/A Converter Data

Some converter data are shown in Table I. Note that the given settling time corresponds to a D/A converter with filtering applied to the bits.

A photomicrograph of the chip is shown in Fig. 12.

Conclusion

The dynamic element matching method provides a simple, accurate, and reliable design procedure for high-accuracy monolithic D/A converters. The method requires no costly trimming procedures and is insensitive to process variations and aging of components. The good long-term stability and the low noise of the filtered bit currents are major advantages of the system.

The good dynamic performance of the converter described makes it very suitable for sound-reproduction and recording systems.

Acknowledgment

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Rudy J. van de Plassche, for a photograph and biography, see this issue, p. 531.

Dick Goedhart was born in Arnemuiden, The Netherlands, on January 6, 1949. He received a degree in electrical engineering from the Technical College in Flushing, The Netherlands, in 1973.

In the same year he joined the Philips Research Laboratories, Eindhoven, The Netherlands, where he was engaged in an instrumentation group. He is working in this group on the design of linear integrated circuits.

A Single-Chip A/D Converter in PMOS Technology for Digital Voltmeter Applications

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Abstract—**A single-chip A/D converter in p-channel MOS enhancement depletion-mode technology is presented, using a single-slope conversion technique. The analog part consists of a constant-current source and a comparator with internal digitally corrected offset. The A/D converter for a $3\frac{1}{2}$-digit DVM can be operated with only two external components (integration capacitor and oscillator capacitor) and is mounted in a DIL 18 package.**

I. Introduction

SINGLE CHIP digital voltmeter circuits, which have been available for some years, are mostly fabricated in complicated IC technologies, as, for instance, MOS-bipolar combinations [1], [2]. Chips in simpler technologies often need a great deal of external circuitry for compensation and stabilization of the analog parts of the integrated circuits.

In the study presented, possibilities to circumvent these problems are shown.

First the design targets are summarized. A $3\frac{1}{2}$-decade voltmeter has been constructed, which is sufficiently accurate for a wide range of applications. The circuit is fabricated in a standard PMOS metal-gate enhancement-depletion line. Fabrication in this line should give the same yield as typical digital circuits of that complexity. That means that wide tolerances in etching patterns, misalignments, and transistor parameters, which are found in standard lines must, to the same extent, also be tolerated by the analog parts of the circuit.

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