Non-slewing audio power amplifier

Advancing his 'non-slewing' technique, which enabled an instrumentation amplifier capable of ±1000V/µs, Giovanni Stochino now applies the principles to audio power amplification.

In a recent article[1] some high slew rate voltage feedback amplifier architectures were presented and discussed. A virtually non-slewing 50Ω power amplifier configuration was finally proposed, where high speed is accompanied with low input offset voltage and noise, as well as with low total harmonic distortion in the audio frequency range.

In this article I show how the same basic principles, embodied in Fig. 9[1], with appropriate adaptations, can be applied to the design of high performance audio power amplifiers.

Non-slewing amplifier performance

In non-slewing architectures, as explained in the previous article[1], all main slewing mechanisms are virtually eliminated. Therefore, when the input signal is within the common mode input voltage range, the current at the output of both input and intermediate gain stages, is always controlled by the differential input voltage $V_d=V_1-V_2$.

Figure 1 allows us to compare the performance of a non-slewing amplifier, nsa, with a similar yet conventional and slewing architecture, or csa. For clarity, only the input and intermediate stages are detailed, while the output stage is shown in the form of an ideal voltage follower.

Biasing currents are the same in both nsa and csa configurations. The results of Spice simulation for an input stimulus consisting of a 10kHz square wave with a superposed high frequency sinusoidal voltage of 500kHz are shown in **Fig. 2**.

It is apparent that the non-slewing architecture has no visible transient intermodulation distortion, while the conventional configuration shows clear signs of the presence of intermodulation distortion due to slewing times T_f and T_r – both of about 7µs.

In **Fig. 3**, transfer curve I_b, which is the intermediate stage output current, versus V_d is shown for both $I_B=0$ and $I_B\neq0$.

Three regions of operation are identified:

I - input and intermediate stage in class-A operation;
II - input stage in class-AB, intermediate stage in class-A operation;
III - input and intermediate stage in class-AB operation.

Transconductance $g_m=I_b/(V_1-V_2)$ in these regions is approximately as follows:

$$g_m(I)=2/(R_e+2V_T/I_A) \text{ (small signal)} \quad (1)$$

where $V_T=kT/q$ is the thermal voltage of around 25mV at ambient temperature , and,

$$g_m(II)=2/(2R_e+R) \quad (2)$$
$$g_m(III)=1/(2R_e+R) \quad (3)$$

Maximum positive and negative current $I_{b(max)}$ at node B is defined by the maximum input voltage $V_{max}=V_{EBO}+V_{be(on)}$ that should never be exceeded, according to the following relationship:

$$I_{bmax}=(V_{max}-2V_{be(on)})/(2R_e+R)$$
$$=(V_{EBO}-V_{be(on)})/(2R_e+R) \quad (4)$$

Here, voltage V_{EBO} is the rated base-emitter reverse voltage of input transistors. If, for instance, V_{EBO}=6V, R_e=50Ω and R=200Ω, equation (4) yields 18mA. This value, added to I_B , is enough to sustain a rate of change – still linear – of ±160V/µs across a capacitance

Performance of the 'non-slewing' amplifier.

Test conditions: ambient temperature=20°C; $V_{cc}=V_{ee}$=55V regulated.

- Gain=30dB
- Output power 20Hz-20kHz, 110W/8Ω; 180W/4Ω
- Small signal –3dB bandwidth, 800kHz (at node F before output inductor)
- Input offset voltage, 4mV
- Maximum output voltage rate of change, ±170V/µs (at node F)
- Overload recovery time (up to 300% input overload) ≤120ns
- Distortion, see Table 1.

Table 1. THD+noise of circuit in Fig. 4, bandwidth 80kHz.

V_{out} (V_{pp})	thd+noise(%) 8Ω load		thd+noise(%) 4Ω load	
	1kHz	20kHz	1kHz	20kHz
10	0.004	0.016	0.004	0.050
20	0.003	0.020	0.004	0.040
40	0.003	0.030	0.008	0.040
60	0.003	0.040	0.009	0.050
80	0.004	0.045	0.010	0.060

thd+noise instrumentation=0.002%

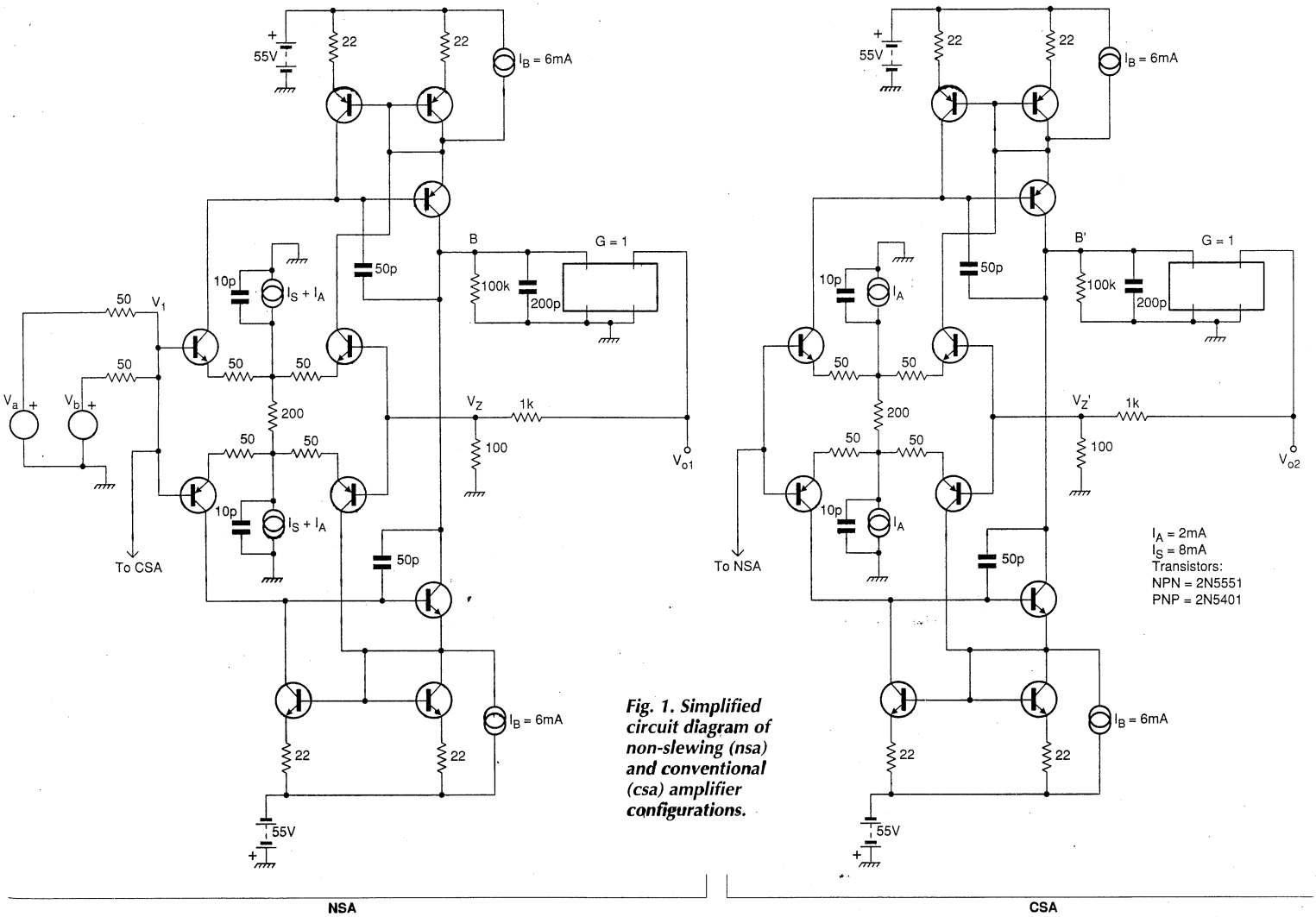

Fig. 1. Simplified circuit diagram of non-slewing (nsa) and conventional (csa) amplifier configurations.

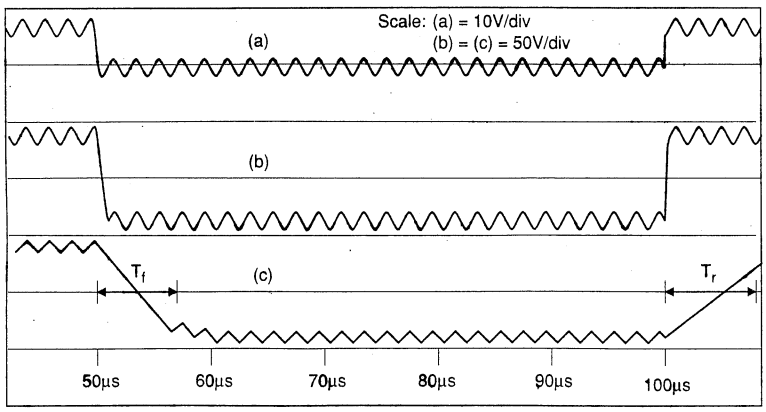

Fig. 2. Spice simulation results demonstrate the absence of visible TIM in non-slewing architectures. (a) is $(V_a+V_b)/2$, (b) is output of non-slewing amplifier, V_{o1}, and (c) is output of conventional slewing amplifier, V_{o1}.

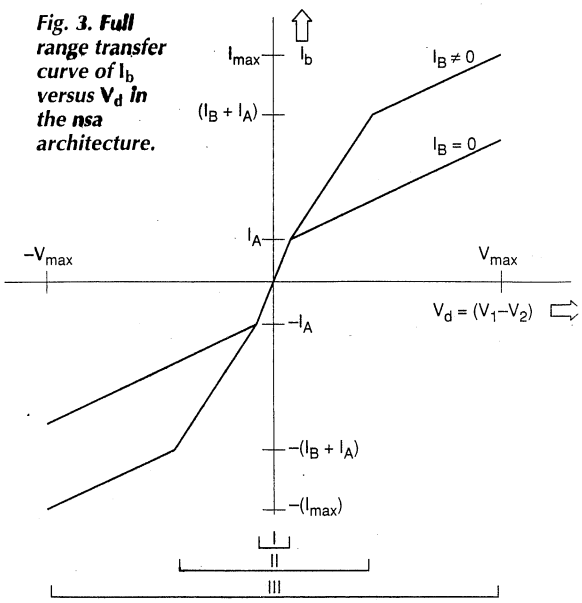

Fig. 3. Full range transfer curve of I_b versus V_d in the nsa architecture.

of 150pF at node B, which is a realistic value in an audio power amplifier.

It is worth noting again that this maximum rate of change is not to be confused with the non-linear slew rate limitation due to input and/or intermediate stage overdrive phenomenon in csa architectures.

The remaining problem in this type of nsa configurations, as well as in all other high slew rate class-AB architectures, is associated with the large full scale non-linearity due to class-AB operation, as is apparent from Fig. 3. This can leave a residue – although rather low – of transient intermodulation products, even when overall feedback is applied to the amplifier. Additionally this limits large signal linearity at high frequency where loop gain is reduced for reasons of loop stability.

An effective way to further limit the already low transient intermodulation distortion in non-slewing audio power amplifier architectures, is to set the bias current of input and intermediate stages so that class-A operation is retained with actual music programs at the maximum expected power and frequency. Considering that the peak current needed to sustain full swing at node B is equal to $2\pi f V_{cc} C_0$, where C_0 includes also the base-collector capacitances of transistors connected to node B, the previous reasoning leads us to set $I_A \geq 1$mA for f=20kHz, when V_{cc}=50V and C_0=150pF. As suggested by Self[2], a safety

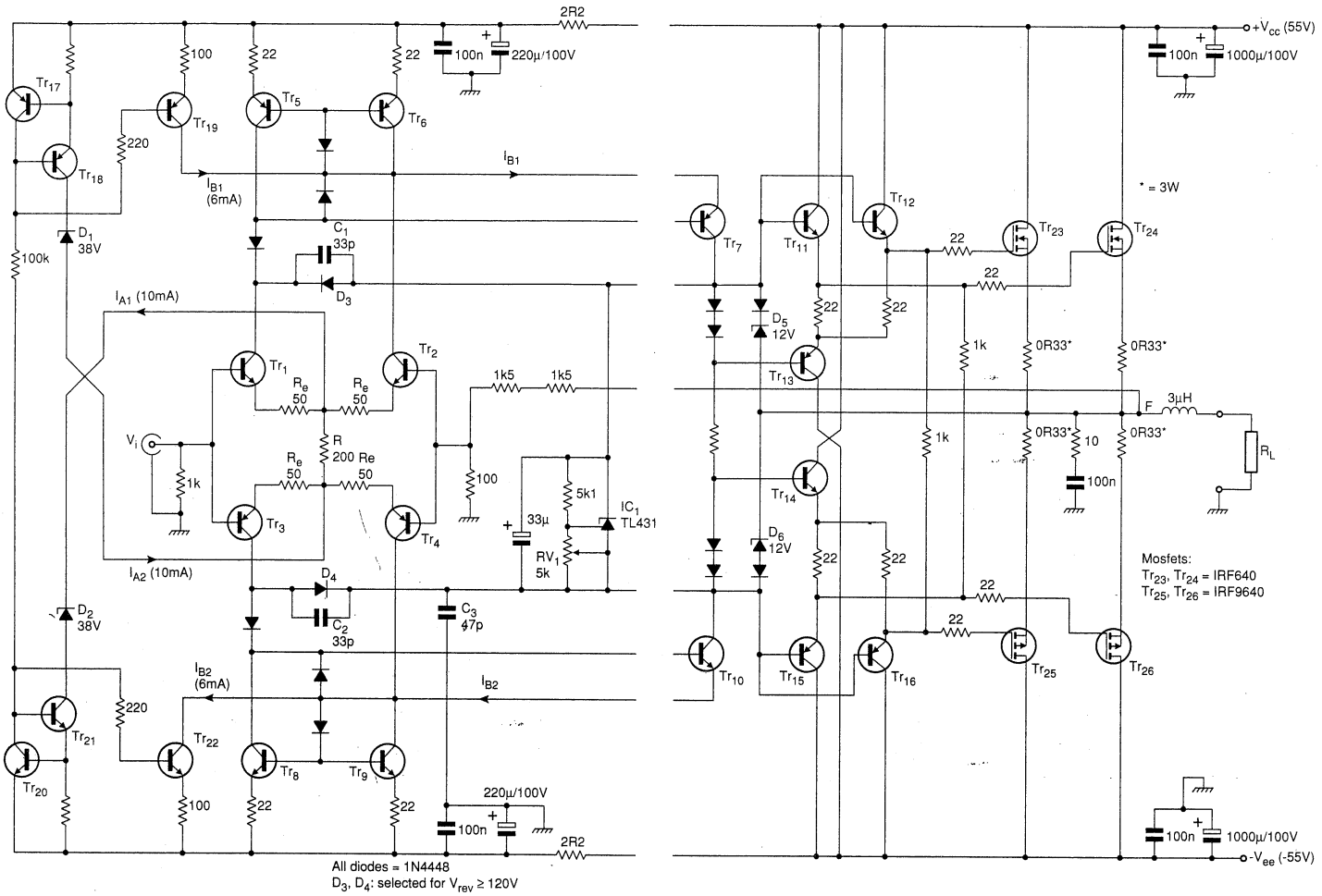

Fig. 4. Detailed circuit diagram of a viable non-slewing audio power amplifier.

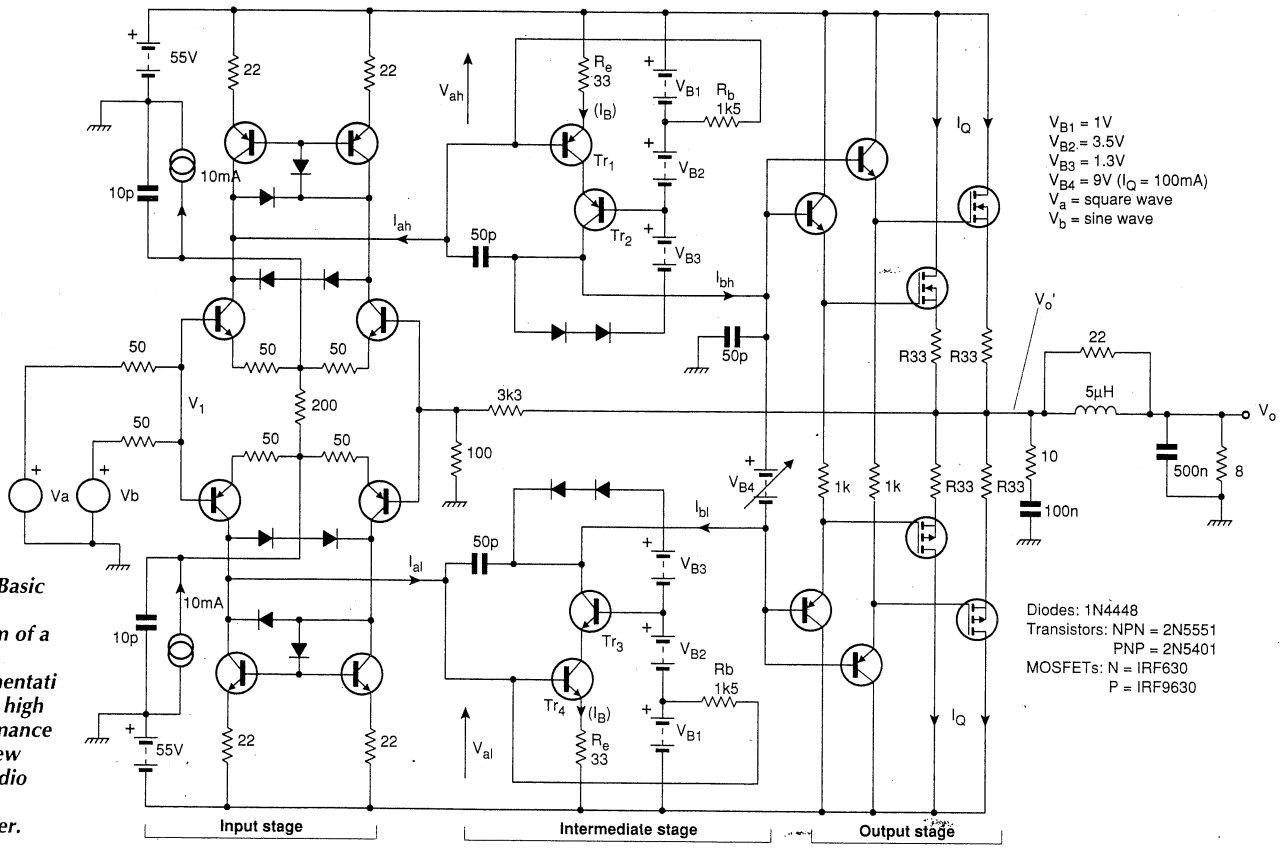

Fig. 5. Basic circuit diagram of a new implementation of a high performance high slew rate audio power amplifier.

margin of about two is recommended. This also takes into account the current contribution needed to drive the output stage and to make up for component tolerances.

In principle, this solution promises very good thd and transient intermodulation distortion performance with normal audio programs. At the same time, it is capable of assuring the very low – if any – transient intermodulation distortion offered by non-slewing architectures, should unexpectedly fast and/or large input transients occur, as maintained by Duncan[3].

Non-slewing, high power audio amplifier architecture

Figure 4 shows the complete circuit diagram of a possible implementation of a non-slewing audio power amplifier, designed bearing in mind the above considerations. If compared with the 50Ω power amplifier of Fig. 9[1] discussed in my previous article, it contains some minor changes.

Firstly, cross coupling resistance R is reduced to 200Ω to improve full range linearity of the input stage and increase its maximum available output current. Current shifting component I_S has been increased accordingly to 8mA, while I_A has been kept at 2mA.

To reduce power consumption of current source transistors Tr_{18} and Tr_{21}, zener diodes D_1 and D_2 have been added. Furthermore, the output stage is built around a double pair of high-power complementary mosfets. These are the *IRF 640* and *IRF 9640*, from International Rectifier.

Each power mosfet can dissipate 125W of power and provide more than 20A peak current. Therefore, the amplifier can safely drive very low impedance loads, provided the output mosfets are adequately heat-sinked.

Transistors $Tr_{11\text{-}16}$, which serve as low output resistance push-pull drivers, are capable of providing the high peak currents needed to drive the high and non linear input capacitances of power mosfets. This can amount to about 800pF worst case each. Peak output current limitation is set to about 40A by zener diodes D_5 and D_6, but a 3-4A fuse has to be inserted at the amplifier output for safe continuous operation.

Due to the high gate-source voltage needed to drive mosfets into full conduction, maximum output voltage swing is limited to about 12V from the supply rails. This results in reduced amplifier efficiency. If needed ,better efficiency can be obtained by operating power mosfets with separate supply rails of ±45V.

Output stage bias current is set by adjustable shunt regulator, IC_1, and by trimmer RV_1. This component has to be set to its maximum before applying power to the amplifier and adjusting bias current of $Tr_{23\text{-}26}$. A suitable value for total mosfet bias current was found to be about 200mA. Unless otherwise stated, resistors are 300mW, 1% metal film types.

Measured performance of the amplifier prototype, which is in good agreement with simulation data, is shown on the first page of this article.

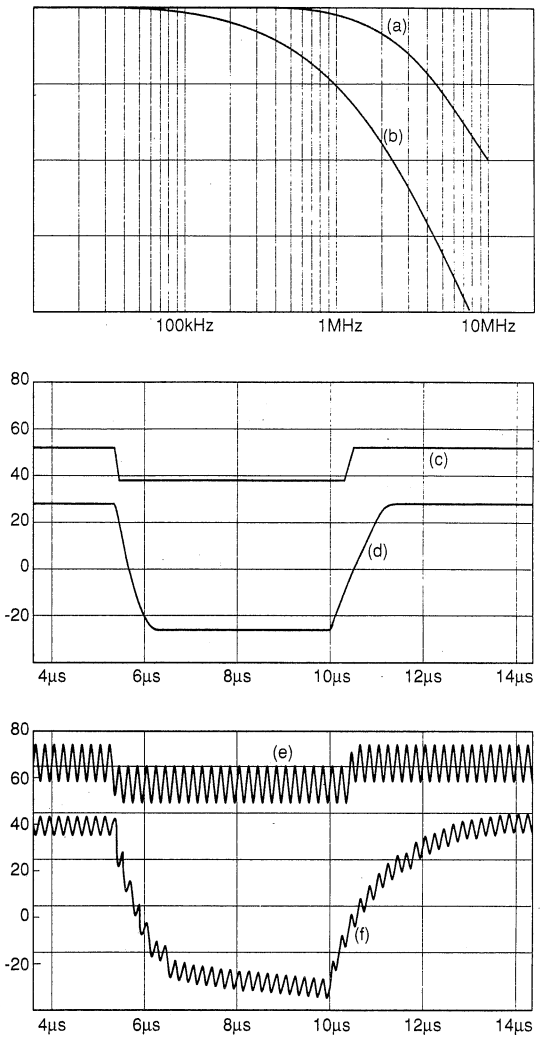

Fig. 6. Some Spice simulation results of the amplifier configuration of Fig. 5:

(a) Frequency response, Magnitude of V_o'/V_1 (10 dB/div)
(b) Frequency response, Phase of V_o'/V_1 (50°/div)
(c) Square wave response, V_1 (2V/div)
(d) Square wave response, V_o' (20V/div)
(e) TIM test, V_1 (5V/div)
(f) TIM test, V_o' (20V/div).

Further developments.

In the last few months I have investigated whether better results can be attained in terms of both maximum rate of change and thd in high slew rate audio power amplifiers configurations.

Figure 5 illustrates the further evolution of the basic power amplifier circuit structure depicted in Fig. 4, which I am currently working on. In comparison with Fig. 4, where the intermediate stage current gain is low (1 to 2), Fig. 5's topology features an intermediate stage with high low frequency current gain, equalling R_b/R_e for $R_b/R_e<\beta$.

With component values shown in the figure, this gain amounts to 45. The expected advantages are increased low frequency open loop gain – and hence lower thd for the same closed loop gain – and potentially higher speed, since the current available at the intermediate stage output is larger than the corresponding current in Fig. 4's architecture.

From Fig. 5 you will find that,

$$I_{ah}(V_d=0)=I_{aI}(V_d=0)=0,$$

therefore bias current I_B is equal to,

$$[V_{B1}-V_{be(on)}]/R_e=9mA.$$

Available peak current is defined by V_{ah} and V_{aI} peak value, ie $V_{a(pk)}$, via the relationship $I_{b(pk)}=[V_{a(pk)}-V_{be(on)}]/R_e$.

In the interests of reliability, this peak current has been limited to about 60mA, by means of the diode clamping networks at the collector of input transistors. These limit $V_{a(pk)}$ to about 2.8V. With this high peak current value it is now possible to sustain slew-rates of ±400V/µs across a 150pF total capacitance at the input node of the output stage.

I cannot provide measurement results yet, however, Spice simulations confirm the above theoretical predictions.

For the moment, I can report the simulation results shown in **Fig. 6**, which demonstrates the frequency response – magnitude and phase – the square-wave response and the square+sine wave response. They prove the stability and clean response of the amplifier – even with a severe 8Ω//0.5µF load impedance. In addition, they show the absence of any visible transient intermodulation distortion. ■

References

1. Stochino, G, 'Ultra-fast Amplifier', *EW+WW*, Oct 1995, pp.835-841.
2. Self, D, 'High Speed Audio Power', *EW+WW*, Sep 1994, pp.760-764.
3. Duncan, B, 'Simulated Attack on Slew Rates', *EW+WW*, Apr 1995, pp.303-309.