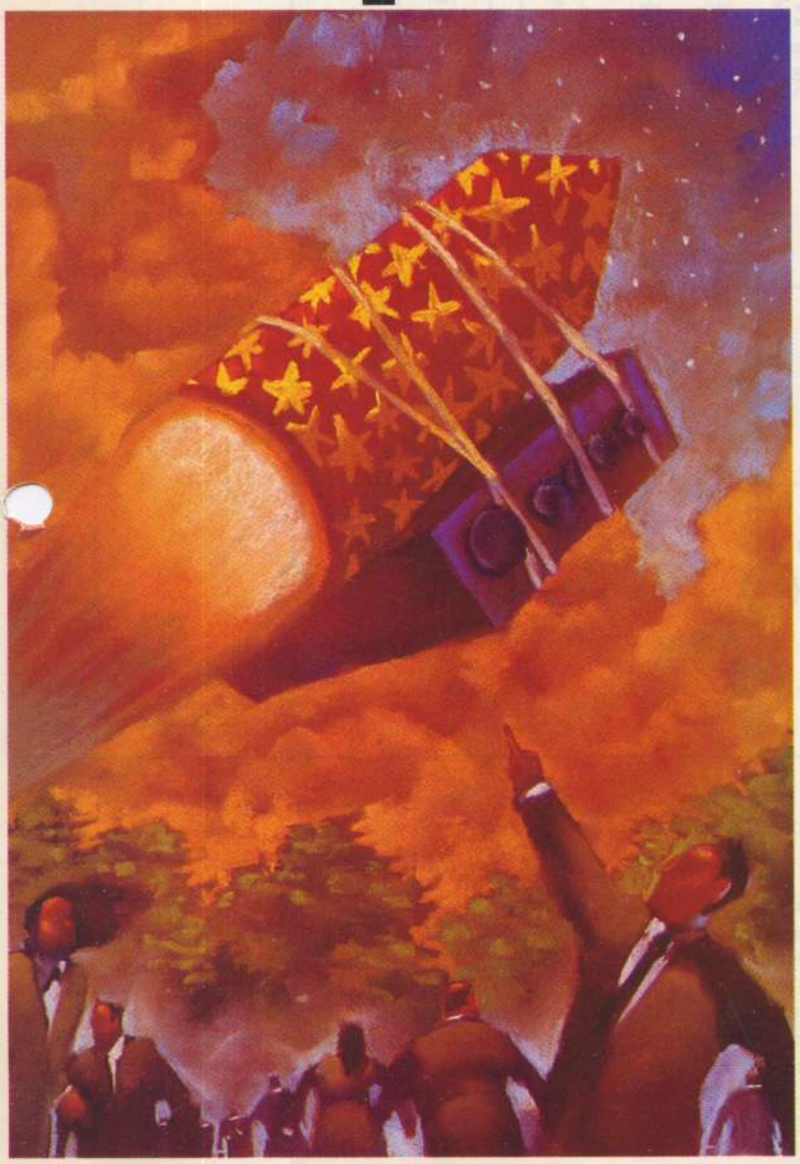
E.W. August 1998

Fast, clean and powerful

Giovanni Stochino has enhanced his ultra fast, low-distortion power amplifier for audio use. Delivering 100W into 8Ω, this design slews at over 300V/μs and features 0.0026% distortion at rated power. In addition, Giovanni has refined the design to make sure that this performance level can be replicated.



Since the publication of my article on the 100W into 8Ω low distortion audio amplifier, I have received a number of letters from *EW* readers interested in implementing a low thd fast amplifier.

I must stress that special care is essential when implementing this amplifier design, since all stages are capable of providing extremely high currents. Wrong connections or occasional shorts during testing can have catastrophic consequences.

Here I present a functionally optimised design, and include instructions for the implementation of a suitable powering scheme. I have also designed and fully tested a pcb, details of which appear later.

Circuit enhancements

Figure 1 shows the detailed circuit diagram of the amplifier which has been implemented. Compared with the corresponding diagram presented in my previous article, i.e. Fig. 3a, some minor changes have been introduced in order to add more flexibility to the design.

In particular, I have introduced dc decoupling into the feedback network via capacitor C_{22} and C_{23}. This is to keep low the output offset voltage even when using a relatively high value of resistor R_{12}, which both provides a return path to ground for the base currents of input transistors Tr_1 and Tr_3, and sets the level of the overall amplifier input impedance.

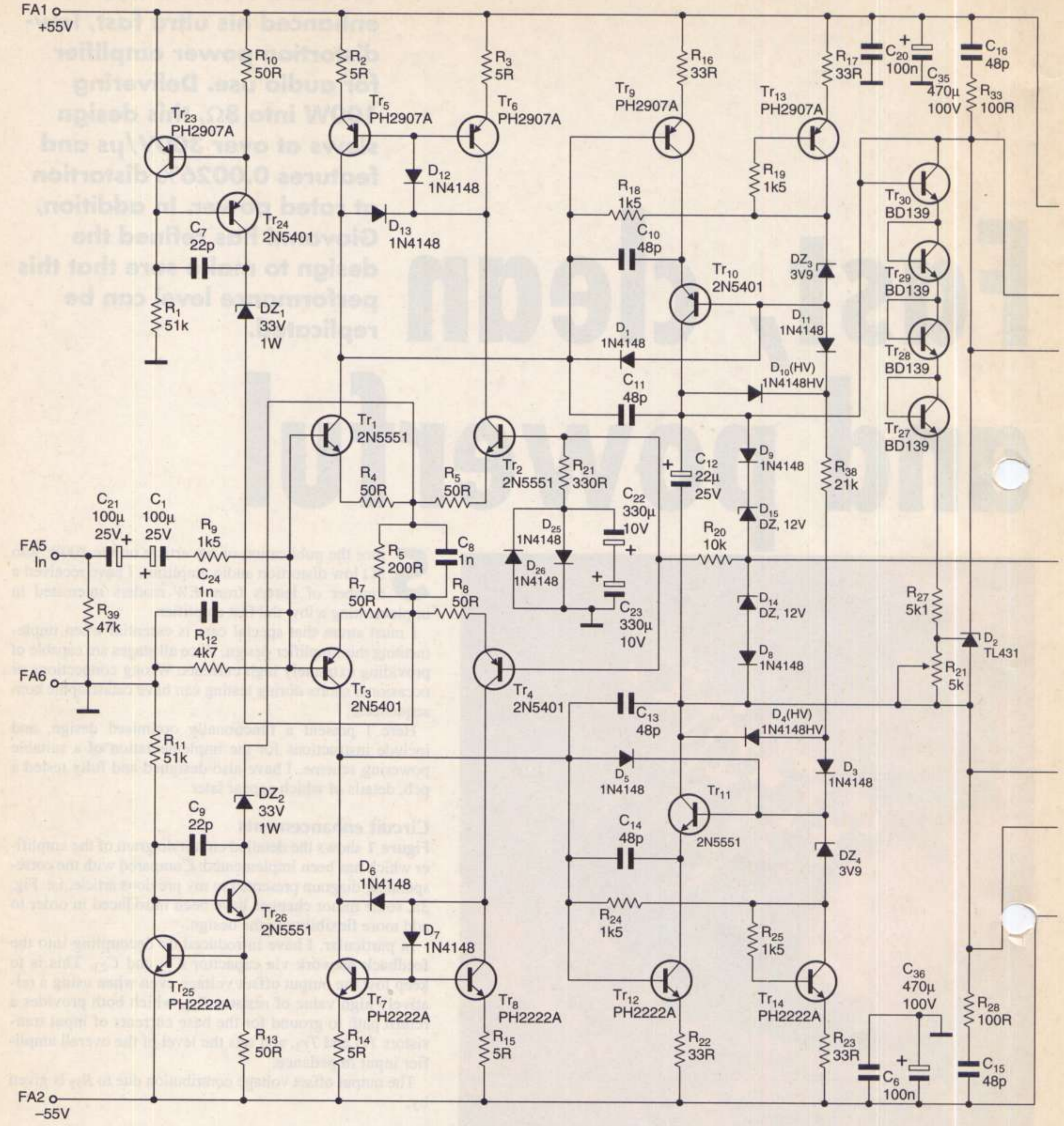
The output offset voltage contribution due to R_{12} is given by,

$$V_{os} = \frac{I_A(\beta_p - \beta_n)}{\beta_p \beta_n} R_{12} G_o \qquad (1)$$

where I_A is the bias current of the input stage transistors, $Tr_{1\text{-}4}$, β_n and β_p are the current gain of n-p-n and p-n-p bipolar input transistors, respectively. Finally, G_o is the closed-loop dc gain of the amplifier.

Typical gain figures when $I_A \approx 2$mA are $\beta_n \approx 150$ for the n-p-n 2N5551 transistor and $\beta_p \approx 70$ for the 2N5401 p-n-p device. While $G_o = 32$, with R_{21} connected to ground, equation (1) yields 2.3V for $R_{12} = 4.7$kΩ.

This offset is unacceptably high. The insertion of dc decoupling reduces G_o to almost unity, so that the worst



case V_{os} is limited to few hundred millivolt. This represents an acceptable level of output offset.

Filtering added. Another change made to increase flexibility is to allow the possibility of incorporating an input pass-band filter, via components C_1 and C_{21}, together with R_{12} for the high-pass section and R_9+C_{24} for the low-pass section.

In the following analysis, C_1 and C_{21} are considered equal to $2C_H$. With component value shown, the –3 dB bandwidth is 1Hz to 120kHz. Assuming that the signal source resistance, which is usually lower than 300Ω, has no influence, high-pass and low-pass frequency corners are given by

$$f_H = \frac{1}{2\pi R_H C_H}$$

and

$$f_L = \frac{1}{2\pi R_L C_{24}}$$

respectively, where R_H is the sum R_{12}+R_9, and R_L is the parallel $R_{12}//R_9$. They are easily adapted, and the low-pass section can be bypassed by omitting C_{24} and shorting R_9.

Improved temperature sensing. The temperature-sensing network *TS* incorporates an additional transistor. This adds

Fig. 1. Detailed circuit diagram of the chosen practical implementation of the 100W/8Ω audio-power amplifier, featuring a speed higher than 300V/μs and rated power thd figures of 0.002% and 0.018% at 1kHz and 20 kHz, respectively. All diodes are 1N4448 Diodes D_4 and D_{10} marked 1N4448HV are still 1N4448, but selected for a reverse voltage higher than 120V. This selection is made by applying a reverse voltage of 130V via a resistor of 10kΩ and measuring the current, which has to be less than 10mA. The yield is normally higher than 50%.

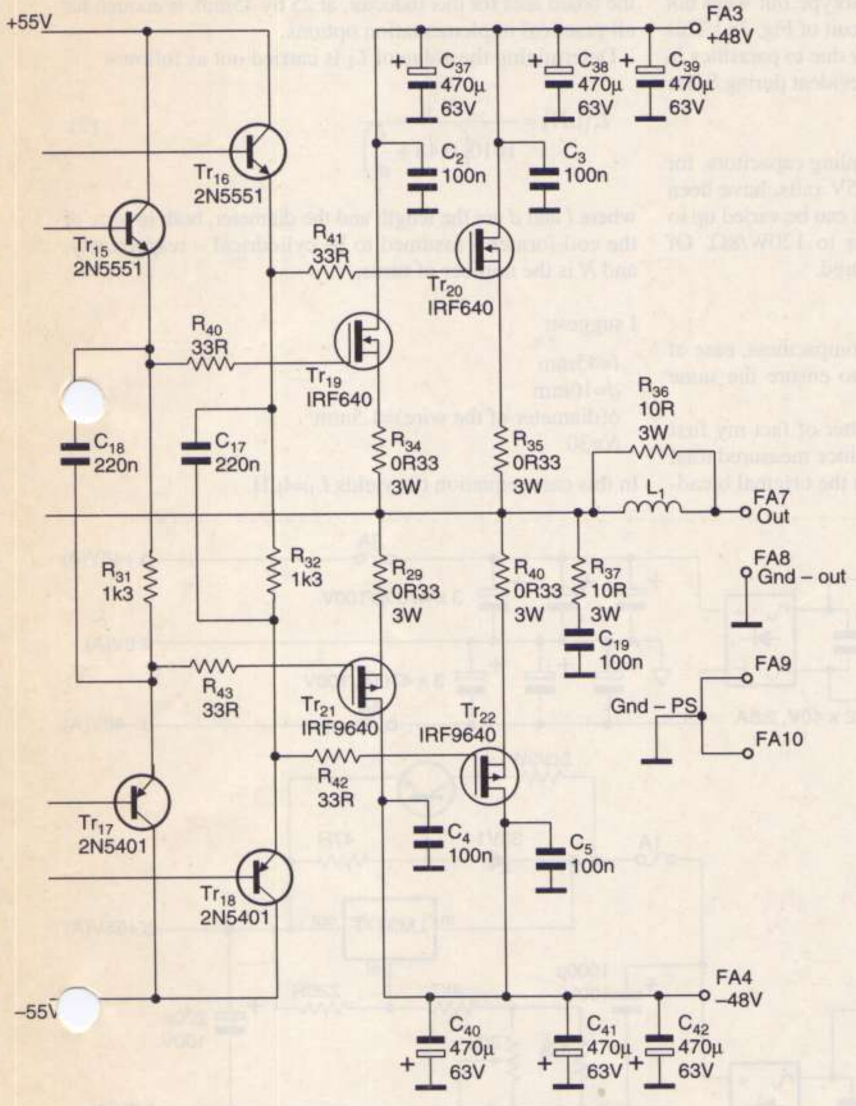


Table 2. Slewing performance of the audio power amplifier for a source resistance of 50Ω and an 8Ω load. Pulse input was 6V peak, as in Fig. 4 of my previous article.[1]

Characteristic results	Measurement
Positive slew-rate	+320V/μs
Negative slew-rate	−300V/μs

Table 3 . Total harmonic distortion figures of the final 100W/8Ω audio power amplifier for a source resistance of 50Ω and an 8Ω load. Quiescent current was 150mA and bandwidth 80kHz.

V_{out}, pk-pk	1kHz	20kHz
5	0.0030%	0.0043%
10	0.0028%	0.0047%
20	0.0023%	0.0061%
40	0.0028%	0.0110%
80	0.0026%	0.0170%

Note: Total harmonic distortion remains virtually constant when source impedance R_s varies in the range 50Ω to 5kΩ. The instrumentation limit, thd+noise, was 0.002% at 1kHz; 0.003% at 20kHz.

extra flexibility to the mounting mode of the temperature-sensing network relative to the power output devices $Tr_{19\text{-}22}$.

In my original prototype, the three sensing transistors were mounted very close to output power mosfets. A total $\Delta V_{TS}/\Delta T$ of −6mV/°C was adequate.

However, when a more practical scheme for mounting the temperature-sensing network on the heat sink is needed, like the one presented here, you have to allow a looser thermal coupling with power devices. Because of this, $\Delta V_{TS}/\Delta T$ will be higher and it may turn out that a greater number of temperature sensing transistors will be needed.

In the layout scheme proposed, four transistors providing a $\Delta V_{TS}/\Delta T$ of −8mV/°C were x found adequate to provide a fairly stable – within 20% – output power mosfets bias setting under a wide range of operating conditions.

The quiescent current of output devices has been set to 150mA, which further contributes to the thermal stability of the operating point of the output mosfets. The

Table 1. Main characteristics of the fast audio power amplifier for 150mA quiescent current and 80kHz bandwidth.

Characteristic	Measurement results
Measured output offset voltage	+32mV
DC open-loop gain	110dB
Low-frequency closed loop gain	32dB
Small-signal bandwidth before the output filter (−3dB)	20Hz (−0.1dB), 1.3MHz
Unity gain frequency before the output filter	22MHz
Open-loop gain at 20kHz	66dB
Closed-loop amplifier phase margin before the output filter	+76°
Output noise (BW=80kHz, input terminated with 50Ω)	42μV rms
Slew rate	See Table 2
Total harmonic distortion (thd)	See Table 3

scheme is flexible in the sense that a different $\Delta V_{TS}/\Delta T$ is easily achieved by bypassing one or more thermal sensing transistors. Remember to make sure to set trimmer R_{26}, i.e. VR_1 in Fig. 3a of my previous article,[1] to its highest value before applying power to the amplifier.

Better stability. Gate resistors $R_{40\text{-}43}$, needed to prevent high frequency oscillation of the output mosfets, are shown in Fig. 1. They were also used in my first prototype but were not reported, inadvertently, on the earlier circuit of Fig. 3a.[1] This oscillation is very likely to occur, mainly due to parasitics in the implementation, but it is not usually evident during Spice simulation.

More decoupling. Power supply decoupling capacitors, for both unregulated 48 V and regulated 55V rails, have been included in Fig. 1. Regulated supply rails can be varied up to 58V in order to increase output power to 120W/8Ω. Of course adequate heat-sink has to be assured.

Is board layout critical?

The amplifier layout was designed for compactness, ease of assembly and alignment, and, finally, to ensure the same level of performance as the prototype.

It has not been an easy task. As a matter of fact my first pcb layout had to be slightly modified, since measured total harmonic distortion was 6dB worse than the original breadboarded prototype. The reason for this poor thd performance was found in the return path for the load current, which was not well controlled.

The final design, however, has proved effective and the amplifier performances are more or less the same as those reported in my previous article.

The value of inductance L_1 should be in the region of 3-5mH. I suggested wire diameter of 1.5-1.8mm. On my pcb, the board area for this inductor, at 25 by 45mm, is enough for all practical implementation options.

Determining the value of L_1 is carried out as follows:

$$L_1(\mu H) \approx \frac{N^2 d}{1010\left(0.45 + \frac{l}{d}\right)} \qquad (2)$$

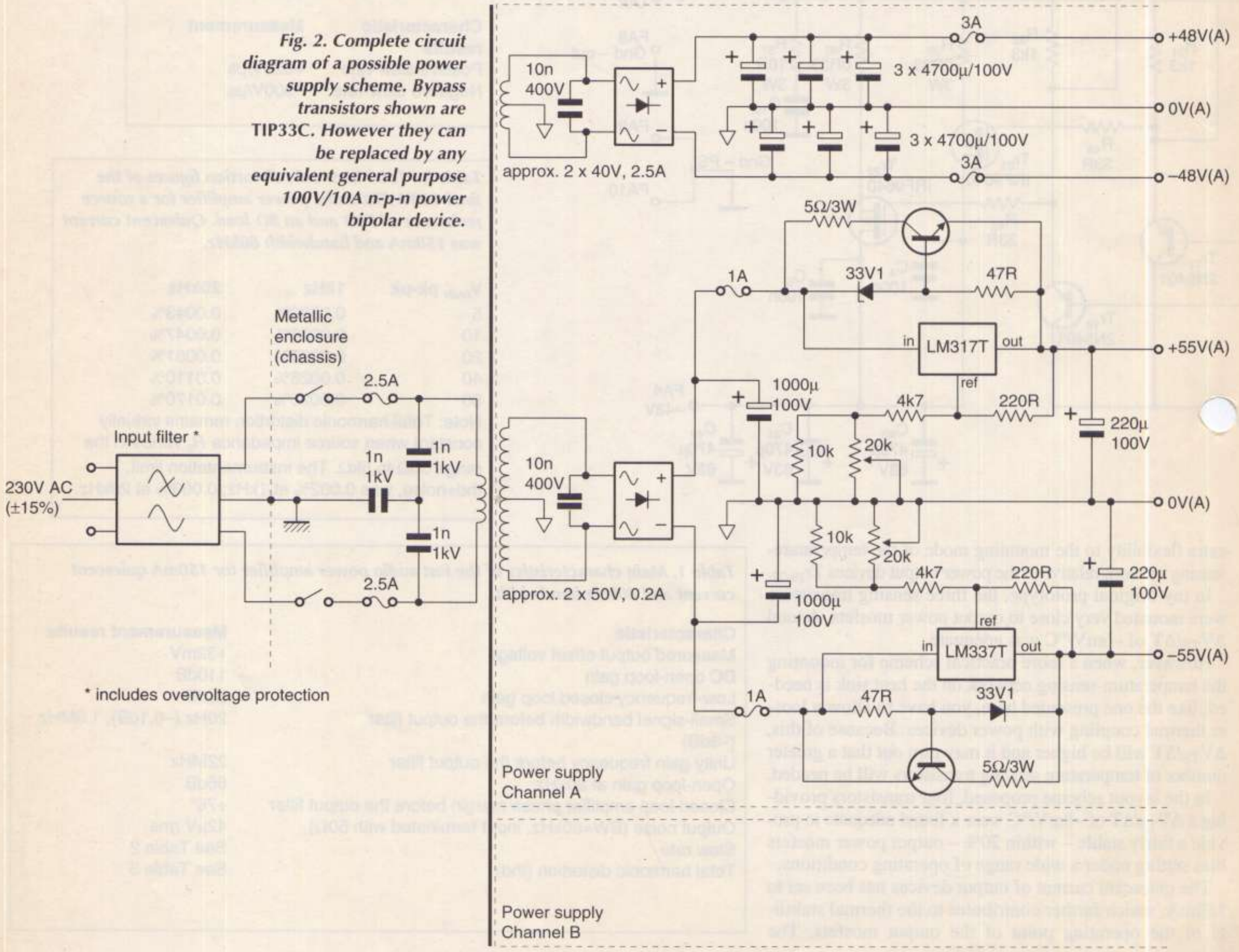
where l and d are the length and the diameter, both in mm, of the coil former – assumed to be cylindrical – respectively, and N is the number of turns.

I suggest:

l=45mm
d=16mm
ϕ(diameter of the wire)=1.5mm
N=30

In this case, equation (2) yields L_1=4μH.

Fig. 2. Complete circuit diagram of a possible power supply scheme. Bypass transistors shown are TIP33C. However they can be replaced by any equivalent general purpose 100V/10A n-p-n power bipolar device.



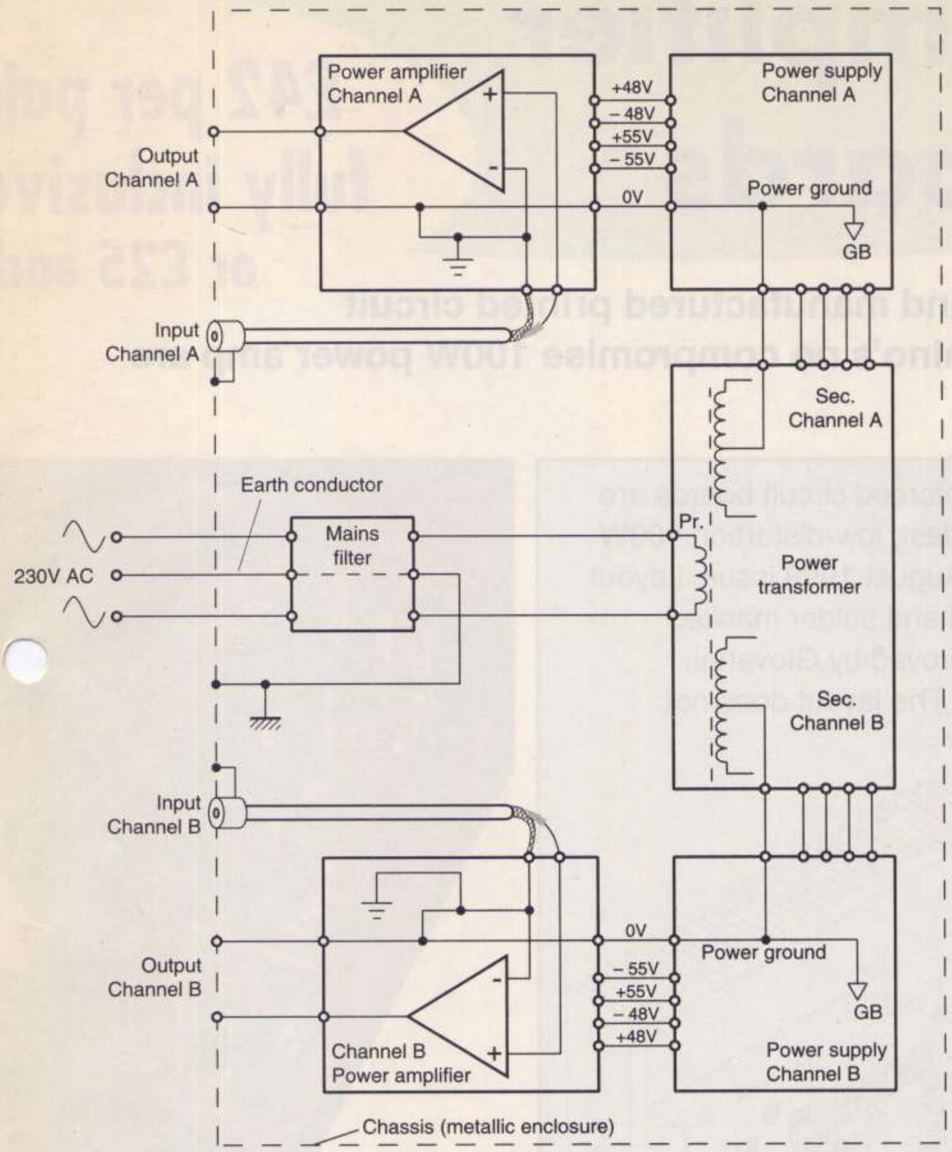


Fig. 3. A practical grounding scheme.

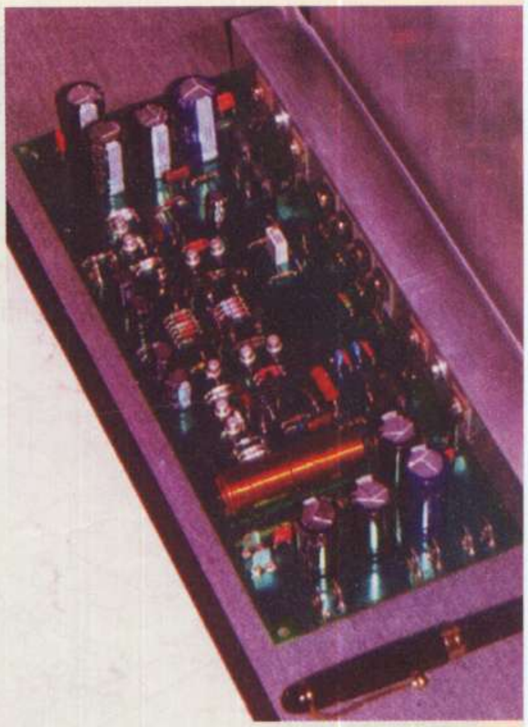


Fig. 4. Photograph of the amplifier printed board assembly prototype.

Power supply

Figure 2 shows a suggested power supply scheme, which is simple, effective and low cost.

Separate power supply sections are recommended in order to avoid ground loops and ensure the optimum signal to noise ratio. One section – channel A – only is shown in detail in Fig. 2.

Regulators *LM317T* and *LM337T* are bypassed by a protection-clamping circuit made up from a 33V zener diode of a few watts, a power resistor and *TIP33C* power transistors. This prevents the maximum input-output voltage difference from being exceeded, which is 40V for both regulators.

Note that, in order to avoid ground loops, the ground references of channel A and channel B have to be joined at a single point, normally at the inputs of the two A and B amplifiers. Connection to the metallic enclosure, i.e. chassis ground, is also usually made here.

Safety is assured by connecting, as usual, the chassis to the safety ground ⏚. The chassis also acts as a metallic shield.

Figure 3 shows a suggested grounding scheme, where the power ground of the power supply ⏚ is connected to the signal ground ⏚ of the corresponding power amplifier.

The outer conductor of the input signal connector of both channels is connected – the usual mechanical connection provides good electrical contact too – to the chassis ground of the mechanical enclosure.

Finally, **Fig. 4** is a photograph of the prototype of the power amplifier used for all measurements.

Verified amplifier performance

Measurements have shown that the performance of the prototype assembled on the final version of the pcb are as good as the performances of the first experimental prototype of the low thd, very fast audio power amplifier.

This fact, in conjunction with the observation that even combining n and p-channel output power mosfet coming from different vendors did not affect distortion performance, is additional proof that the chosen architecture for very fast, low distortion audio power amplification is robust and relatively insensitive to component tolerances and mismatches.

Finally, it is worth mentioning that the amplifier is stable for any value of the input signal source impedance Z_s, consisting of a resistor in parallel with a capacitor, $R_s//C_s$.

Reference

1. Stochino, G, '300V/μs Power', *Electronics World*, April 1997, pp. 278-282.

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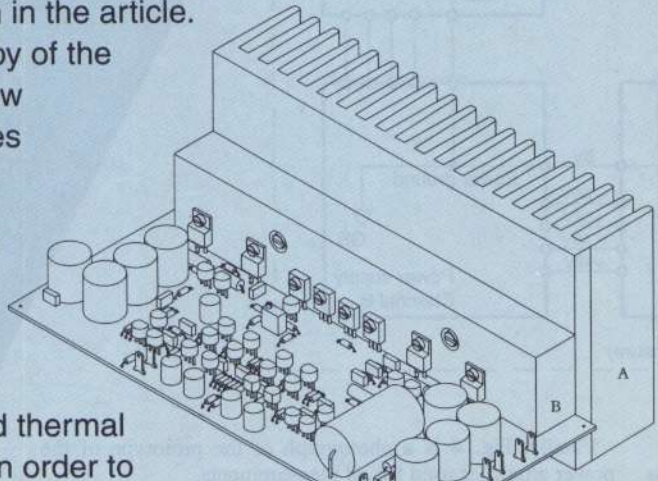

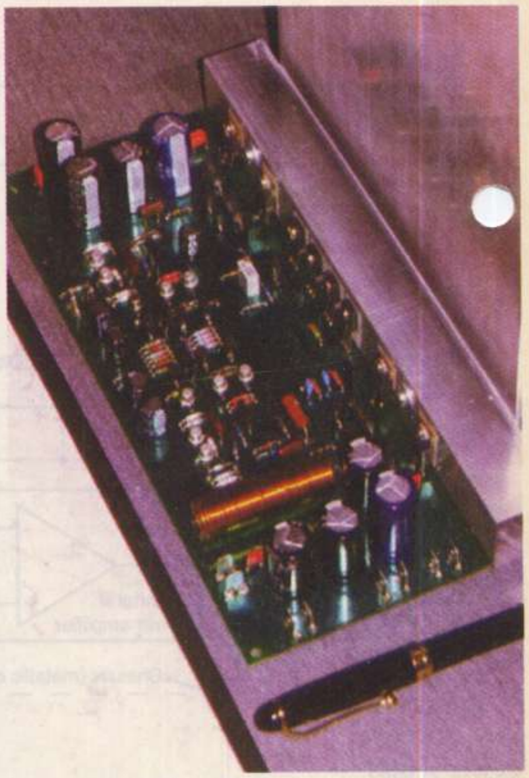

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Specifications

Power into 8Ω load	100W
Small-signal bandwidth before the output filter	20Hz (–0.1dB), 1.3MHz (–3dB)
Unity gain frequency before the output filter	22MHz
Output noise (BW=80kHz, input terminated with 50Ω	42µV rms
Measured output offset voltage	+32mV

Distortion performance

V_{out}, pk-pk	1kHz	20kHz
5	0.0030%	0.0043%
10	0.0028%	0.0047%
20	0.0023%	0.0061%
40	0.0028%	0.0110%
80	0.0026%	0.0170%

Slew rate

Positive slew-rate	+320V/µs
Negative slew-rate	–300V/µs