

Precision DC-to-AC Power Conversion by Optimization of the Output Current Waveform—The Half Bridge Revisited

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Abstract—A simple form of a buck-derived interleaved four-quadrant pulsewidth modulation (PWM) power stage results in a doubling of the output ripple frequency while greatly reducing the ripple current amplitude. Shootthrough currents are reduced to low d_I/d_t events that are readily controlled, allowing zero dead-time operation.

Index Terms—Amplifier, class-I amplifier, control, full-bridge, half-bridge, inverter, modulation, PWM.

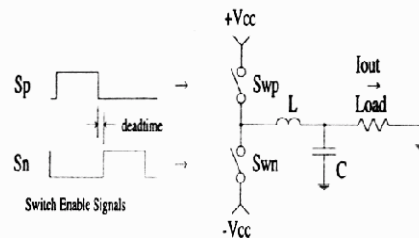


Fig. 1. Basic half bridge.

I. INTRODUCTION

THE BASIC half-bridge topology (Fig. 1) provides some implicit problems for designers who wish to create a high-linearity power converter. The power stage switches are normally operated in strict time alternation. The topology has an inherent fault path when both switches are enabled. Therefore, it is common practice [1] to add a third state to the switching sequence with all switches off (dead time) to reduce the probability of common-mode (shootthrough) currents. The insertion of the dead-time state creates an inherent nonlinearity (Fig. 2) in the conversion cycle for output currents near zero current as the converter does not remain in continuous current mode (CCM). The effects of a dead zone are additive to the distortion resulting from switch and freewheel diode losses [2].

When used as amplifiers, wide-bandwidth dc-to-ac power converters often require relatively high-switching frequencies to provide ample bandwidth for processing and filtering a full-band signal. For example, audio pulsewidth modulation (PWM) amplifiers can be designed to have adequate 20-kHz bandwidth and acceptably low-output impedance when switched at 500 kHz. The higher the operating frequency (shorter conversion cycle), the larger the proportion of the switching cycle that is lost by a given dead-time interval. This also increases the amount of nonlinearity created by the dead zone in the conduction cycle.

A number of partial solutions have been suggested for improving this problem [3], [4]. A better solution is to develop a topology that eliminates the shootthrough high d_I/d_t current path and allows the sum total switch duty cycle to be unity.

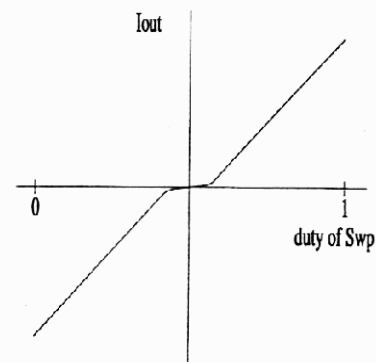


Fig. 2. I_{out} versus converter duty cycle reveals a dead zone caused by the dead time in the switch timing.

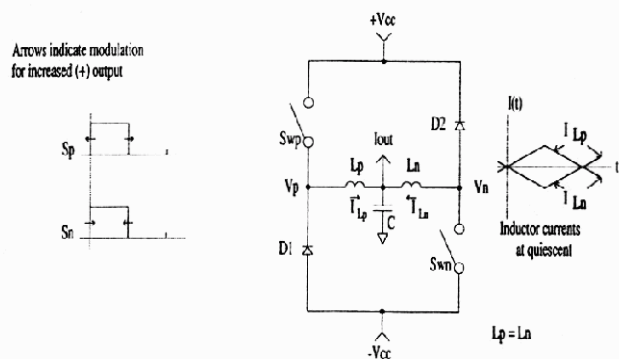


Fig. 3. The opposed current (OC) half bridge.

II. THE BASIC OPPOSED CURRENT CONVERTER

The solution is found in the topology of Fig. 3. Two simple buck converters are operated not in time alternation, but in time opposition. The shootthrough d_I/d_t is now limited by a large in-series inductance ($L_p + L_n$). The sum of the inductor currents is the signal current and has useful properties.

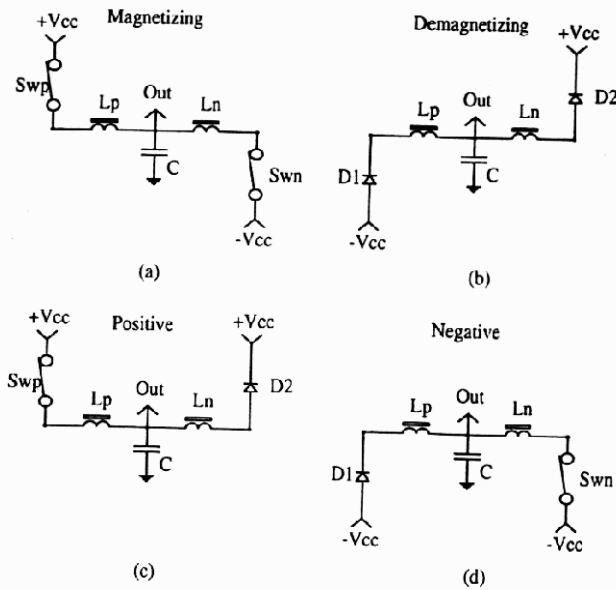


Fig. 4. CCM states of converter: (a) magnetizing, (b) demagnetizing, (c) positive, and (d) negative.

When the output voltage is set to zero, the two switches ideally are gated simultaneously with 50% duty. This results in no ripple current at the output, making filtering simpler. This ripple null is in addition to the traditional design's minimum ripple points at saturation duty cycles $[D(S_p), D(S_n)]$ of (0, 1) and (1, 0).

The four states of CCM operation are shown in Fig. 4. The magnetizing and demagnetizing states are the only states used for quiescent operation. The positive (negative) output state is inserted between the magnetizing and demagnetizing states should positive (negative) output be desired. The output inductive impedance of the power stage is constant at $L_p L_n / (L_p + L_n)$ for all CCM states. There are five additional discontinuous current mode (DCM) states which are not ideal states for linear operation. Four DCM states have only one switch or diode conducting, and the fifth DCM state has none of the branches conducting.

As the output is programmed to nonzero values of voltage, the duty of one switch is increased and the duty of the other is decreased in like manner (Fig. 5). The sum total switch duty is maintained at unity. When natural PWM and double-edged modulation are used, the result is that the output ripple frequency is doubled. Conceptually, the effective output derives from the two pulses that form as the difference between the S_p and S_n pulse widths. Therefore, it is only necessary to operate the switches at one half of the functional operating frequency required of a traditional half-bridge output stage. This is consistent with the observation that the traditional half-bridge output stage contains redundant modulation information by virtue of using complementary drive signals to its two switches.

The use of two independent PWM samplers can double the information extracted from the demand signal. Such a modulator is shown in Fig. 6. Note that it is easy to control the total duty (dead time) with a common to ground signal

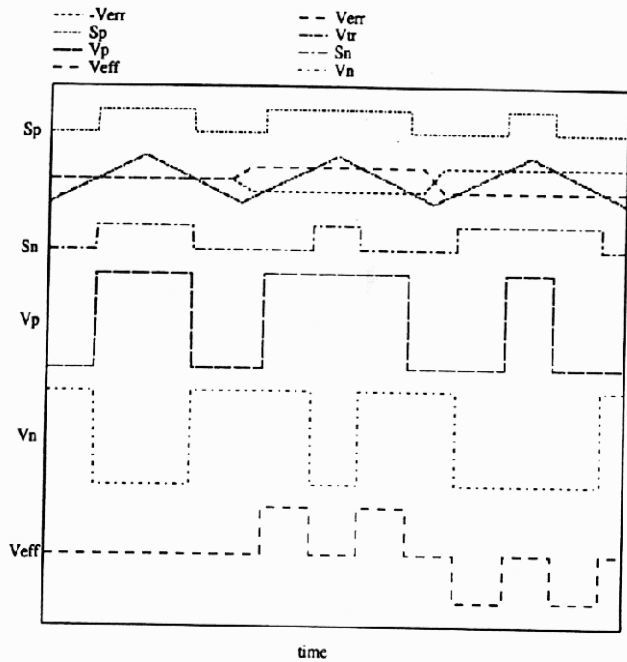


Fig. 5. Modulating the OC power stage. Three values of signal (V_{err}) are shown resulting in zero, positive, and negative output, respectively. The two-pulse difference between $S_p(V_p)$ and $S_n(V_n)$ results in output (V_{eff}).

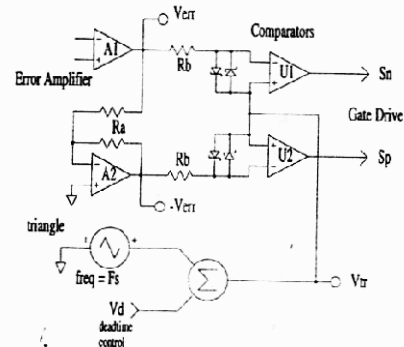


Fig. 6. Opposed current PWM modulator.

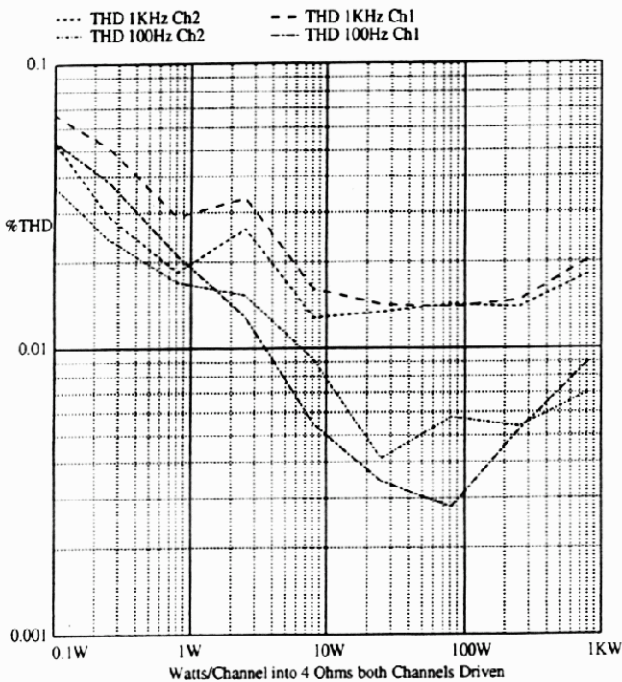
V_d . Losses in the output stage will require the total duty to be slightly above the ideal value of 100%.

When an opposed current power converter is used as a power amplifier, it is referred to as an opposed current amplifier or OCA.

III. IMPLEMENTATION—A 2.5-kW AMPLIFIER

Total harmonic distortion (THD) measurements are shown (Fig. 7) for a studio-quality two-rack-space two-channel audio amplifier which is switched at 250 kHz (500-kHz equivalent) and has an output power stage efficiency of 92%, high enough to not require forced air cooling.

The open-loop full-scale THD of the output stage is $\approx 0.2\%$ and well balanced, giving rise to odd-order harmonics. For less demanding audio applications, the power stage could be used open loop without additional feedback. A regulated supply would be appropriate for applications not using overall feedback. The present design (Fig. 9) uses both current and

Fig. 7. THD versus watts into 4 Ω .

voltage feedback with large amounts of low-frequency voltage feedback eliminating any distortion resulting from supply voltage fluctuations [2].

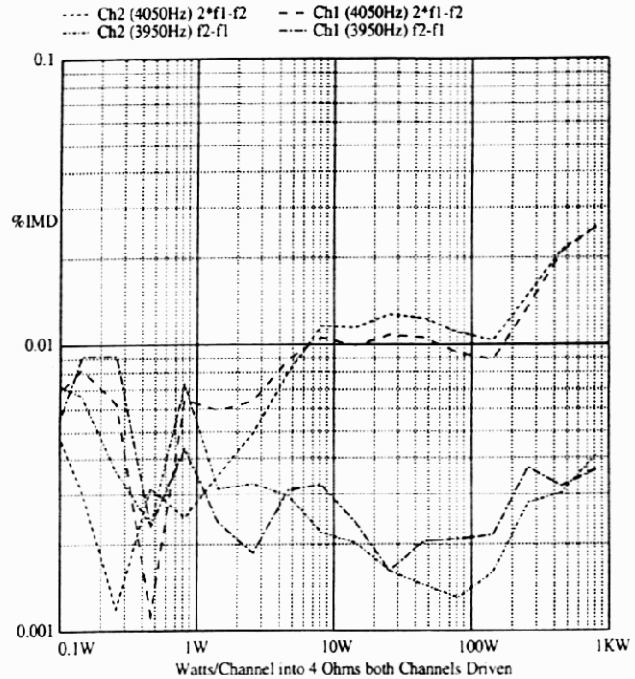
The open-loop linearity of the output stage is higher than traditional linear amplifier forms if comparison is made with all feedback removed inclusive of topologically derived feedback.

High-frequency linearity is best described with an in-band intermodulation (IM) distortion test such as total difference frequency distortion or TDFD [5]. Two, equal amplitude tones at 8 and 11.95 kHz are used as a signal, and the distortion products at f_2-f_1 (3950 Hz) and $2f_1-f_2$ (4050 Hz) are measured (Fig. 8). No careful tuning of the output distortion factors can simultaneously eliminate both of these products. It is noted that the simple difference tone at 3950 Hz is nearly null as the transfer function of the amplifier is symmetric (an odd function with vanishing even powers of the input). Any two-tone IM test which reports only the difference tone can be zero distortion even when the amplifier under test is significantly distorted.

While linear amplifiers are thermally affected adversely by the load reactance they drive (loudspeakers), the PWM design has no such issues. It is not unusual for overheating in linear designs to invoke protection mechanisms which may create large amounts of audible distortion. No such behavior occurs with cycle by cycle current limiting as is common to PWM controllers. This product is far less distorted under all extremes of operation as compared with its linear predecessors.

IV. EXTENSION TO N -PHASE INTERLEAVE (OCIA)

The basic opposed current output stage being interleaved by nature can be extended to more stages increasing the ripple frequencies and further reducing net output ripple current amplitudes. Such an amplifier has been dubbed an opposed

Fig. 8. Eight- and 11.95-kHz TDFD versus watts into 4 Ω .

current interleaved amplifier or OCIA. Because the basic power stage provides an interleave factor [6] N of two, all derivative designs will have an even interleave number.

The optimum format when used as a full bridge operates the second half bridge from a quadrature clock, thereby increasing the interleave factor N to four. The above-mentioned audio amplifier operates its second channel from such a clock and produces a bridged output mode ripple frequency of 1 MHz, yet all switches are operating at 250 kHz. Such are the implicit benefits of interleaving as a design philosophy. Zero net ripple occurs when duty cycles are (0, 1), (0.25, 0.75), (0.5, 0.5), (0.75, 0.25), or (1, 0).

If a bridged design was also paralleled, its interleave factor N would be 8, 12, 16, ..., i.e., four times whatever degree of paralleling was performed. Phasing of the modulation waveforms would evenly divide the unit circle into $360/N^\circ$ intervals, i.e., the modulation waveforms will be evenly spaced over the switching interval. This progression is shown in Fig. 10. Note that the inverted versions of the modulating triangle waveforms are not shown as the modulator (Fig. 6) does not require such.

Increasing N constructs an output current waveform that progressively converges to the intended output current without requiring extensive filtering by other means. There will be $N+1$ ripple nulls evenly spaced along the duty-cycle continuum. The resultant output spectrum is that of a PWM amplifier operating at N times the switch frequency and having reduced output ripple (see Figs. 13 and 14 and Appendixes A and B).

Figs. 11–14 (simulations) show both time and frequency domain displays of PWM output signals for the case of one cycle of 5-kHz cosine modulation (modulation index $M = 1.0$) and with a switching frequency of 100 kHz on all switches. Supply voltages are shown as $\pm 100 V_{dc}$. The output is taken as the open circuit voltage that forms at the common

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