Development of a spice op-amp macro-model for current-feedback amplifiers (Part 1 of 2)

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Current-feedback amplifiers (CFAs) are the high-speed relatives of more common voltage-feedback amplifiers (VFAs). CFAs have wider bandwidths and faster slew rates. Applications like DSL rely on their fast and strong output drives.

Models are important because they allow engineers to test designs before they go through the time-intensive and costly process of building a working prototype. In this article, we introduce you to a circuit model for a current-feedback amplifier. Since it would take far too long to simulate every nuance of a complete design, this macromodel simulates the most common effects such as transient response, frequency response, voltage noise and output slew rate limiting. Detailed descriptions of each stage in the model will be presented with examples of model performance and correlation to actual device behavior.

Figure 1 shows the conceptual approach of the current-feedback amplifier. CFAs have a unity gain buffer to force the inverting input (V_{in-}) to follow the non-inverting input (V_{in+}). This topology is very different from the high impedance inputs of the voltage-feedback amplifier. In the CFA case, the inverting input node shows the low input impedance (Z_{in-}) from the output of the buffer. The error signal is the current (I) flowing into or out of the non-inverting node. The error current is converted by a large transimpedance, Z, to the output voltage. R_f is used to control the feedback current.

This is another major deviation from the voltage-feedback topology. In VFAs, the feedback network (R_f and R_g) primarily set the voltage gain. In CFAs, the feedback network does set the gain, but the value of R_f also affects the bandwidth of the amplifier.

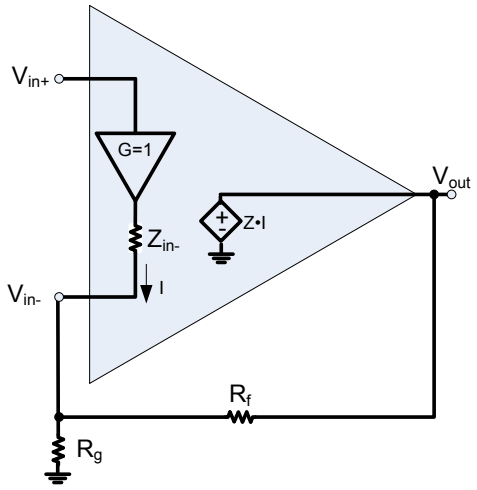

Figure 1: The Block Diagram of a Current-feedback amplifier

A five-stage model represents the actual circuit and the block diagram is shown in **Figure 2**. These five basic blocks are the input stage, the gain stage, the frequency-shaping stage, the output stage and the noise module.

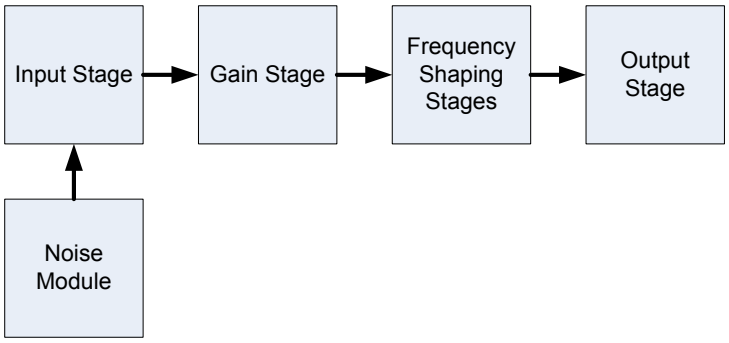

Figure 2: The block diagram of a CFA Macromodel

The Input Stage

As stated, the biggest difference between a CFA and a VFA is the input stage. **Figure 3** shows an example, the input stage of a CFA model. Four identical bipolar transistors are included, Q1 to Q4. The effective output of this stage is at nodes 11 and 12 which are coupled into the gain stage by using voltage controlled current source. The bias current I1/I2 of Q1/Q2 should be set by:

$$I_1 = I_2 = \frac{kT}{2q \bullet Z_{in-}} \text{ i.e. } Z_{in-} = \frac{1}{2\,g_m} \qquad (1)$$

The impedance at the inverting input, Z_{in-}, can be measured. In this example, I1=I2=85 μA. R1, R2, C1, C2 are used to fit the frequency response and to control the input stage slew rate.

There are many other components used in the input block. C_{s1} and C_{s2} are the inverting input capacitance. C_{in1} is the non-inverting input capacitance. The input bias current is modeled by current sources I_{b1} and I_{b2}. The input offset voltage is modeled by the voltage source V_{os}. The current source G_{b1} is used to model the input current common mode rejection at the inverting input.

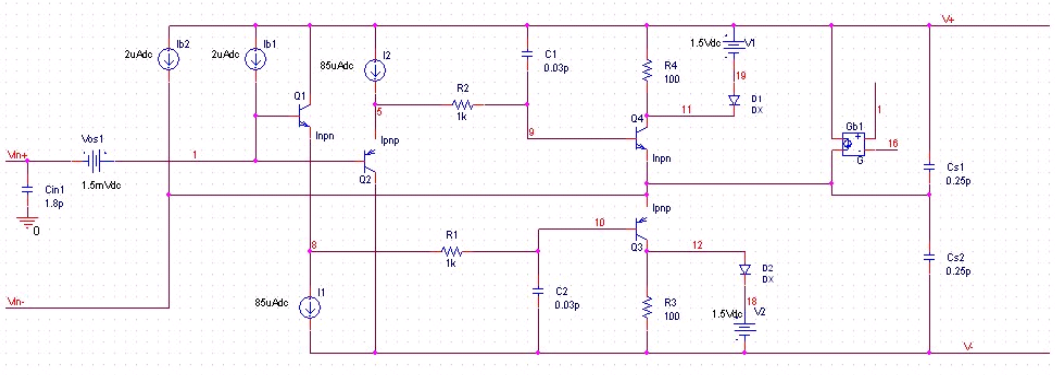

Figure 3: Input Stage of a CFA (EL5165)

The Gain Stage

This stage is similar to the gain stage of a VFA. It performs many important functions.

1) This stage sets the open loop trans-impedance of the part.
2) It provides output slew rate limiting.
3) It contributes the dominant pole to the AC characteristic.
4) It level shifts the signal from two voltages referred to the supplies to a single voltage referred to the mid-point.
5) It limits the output.

Taking a closer look at the components of the gain stage in **Figure 4**, slew rate limiting is set by limiting the current to C3 and C4 in Figure 4. The current limiting is set in the input stage by clamping the voltage across R3 and R4 shown in Figure 3. This voltage is decided by voltage sources V1 and V2 and diodes D1 and D2. R7/C3 and R8/C4 decide the dominant pole of this model. D3/D4 and V5/V6 are used to control the output clamping voltage.

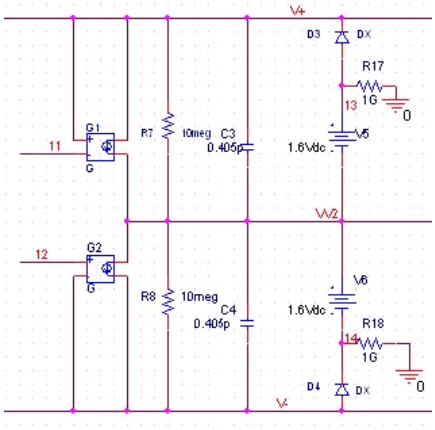

Figure 4: Gain Stage

Frequency-Shaping Stages

The frequency-shaping stages of a CFA model are very similar to that of a VFA. Each frequency-shaping block provides unity gain, so it is easy to add more poles and zeros. For more information of the frequency-shaping stages, see **Reference 2**. For our example op amp, only three pole stages are used which is shown in **Figure 5**. E3 is used to set the reference level at the middle of the supplies, V+ and V-.

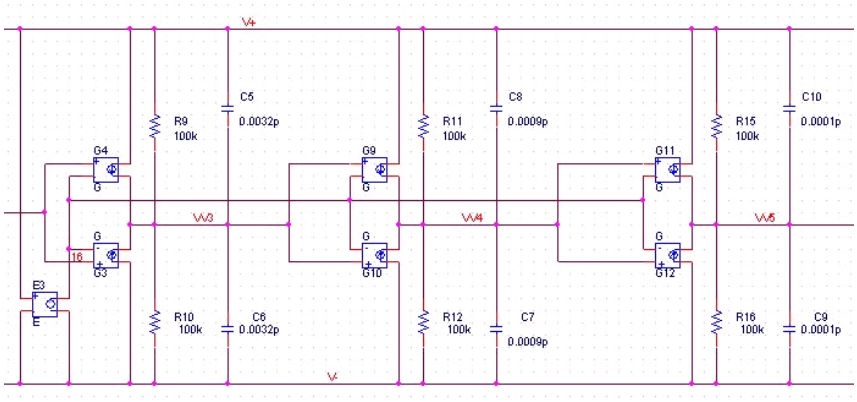

Figure 5: Higher-Order Pole Stages

Noise Module

The input current noise of the current feedback can't be neglected. It is measured in $pA/\sqrt{Hz}$. Voltage noise can be larger, so both a voltage noise module and a current noise module are needed for our CFA model.

For the right noise analysis, one trick called "noiseless resistors" has to be used at the input stage. All the resistors in the input stage should be substituted by voltage controlled current sources (Device G in SPICE) where input and output terminals are connected together and the g_m is set to the reciprocal of the required resistance.

We will use two pieces to construct the total noise model. The noise module of **Figure 6** generates 1/f and white noise by using a 1.5V voltage source biasing a diode-resistor series combination. White noise is generated by the thermal noise-current generated in the material of the resistors.

$i_n^2 = \dfrac{4\ kT}{R}$ (k is the Boltzmann's constant)

So the required value of the resistor for a given noise-voltage spectral density is

$R = \dfrac{e_n^2}{2 \times 4\ kT}$ (e_n is the spectral density of the white noise voltage)

Flicker noise, also called 1/f noise, refers to the noise exhibiting power spectral density inversely proportional to the frequency. More generally, this noise has a spectral density of $S_N \propto \dfrac{1}{|f|^{\beta}}$ ($\beta > 0$). As a data point, the frequency where the flicker noise curve crosses the white noise curve is defined as the corner frequency. The small amount of flicker noise that remains is modeled within the SPICE diode model. Referring to Figure 6,

$$i_n^2 = 2qI_d + KF \bullet \frac{I_d^{AF}}{frequency}$$

where I_d is the DC diode current. AF and KF are the model parameters of the SPICE diode and q is the charge of the electron. The flicker noise exponent (AF) is set to 1 and the flicker noise coefficient (KF) is set $KF = \frac{E_a^2}{2R^2 \bullet I_d}$ where E_a is the noise-voltage spectral density at 1 Hz. The simulated voltage noise will show the 1/f noise-voltage spectral density with the correct corner frequency.

The noise module in **Figure 7** only simulates the white portion of the current noise by utilizing thermal noise of two parallel resistors.

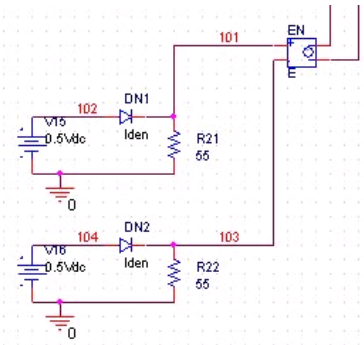

Figure 6: Noise Voltage Module

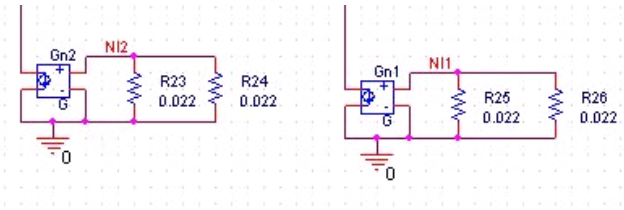

Figure 7: Noise Current Module

Output Stage

After the frequency shaping-stages, the signal appears at Node VV5 which is referenced to the midpoint of the two supply rails, **Figure 8**. Each controlled source can generate enough current to support the desired voltage drop across its parallel resistor. R13 and R14 are equal to twice the open loop output resistance, so their parallel combination gives the correct Z_{out}. D5-D8 and G9-10 are used to force a current from the positive rail to the negative rail to correct the real current sink or source. G11-12 drive the output.

$$G9 = G10 = G11 = G12 = \frac{1}{2Z_{out}}$$

$$R13 = R14 = 2Z_{out}$$

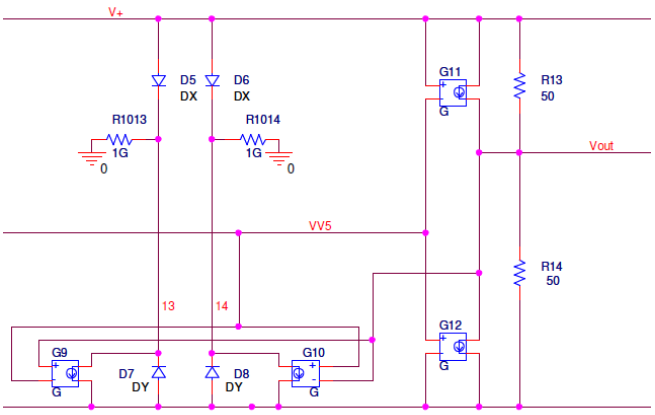

Figure 8: Output Stage

(***Part 2*** will discuss the simulation results and includes a net list)

References

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2. Mark Alexander, Derek Bowers, "AN-138 SPICE-Compatible Op Amp Macro-Models", Analog Devices Inc., Application Note 138.
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4. "Current-feedback amplifier Theory and Applications", Intersil Corp., Application Note 9420.

About the authors

Jian Wang was born in China in 1975 and has served as an applications engineer with Intersil since 2005, focusing on high speed amplifiers and drivers. He received a Ph.D. from the University of California at Davis in 2006.

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