Analogue filter calculations for my solid-state DAC

Version 2, Marcel van de Gevel, August 2021

1. Choice of pole locations

I've chosen a Gaussian-to-6 dB low-pass filter at about 500 krad/s with one extra negative real pole added to it. This has a very good phase response over its passband while falling off much steeper above its passband than the 0.05° linear phase filter I used for my valve DAC, which reduces the amount of ultrasonic noise that comes through. The extra negative real pole can be implemented as a passive RC section to get some suppression of high-frequency spikes before reaching the first op-amp, in order to prevent slewing induced distortion. Its position has been tweaked to further improve the phase response and to get about the same in-band roll-off as the 0.05° linear phase filter I used for my valve DAC, so the digital roll-off compensation works for both.

The target pole locations were:

-1.25 Mrad/s and (-271665 +/- 171562.5 j) rad/s for the first filter stage
(-233613.5 +/- 499550 j) rad/s for the second filter stage
(-110183.5 +/- 753361.5 j) rad/s for the third filter stage

2. Compensating for the effect of finite op-amp gain bandwidth product in an integrator

The circuit of the upper part of figure 1 is a simple op-amp integrator. Assuming that the op-amp is ideal (has nullor properties), its negative input is at ground potential. When the input voltage is V_{in}, a current V_{in}/R flows through the resistor, a voltage $V_{in}/(sRC)$ drops across the capacitor and the output voltage becomes $-V_{in}/(sRC)$, assuming that the resistor and capacitor are also ideal. So far, so good. Conversely, the input voltage is $-sRC\ V_{out}$.

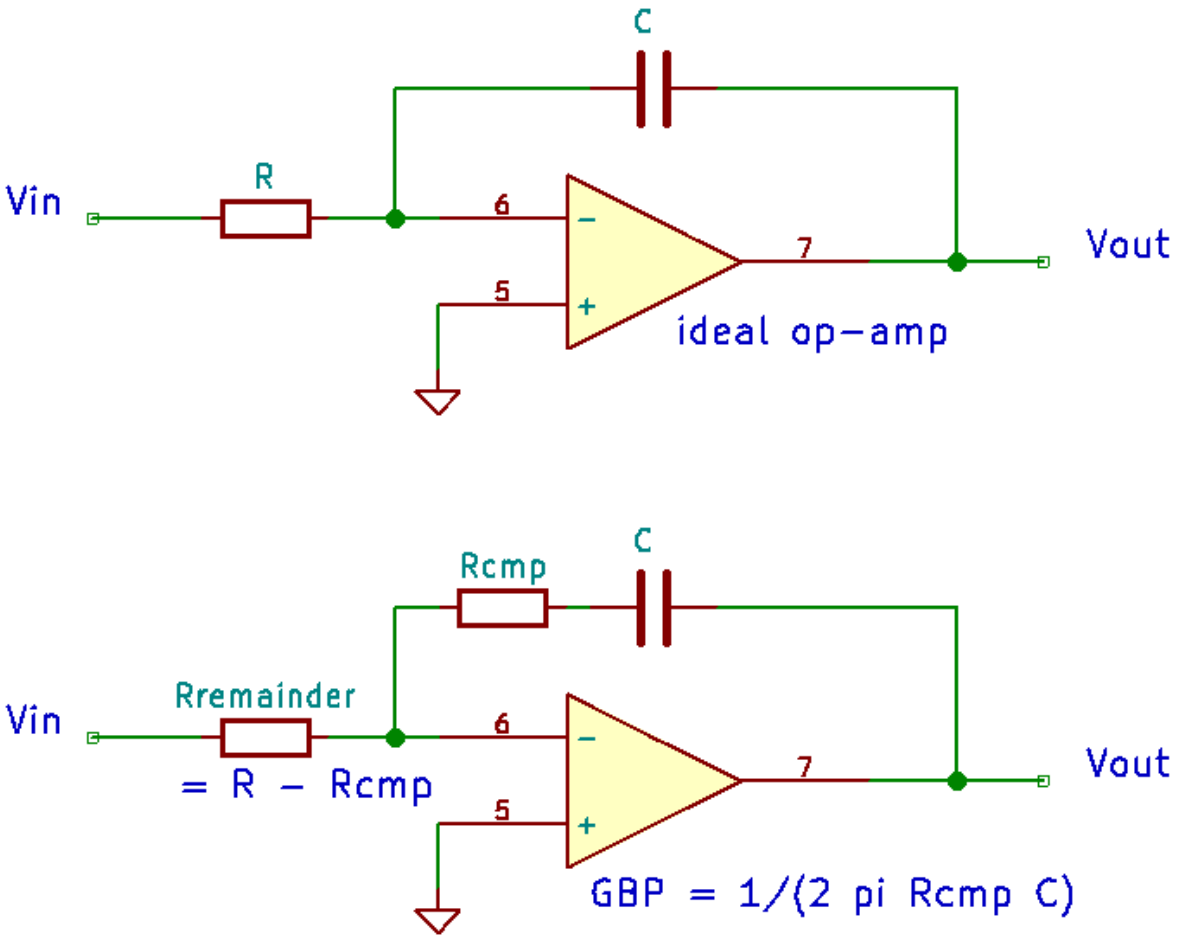

Figure 1: Integrator with an ideal and a non-ideal op-amp

When good resistors and capacitors are used, the main non-ideality in a practical implementation of the circuit is usually the finite gain-bandwidth product of a practical op-amp. With its positive input grounded, an op-amp with open-loop gain $2\pi f_{GBP}/s$ requires an input voltage of $-(s/2\pi f_{GBP})\ V_{out}$ at its negative input to produce an output voltage V_{out}.

Imagine R in the circuit with an ideal op-amp is replaced with a potmeter with the wiper open. Depending on the position of the wiper, the voltage on it can then be anything between $-sRC\ V_{out}$ (wiper turned to the input) and 0 (wiper turned to the virtual ground). As long as $RC \geq 1/2\pi f_{GBP}$, there is a wiper position where the voltage is the $-(s/2\pi f_{GBP})\ V_{out}$ that a non-ideal op-amp would need.

Hence, using an op-amp with finite gain-bandwidth product, the effect of the finite gain-bandwidth product can be compensated for by connecting the inverting input to a tap on the input resistor. Practically, this means that resistor R is split into a part $R_{cmp} = 1/(2\pi f_{GBP}C)$ and $R_{remainder} = R - R_{cmp}$. Resistor R_{cmp} is connected straight in series with the integration capacitor C and the resistor to the negative input is reduced to $R_{remainder}$. This is shown in the bottom circuit of figure 1.

For simplicity, in the rest of this document, the op-amps will be assumed ideal. Most of the circuits can be corrected for finite gain-bandwidth product using the method explained in this section.

3. Replacing integrators with ideal inductors to simplify calculations

Figure 2 shows a subcircuit that's often found in multiple feedback (MFB) filters. When you apply a voltage step from 0 to V at the input, a current $V/R_a + V/R_b$ will immediately start flowing into the input. As the integrator output voltage builds up, the input current increases. All in all, the input impedance is equal to the parallel connection of R_a, R_b and an inductance $L = R_a R_b C_a$, as can be verified by straightforward network analysis.

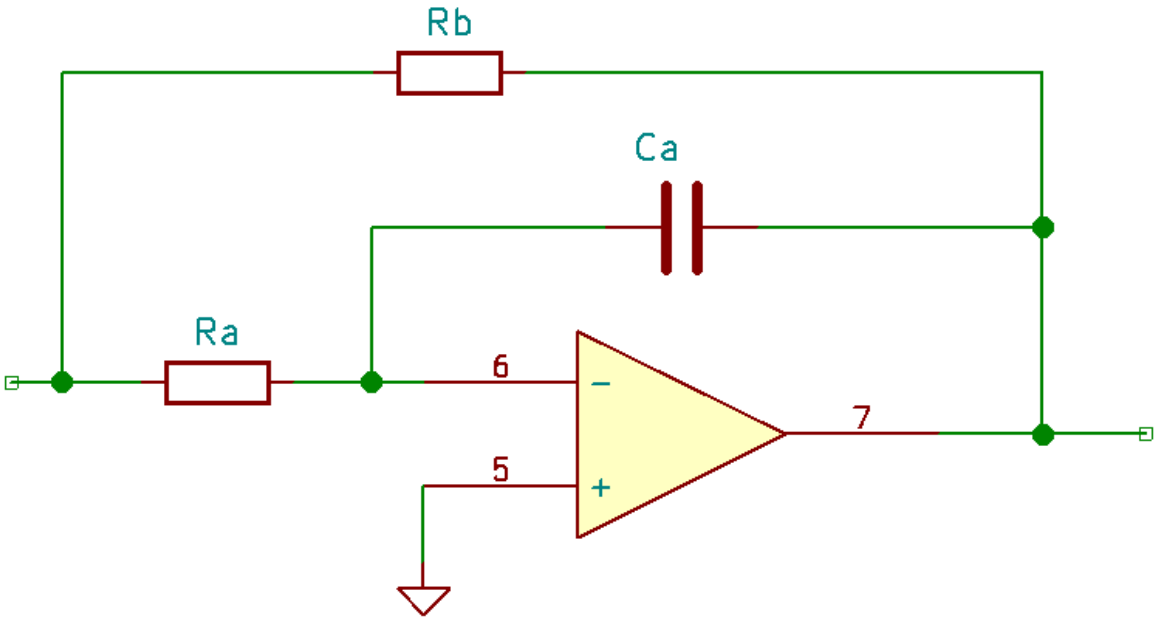

Figure 2: Subcircuit often found in MFB filters

When the desired parallel resistance R_{par} and inductance L are given and C_a is chosen, the required resistor values are

$$R_a = \frac{\frac{L}{C_a R_{par}} \pm \sqrt{\frac{L^2}{C_a^2 R_{par}^2} - 4\frac{L}{C_a}}}{2}$$

$$R_b = \frac{L}{R_a C_a}$$

There are two solutions because swapping the resistors results in the very same impedance.

4. Second-order MFB sections

Adding a resistor R_c and a capacitor C_b to the circuit of section 3 results in a second-order MFB low-pass stage, which is equivalent to an LRC parallel network with $L = R_a R_b C_a$, with $R = R_a // R_b // R_c$ where // stands for in parallel with, and with $C = C_b$. Hence,

$$\omega_0^2 = \frac{1}{R_a R_b C_a C_b}$$

$$Q = \frac{\omega_0 C_b}{1/R_a + 1/R_b + 1/R_c}$$

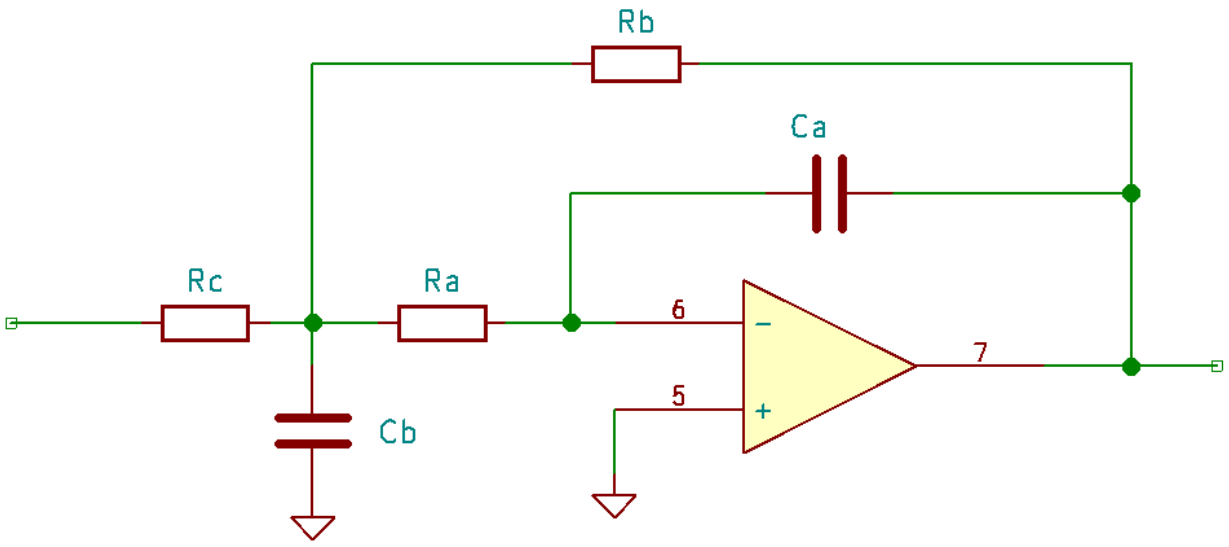

Figure 3: Second-order MFB stage

As capacitors come in fewer standard values than resistors and as the DC gain is $-R_b/R_c$, it is handy to choose the capacitances, the pole positions and the ratio R_b/R_c and to calculate the rest. In the remainder of this section, we will define $A = R_b/R_c$.

Assuming the target poles are a complex conjugate pair, one can calculate $\omega_0^2 = (\mathrm{Re}(p))^2 + (\mathrm{Im}(p))^2$ and $Q = -\omega_0/(2\,\mathrm{Re}(p))$. Given this, $A = R_b/R_c$ and chosen values for C_a and C_b, one can derive that

$$R_b = \frac{\frac{1}{Q} \pm \sqrt{\frac{1}{Q^2} - 4\frac{C_a}{C_b}(1+A)}}{2\,\omega_0 C_a}$$

$$R_c = \frac{R_b}{A}$$

$$R_a = \frac{1}{\omega_0^2 C_a C_b R_b}$$

When complex or negative values are found, the choice of C_a and C_b was not suitable. I haven't checked this for this type of filter, but usually the Q factor becomes most accurate when capacitance ratios are used that only just make the expression under the square root positive, that is the largest ratio that still meets

$$\frac{C_a}{C_b} \le \frac{1}{4Q^2(1+A)}$$

5. Third-order MFB section

The first filter stage of the DAC is a third-order MFB section. It has some purely passive filtering before reaching the first op-amp, which helps to prevent slewing-induced distortion. It also

complicates the mathematics.

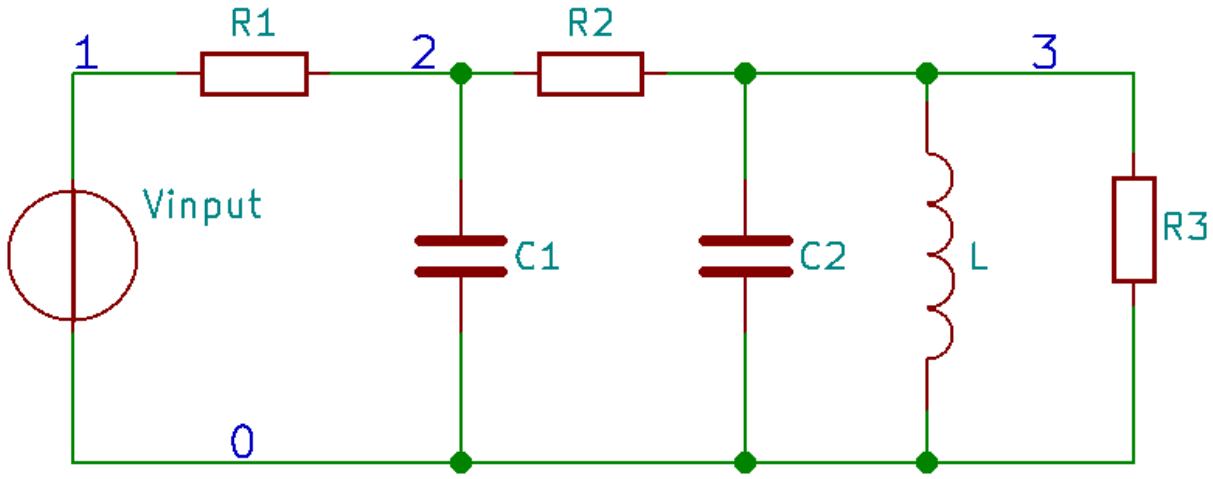

Figure 4: LRC equivalent of a third-order MFB stage

Figure 4 shows the RLC equivalent of this stage. I've calculated the transfer from the voltage source to V_3 (voltage at node 3) by replacing the voltage source and R_1 by their Norton equivalent to reduce the number of nodes by one and then applying modified nodal analysis. The result is:

$$\frac{V_3}{V_{input}} = \frac{sL/(R_1+R_2)}{s^3 L\frac{R_1R_2}{R_1+R_2}C_1C_2 + s^2 L\left(\frac{R_1R_2}{R_1+R_2}\left(\frac{1}{R_2}+\frac{1}{R_3}\right)C_1 + C_2\right) + s\left(\frac{R_1R_2}{R_1+R_2}C_1 + L\frac{R_1+R_2+R_3}{(R_1+R_2)R_3}\right) + 1}$$

Of course the voltage at node 3 is not the output voltage of the entire MFB stage, but as a system has only one characteristic polynomial, the denominator and the pole positions must be the same.

In order to get the poles at the intended locations without having to solve third-order equations, you can calculate the desired coefficients of the denominator polynomial and equate them to the expression that was just found. That is, suppose the desired poles are p_1, p_2 and p_3. The desired denominator polynomial is then

$$\left(s\frac{-1}{p_1}+1\right)\left(s\frac{-1}{p_2}+1\right)\left(s\frac{-1}{p_3}+1\right) = s^3\frac{-1}{p_1p_2p_3} + s^2\left(\frac{1}{p_1p_2}+\frac{1}{p_2p_3}+\frac{1}{p_1p_3}\right) + s\left(\frac{-1}{p_1}+\frac{-1}{p_2}+\frac{-1}{p_3}\right) + 1$$

To make the equations simpler, let's introduce

$$\alpha_3 = \frac{-1}{p_1p_2p_3}$$

$$\alpha_2 = \frac{1}{p_1p_2}+\frac{1}{p_2p_3}+\frac{1}{p_1p_3}$$

$$\alpha_1 = \frac{-1}{p_1}+\frac{-1}{p_2}+\frac{-1}{p_3}$$

so the desired denominator polynomial becomes

$$\alpha_3 s^3 + \alpha_2 s^2 + \alpha_1 s + 1$$

When you choose C_1, C_2 and $R_1 R_2/(R_1 + R_2)$, which will be called R_{1p2} from now on, rearranging lots of terms gives:

$$L=\frac{\alpha_3}{R_{1p2}C_1C_2}$$

$$R_2=\sqrt{\frac{R_{1p2}}{\frac{1}{L}(R_{1p2}C_1-\alpha_1)+(\frac{\alpha_2}{L}-C_2)\frac{1}{R_{1p2}C_1}}}$$

$$R_1=\frac{1}{\frac{1}{R_{1p2}}-\frac{1}{R_2}}$$

$$R_3=\frac{1}{\frac{-1}{R_1+R_2}+\frac{\alpha_1-R_{1p2}C_1}{L}}$$

As usual, the trick is to choose C_1, C_2 and $R_{1p2} = R_1 R_2/(R_1 + R_2)$ such that you get positive real outcomes.

6. Reduced DC blocking capacitor output stage

The output stage features a DC blocking capacitor that's inside a feedback loop to get away with a relatively small value, at the expense of subsonic peaking at the op-amp output. It has a second-order high-pass response. The schematic is shown in figure 5. R_2 represents the parallel connection of a resistor that keeps the output biased at 0 V and the load.

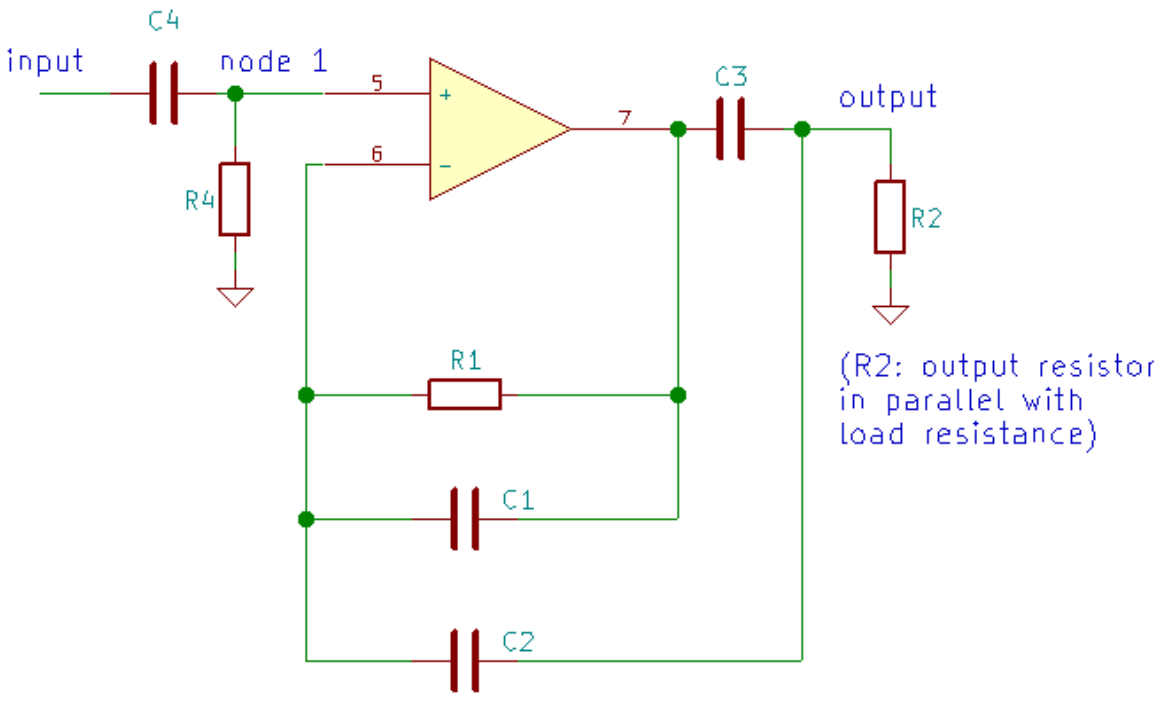

Figure 5: Output stage

Skipping R_4 and C_4 for the time being and using modified nodal analysis to calculate the transfer from node 1 to the output results in

$$\frac{V_{out}}{V_1}=\frac{sR_2(C_2+C_3)\left(sR_1\frac{C_1C_3+C_2C_3+C_1C_2}{C_2+C_3}+1\right)}{s^2(C_1C_3+C_2C_3+C_1C_2)R_1R_2+s(R_1C_1+R_2C_3+R_2C_2)+1}$$

The numerator shows that there is one zero in the origin and one negative real zero, while a normal second-order high-pass has two zeros in the origin. This can be corrected for with R_4 and C_4 by choosing

$$R_4C_4=R_1\frac{C_1C_3+C_2C_3+C_1C_2}{C_2+C_3}$$

As R_2 is not in the equation, this correction will work for any load resistance.

The denominator of the transfer shows that there are two poles with

$$\omega_0=\frac{1}{\sqrt{R_1R_2(C_1C_3+C_2C_3+C_1C_2)}}$$

$$Q=\frac{1}{\omega_0(R_1C_1+R_2C_3+R_2C_2)}=\frac{\sqrt{R_1R_2(C_1C_3+C_2C_3+C_1C_2)}}{R_1C_1+R_2(C_2+C_3)}$$

When $R_2=\frac{R_1C_1}{C_2+C_3}$, both the numerator and the denominator of Q have a sensitivity of ½ to R_2. That is, there is an optimum in Q as a function of R_2 for this value of R_2. This optimum is actually a maximum.

Filling in $R_2=\frac{R_1C_1}{C_2+C_3}$ in the expression for Q and rearranging terms,

$$Q_{max}=\frac{1}{2}\sqrt{\frac{C_1C_3+C_2C_3+C_1C_2}{C_1C_2+C_1C_3}}=\frac{1}{2}\sqrt{\frac{C_1+\frac{C_2C_3}{C_2+C_3}}{C_1}}$$

If you want to prevent subsonic peaking across the load for any load resistance, Q_{max} has to be smaller than or equal to ½√2, as an optimally flat second-order high-pass has a Q of precisely ½√2.

This is met when $\frac{C_2C_3}{C_2+C_3}\le C_1$, so the capacitance of the series connection of C_2 and C_3 has to be smaller than or equal to C_1 to prevent peaking across the load for any load resistance (preferably equal, if you want the response to be as flat as possible under this constraint).

If you don't mind a small amount of subsonic peaking at some load resistances, Q_{max} can be made a bit larger, for example 1. This is met when $\frac{C_2C_3}{C_2+C_3}=3C_1$, so the capacitance of the series connection of C_2 and C_3 can then be up to three times C_1. I've used a ratio of two in my DAC, so it is somewhere in between with a maximum Q of ½√3.