Slewing and DAC current-to-voltage converters

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Figure 1 shows a simplified schematic of a DAC with a current output and a straightforward op-amp-based current-to-voltage converter. The part in the dashed blue line is the op-amp; it is assumed to be a classical three-stage op-amp, but most of what I'm about to write applies to other op-amp topologies as well, except so-called current feedback op-amps. (I don't like this use of the term current feedback, but that's a different matter.)

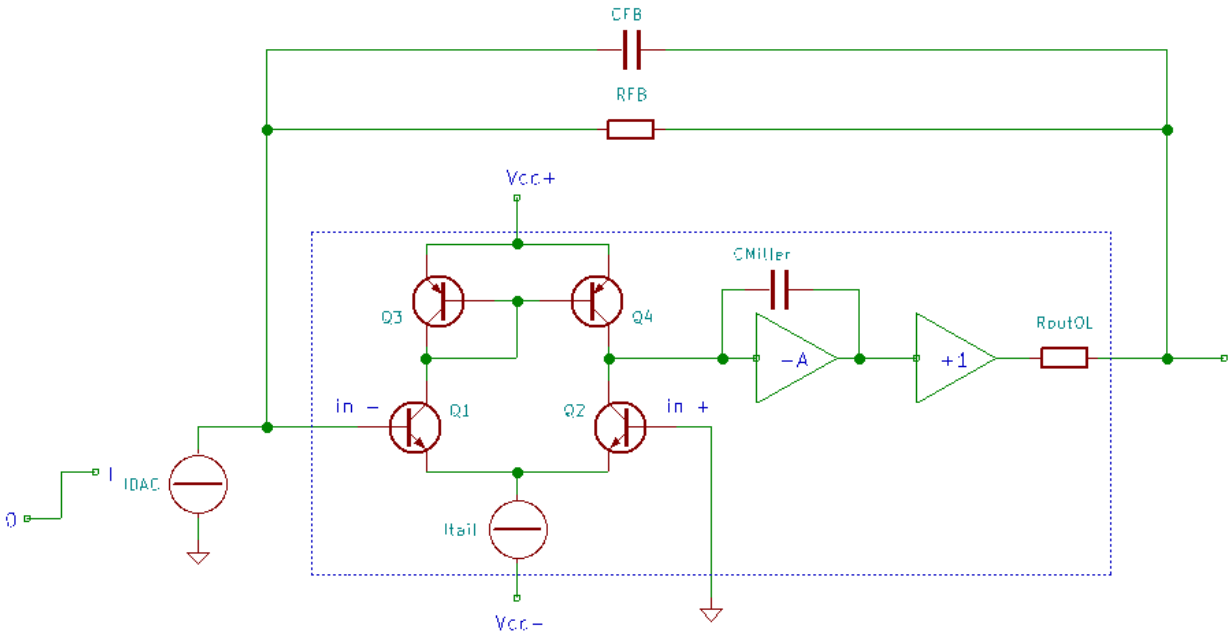

Figure 1: DAC with op-amp current-to-voltage converter. The current source I_{DAC} represents the output current of the DAC, the part in the dashed blue line represents a typical op-amp and C_{FB} and R_{FB} represent its feedback network. R_{outOL} is not a real physical resistor, but a model for the fact that the internal voltage follower that drives the op-amp's output is imperfect and has a nonzero output impedance (which is the op-amp's open-loop output impedance).

The current coming out of the DAC makes a step in each sample period, but for simplicity, we will just consider one step from 0 to I at $t = 0$. Also for simplicity, the DC bias current drawn by the base of Q_1 will be neglected, as will any offsets. The second stage of the op-amp has a DC gain of $-A$ which will be assumed to be $-\infty$.

Before the step occurs, capacitors C_{Miller} and C_{FB} are empty. The voltage across a capacitor can not change instantly, so immediately after the step, capacitors C_{Miller} and C_{FB} are still empty. The current from the DAC will then be divided between the base of Q_1 and the op-amp's open-loop output impedance R_{outOL}. In practice, most of the current will flow through the op-amp's open-loop output impedance R_{outOL}, because it has a lower impedance than the base of Q_1. Hence, the op-amp's output voltage will initially make a step from 0 to $I\,R_{outOL}$. The same voltage step will occur at the base of Q_1, that is, at the op-amp's input, since feedback capacitor C_{FB} is still empty.

Due to the voltage step at the base of Q_1, the collector current of Q_1 will become greater than the collector current of Q_2 (assuming a positive initial voltage step, so $I > 0$). The collector current of Q_1 gets mirrored by the current mirror Q_3 - Q_4 and the difference between the currents through Q_4 and Q_2 will flow into the second stage, mostly into its compensation capacitor C_{Miller}. The voltage across

C_{Miller} will gradually increase and the voltage at the op-amp's output will gradually decrease and become whatever is needed to get the voltage at the base of Q_1 quite close to 0 again. That is, the feedback loop gradually kicks in.

If the initial voltage step is large enough to drive the differential pair into clipping, the voltage coming out of the second stage and the voltage coming out of the op-amp will change with a rate of $-I_{tail}/C_{Miller}$. The absolute value of this rate of change is called the op-amp's slew rate. As the op-amp causes gross distortion when working in this regime, it is very desirable to avoid slew rate limiting.

When the voltage step is much too small to cause clipping of the first stage, the current initially coming out of the first stage is the size of the step times the transconductance of the first stage, which I will call g_{m1}. The absolute value of the initial rate of change is then g_{m1}/C_{Miller} times the size of the step.

The distortion of the op-amp's first stage increases gradually as the slew rate limiting region is approached, so one would like to stay well below slew rate limiting. Hence, one has to fulfill

$$I\,R_{outOL}\frac{g_{m1}}{C_{Miller}} \ll \frac{I_{tail}}{C_{Miller}}$$

Assuming an infinite second-stage gain A, as has been assumed throughout this document, the magnitude of the small-signal open-loop gain of the op-amp at a frequency f is the transconductance of the first stage times the impedance of C_{Miller}. Hence,

$$A_{OL}(f) = g_{m1}\frac{1}{2\pi f\,C_{Miller}} = \frac{1}{f}\frac{g_{m1}}{2\pi C_{Miller}} = \frac{f_{GBP}}{f}$$

where f_{GBP} is the gain-bandwidth product, which, in this case, is the same as the unity-gain frequency.

Hence, the earlier criterion to avoid getting close to slew-rate limiting can be rewritten as

$$\frac{SR}{f_{GBP}} \gg 2\pi\,I\,R_{outOL}$$

where the slew rate limit has been called SR.

For a plain old bipolar differential pair input stage without local feedback, working at a given temperature in the region where bipolar transistors work well, the ratio of transconductance to tail current is fixed by laws of physics. With the basic topology of figure 1, the only ways available to increase SR/f_{BGP} are to use an op-amp with local feedback in the input stage (which are rare), or with another linearization technique such as a so-called multitanh input stage (also rare, although Analog Devices apparently has some) or to use an op-amp with FETs in the input stage (which are quite common).

Another solution to the problem is to apply some form of passive filtering between the DAC and the op-amp. This has its own issues; in particular, the trick is not to increase the input impedance too much, because the DAC output voltage has to stay close enough to zero. But that's a different subject altogether.