

3.4 ELECTRICAL INTERFACE

3.4.1 LPRO rf Output

3.4.1.1 Conversion of 10 MHz sine to 10 MHz TTL.

The LPRO was designed for a 10 MHz sine output with a 50 ohm source impedance at 10 MHz and for a 50 ohm load. The sine output permits built-in ESD and EMI protection even for the rf output signal, (the filter plate capacitance for the rf output signal is built into the matching circuit). The connector scheme is designed for direct plug-in of the LPRO J1 filter plate connector into the customer's circuit board connector, saving the cost of a cable harness.

Transmitting rf output signals over long distances is less of an EMI issue for the user when the signal is a sine wave instead of a square wave because a sine wave lacks harmonics. In addition, the power consumption of the sine wave driver into 50 ohms is lower than for a square wave driver into 50 ohms, especially when providing short circuit protection.

Because some users require a square wave for their application, this section identifies a number of potential methods for the conversion. Keep in mind that any circuitry shown must be verified by the user in their particular application. And no endorsement of any specific manufacturer's product is intended.

Refer to Table 3-1 for a comparison of the phase noise resulting for each of the circuits based on a test sample of one. Note that with the low noise source used there was no degradation in phase noise performance seen for the circuits illustrated in Figure 3-2 and only mild degradation for the circuit in Figure 3-3.

3.4.1.1.1 ac-coupled, CMOS gate

Two topologies are shown in Figures 3-2 and 3-3. The topology of Figure 3-3 has significantly less supply voltage sensitivity than that of Figure 3-2, but dissipates high power if the rf signal is removed (if implemented, the user should be aware of potential reliability issues for this mode of operation).

The best logic family found for low phase noise is AC or ACT logic. However, the faster logic families such as AC and ACT logic have more EMI issues via the power and ground lines because they charge and discharge internal and external capacitances faster and because of the lower drive impedances (higher emissions from the faster waveform edges). If EMI emissions are an issue, a slower logic family may be in order. The use of a small series resistor from the output of the gate to the load can reduce emission problems. Good local power bypassing is recommended for this application, such as a small series resistor and a low ESR tantalum supply bypass capacitor.

3.4.1.1.2 ECL-TTL Level Shifter

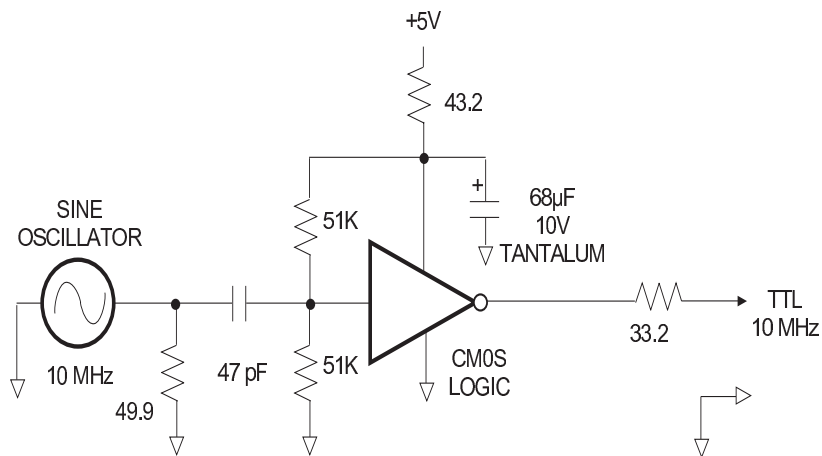
Figure 3-4 shows a sine to TTL converter using a positive ECL to TTL converter microcircuit. The advantage to this approach is the lack of supply and ground noise. Disadvantages are higher phase noise and cost (compared to the ac-couple, CMOS approach), and the extra power dissipation (roughly 18-23 milliamperes more at 5V).

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Table 3-1. Measured Phase Noise, Sine-to TTL Circuits

Figure	1 Hz -dBc/Hz	10 Hz -dBc/Hz	100 Hz -dBc/Hz	1 kHz -dBc/Hz	10 kHz -dBc/Hz	100 kHz -dBc/Hz	Test Notes
3-2 (74AC04)	99	130	149	158	159	161	2
3-3 (74AC04)	102	130	149	155	157	159	2
3-4 (MC10ELT21D)	101	129	134	135	135	135	2, 3
3-5 (LT1016)	98	118	118	119	119	120	2, 4
TYP LPRO	86	96	138	152	156	158	1
FRK LN	103	130	149	158	160	161	1

1. The Wenzel oscillator was used as a reference source for the phase noise test set.
2. The FRK-LN oscillator was used as a driving source for the sine-to-TTL circuit.
This oscillator was screened for best phase noise.
3. Test Figure 3-4 with Figure 3-3 used as a buffer, since Figure 3-4 cannot drive the low 50 ohms test.
4. Test Figure 3-5 with Figure 3-3 used as a buffer, since Figure 3-5 cannot drive the low 50 ohms test.



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Figure 3-2. Sine-to-TTL Conversion, Using C-MOS Logic, Recommended Approach

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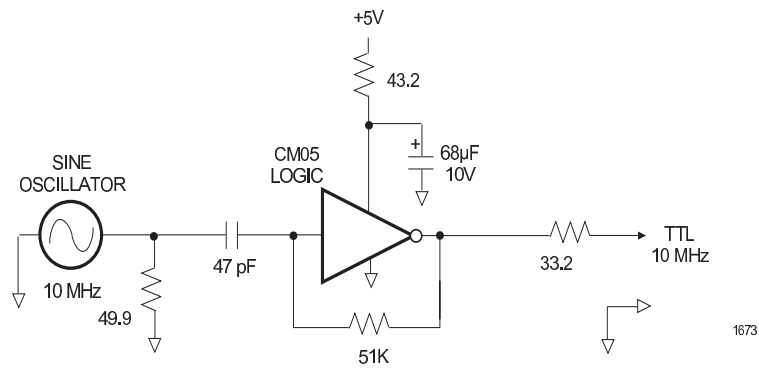


Figure 3-3. Sine-to-TTL Conversion, Using C-MOS Logic, Self-Bias Approach

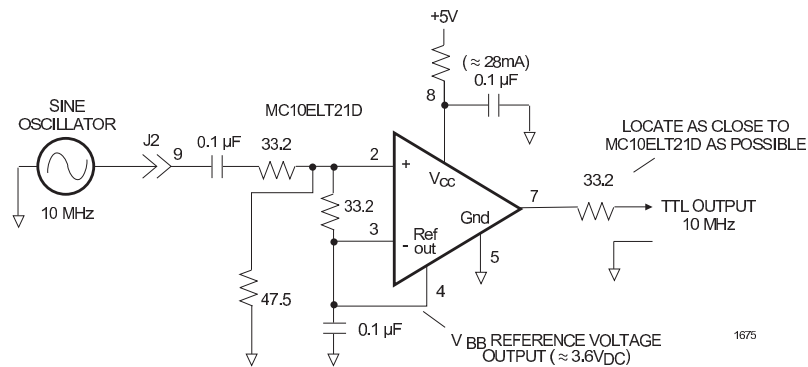


Figure 3-4. Sine-to-TTL Conversion Circuit, Using Positive ECL Converter

3.4.1.1.3 Use of a LT1016 Comparator

Figure 3-5 shows a sine to TTL converter using a high speed comparator. The advantage of this approach is the lower supply and ground noise compared to the ac-couple, high speed CMOS approach. The disadvantages are the higher phase noise and cost (compared to the ac-couple, CMOS approach), and the extra power dissipation (~24-29 milliamperes more at 5V).

3.4.1.2 rf Output Impedance versus Frequency

Figures 3-6 and 3-7 show the active rf output impedance for LPRO. It shows a nominal 50 ohms at 10 MHz, but a widely varying impedance at other frequencies. This would have to be taken into consideration by the user if running the LPRO rf output into a non-buffered filter.

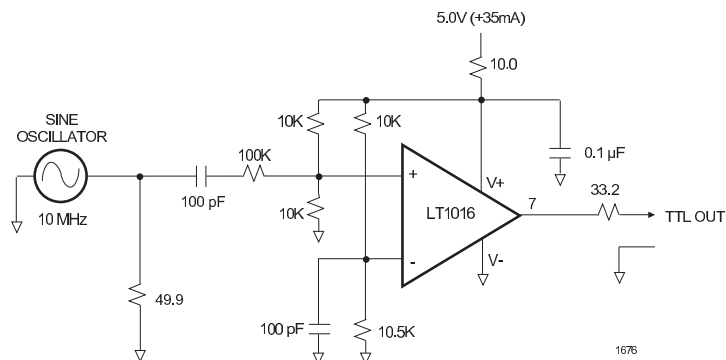


Figure 3-5. Sine-to-TTL Conversion Circuit Using a High Speed Comparator