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A Simple Reliable Power Amplifier with Minimal Component Count

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ABSTRACT

We study an audio power amplifier that has three essential active components: two power MOSFETS and one operational amplifier. Such an amplifier will be reliable because MOSFETS have good safe-operating area properties, and there are no small semiconductors that require high voltage ratings. The topology is that of an op-amp directly driving a grounded-source complementary class-B MOSFET output stage. The centre-tapped power supply for such an amplifier is floating, so each channel must have a separate supply, and there must be a small ±15-volt supply for the op-amp as well. We discuss the design and study the amplifier with simulations and an experimental prototype. It achieves good performance.

1. INTRODUCTION

Serious audio power amplifiers has evolved from the relatively simple but common vacuum tube push-pull amplifier to a variety of solid state embodiments with increasing levels of sophistication and complexity. To some extent, the reliability of any amplifier depends inversely on its complexity. For this reason, we have chosen to study an amplifier topology in which there are basically three active devices: two power MOSFETS and one operational amplifier. An op-amp isn't exactly one device, but from the point of view of ease of use and reliability, it tends to act as a single component. We can capitalize on this feature, yet use the high gain and excellent signal characteristics of such a device to our advantage. Although our final circuit will have some other small semiconductor devices, these occupy peripheral tasks such as current limiting, output stage biasing, and current sources for proper operation.

More recently, switching or class-D amplifiers are becoming commonplace in audio, but it is fair to say that audiophiles prefer a linear amplifier that does not involve switching. The amplifier here can be regarded as an audiophile type that optimizes simplicity and reliability.

Literature on using op-amps in audio power amplifiers goes back a long way [1], and books also cover this [2]. In early attempts, the output of the op-amp was simply boosted in current output. The maximum voltage of the amplifier was then curtailed by the op-amp supply rail voltage. There would be some voltage drop in the output transistors, and since the op-amp output is always a bit short of its rail voltage, the maximum output voltage might be limited to 15 volts or so even though the supply rails had 22 to 24 volts on them. Other subtle uses of op-amps included using the supply terminals as output signals to drive an output stage with higher voltage. We do not have space here for the litany of clever approaches that existed. A recent book [3] shows integrated circuit power amplifiers and drivers. We have sidestepped such approaches by using the op-amp output to drive the gates of a MOSFET grounded-source output stage, a rather uncommon topology not found much in the literature (but see [2] p. 112). Such an output stage has signal gain of more than a factor of 10. This means that only a few volts of signal swing are necessary, and even though some DC gate voltage bias is required, the op-amp can use ±15-volt rails, or even lower.

The penalty for using a grounded-source output stage is that the power output must now be taken from the center-tap of the MOSFET power supply, thus each channel requires an isolated supply, as well as a common ±15-volt supply for the op-amps. This increases the complexity of the power transformer a bit, but does guarantee a low coupling between channels. Fig. 1 shows the bare essentials of our topology, and would actually function. Two batteries of about 3.8 volts are shown that provide gate bias for the output MOSFETS, and two batteries of 40 volts each act as isolated high-power supplies. Because the output stage is inverting, the overall feedback must be returned to the non-inverting input of the op-amp.

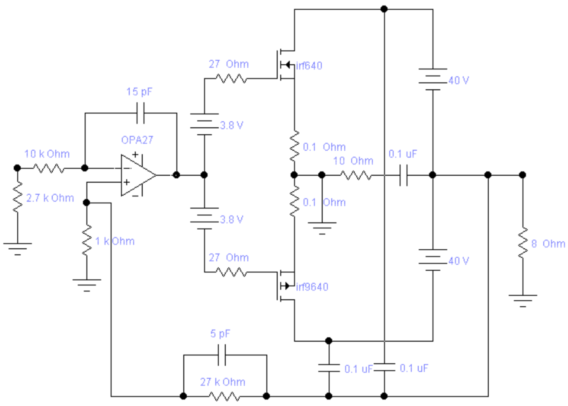

Figure 1. The barebones circuit of the amplifier. Two batteries are used to bias the MOSFET gates of the AB output stage.

An advantage of this topology is that no over-rail voltages are necessary to drive the MOSFETS. Therefore the peak output is essentially equal to the supply voltage for MOSFETS with low R_{DS}.

2. COMPONENT RATIONALE

Our choice of MOSFETS as output devices is based on two main criteria: they can be driven by very simple circuits since the gates represent capacitive loads, and their safe operating area (SOA) is not dominated by second breakdown as is the case for bipolar power transistors. The vertical power devices chosen have high current capacity, but do have a gate threshold of nearly 4 volts. Lateral MOSFETS would have lower threshold voltage. Most op-amps are fine because they have sufficient output current to drive the capacitive gates even at the highest audio frequencies. They also have gain to spare, and can be seconded as a combined input stage, voltage amplifying stage, and driver stage, all wrapped into one convenient, reliable package. There may be audiophiles that distrust any op-amp in an audio system, but the shortcomings of a few of the early devices have long been eliminated. Today's better op-amps are incredibly linear, have no crossover distortion, and have very low noise. It would be a travesty not to utilize these properties in our amplifier.

3. REFINING THE DESIGN

The final schematic of our design is shown in Fig. 2. The op-amp and the two power MOSFETS Q1 and Q2 are evident. A heat sink is essential for the MOSFETS, and the diodes D1 and D2 may be mounted on this heat-sink for thermal compensation. Simple current limiting is implemented by transistors Q3 and Q4, which divert the gate signal when the source resistors R1 and R2 develop a voltage larger than the base-emitter turnon voltage of about 0.7 volts. Transistors Q5 and Q6, diodes D1 and D2, and associated resistors constitute the bias spreader, to bias the output MOSFETS into partial conduction for the class AB output stage. Transistors Q7 and Q8 and associated resistors act as current sources to feed the bias spreader.

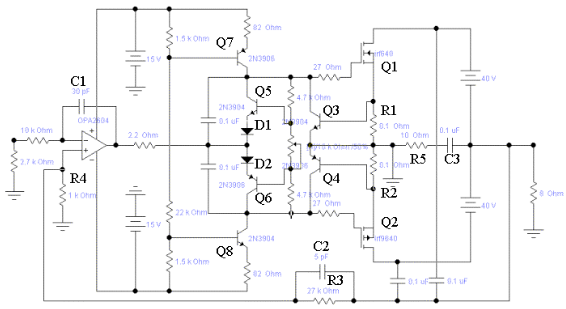

Figure 2. Complete schematic of the amplifier. The six small bipolar transistors are used for current limiting, bias setting, and current sources.

Since the output stage is inverting, the overall feedback must return to the non-inverting op-amp input terminal. C2 creates a phase lead to help stabilize the amplifier. In addition C1 provides local very high-frequency feedback to the op-amp. These two feedback paths can be looked on as a sort of crossover network.

The gain of the output stage itself is approximately 20 with an 8-ohm load. The MOSFETs have a gate-to-source capacitance up to 1150 pF, and a gate-to-drain capacitance up to 130 pF. The Miller effect makes the 130 pF gate-to-drain capacitance act like $21 \times 130 = 2730$ pF. For a peak output voltage of 30 volts, the gate needs 1.5 volts peak. The total input capacitance for two similar but complementary MOSFETS is 2×1150 pF+2×2730 pF=7.8 nF. At 20 kHz, the total peak gate current that will be required is ωCV_p=1.5 mA. The current sources Q7 and Q8 are set to 10 mA, so the bias spreader will never be reverse biased.

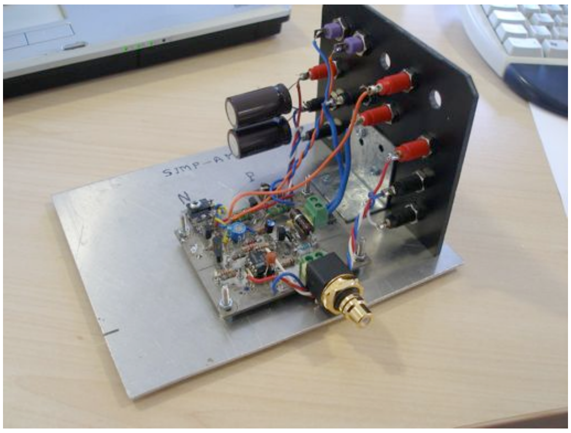

Figure 3. Photograph of prototype amplifier, with the two MOSFETS mounted on an aluminum plate. A small transistor used as a diode is mounted on the N-channel MOSFET for thermal bias tracking.

Note that the 27 Ω parasitic suppression resistors in series with each gate will have a first-order rolloff above 1.5 MHz. There will be negligible voltage drop across them even well beyond the highest audio frequencies. Note also that if the output stage has a different gain, the Miller capacitance is altered, but so is the required peak gate voltage, in such a way that the gate current does not change much.

4. PARASITIC OSCILLATIONS

MOSFETS have very high frequency response, being majority-carrier devices, and they can oscillate at hundreds of MHz unless care is taken to avoid this. The series gate resistors (to suppress HF parasitic oscillation) are mounted very close to the MOSFET packages. These resistors have short clipped leads directly soldered to the gate lead, which has also been clipped short. The source resistors have been bypassed by 0.1 μF surface-mount capacitors (not shown on the diagram), and the MOSFET drains have been bypassed to the feedback line and the Zobel network (R5, C3) with very close-mounted capacitors as well. A ground plane is recommended to lower trace inductance. All of these precautions reduce wiring inductance and help to tame spurious oscillation of the MOSFETS. This is necessary because we have chosen to use very low-value gate resistors, which keeps the bandwidth of the output stage very high. This allows the output stage crossover distortion to be reduced by feedback to much higher frequencies, as we shall explore in future.

5. THERMAL COMPENSATION

The vertical power MOSFETS chosen have thermal coefficients of gate voltage of about –6mV/°C to maintain the same current, at a bias current of about 150 mA [3]. A normal semiconductor diode has a thermal coefficient of about –2.2 mV/°C. This will be increased by the multiplication factor of the bias spreader. Our spreader as drawn has two diode drops for each gate, representing 1.4 volts, which must be raised to 4 volts to bias the MOSFET. This is a multiplier of just under 3, so with one diode on each half on the heat sink, the thermal coefficient is about –6.3 mV/°C, which is reasonable. When we mounted just one of the diodes on the heat sink, the prototype was only slightly undercompensated, so the thermal coefficients of our MOSFETS must be a bit smaller than –6mV/°C. The driving point of the output stage is completely symmetrical, although with the very high DC gain of the op-amp, that will not matter much, and one of the diodes could be removed if we so choose.

6. TESTING THE AMPLIFIER

The ±40V power supply for the MOSFETS is an unregulated capacitor-input split supply. It will have ripple, of course, but this is at a low frequency of 100 or 120 Hz, at which the gain of the op-amp will be very high. Thus we do not expect significant distortion from gain modulation or ripple injection.

The output stage will have distortion, and since the global feedback ensures that the output waveform is essentially free of distortion, we can observe the gate signal at the op-amp output to assess the efficacy of our bias setting. Underbias causes the waveform at this point to have higher slope near zero crossing, since there is a dead spot near the origin in the output transfer characteristic. Overbias will give the waveform a lower slope near zero crossing. Optimum bias will make the gate waveform most sinusoidal. This can be set quite easily by eye, and the bias current can then be assessed for acceptability. If the distortion is very low, we can reduce the bias below optimum values to reduce the quiescent power required by the amplifier. We have used Electronics Workbench™ to simulate the amplifier; many of the simulated characteristics were verified by actual measurements on the prototype.

Stability is more difficult to optimize. Capacitors C1 and C2 determine the frequency characteristic of the amplifier. Distortion will be reduced at higher frequencies if we coax the amplifier to have more HF gain, but this may compromise stability. The reduction of distortion, in the view of the authors, must always be tempered by considerations of practicality, audibility, and aesthetics. Optimization of the compensation to achieve much lower distortion will be left to a future paper.

7. PERFORMANCE

The amplifier was tested with a ±45 volt supply that had a relatively high internal impedance due to the small transformer. Figure 4 shows the distortion THD+N versus frequency at 2.8Vrms output with a filter bandwidth of 80 kHz. The quiescent bias current on the MOSFETS was close to 100 mA. C1 was 10 pF, C2 was 4.7 pF, and the op-amp was an LF351. Distortion at the lower frequencies is at the 0.01% level, rising 6 dB/octave above about 1 kHz. This rise is due to the falling op-amp gain with frequency.

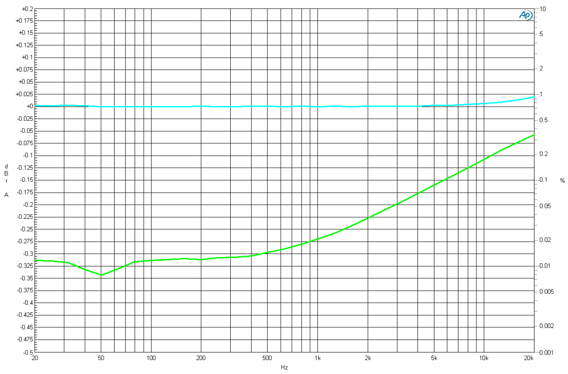

Figure 4. THD+N versus frequency (green) at a signal level of 2.8Vrms into 8 ohms. The limiting distortion of 0.01% may be partially due to noise in the test setup. The cyan curve is the frequency response, showing a slight peaking of 0.02 dB near 20 kHz.

The rise of distortion is of low order and not worrying. The op-amp is unity-gain compensated, thus its gain falls 6dB/octave above about 100 Hz. Distortion at low frequencies is determined mainly by the nonlinearity of the output stage, and is predominantly of low order.

The THD+N versus level at 1 kHz is shown in Figure 5. The curve shows little peaking at lower levels, thus the output stage is reasonably well biased into the AB region. Clipping occurs at about 45 watts for this power supply, which is poorly regulated and comes down to about 28 volts under load.

We might have expected more variation of the distortion with level, and do not know why this is so. Perhaps there is a small residue of the switching between the two output MOSFETS. This would produce a fairly constant distortion with level, which would go down at very low level. This is starting to happen near 1 watt of output, which is the lowest point on the graph.

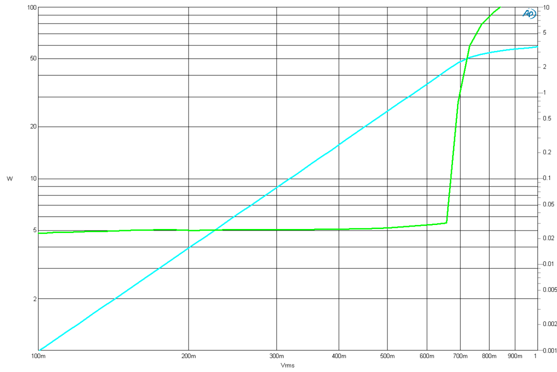

Figure 5. THD+N versus input level (green) at 1 kHz into 8 ohms. The flat portion of the curve is at 0.03%. The cyan curve shows the power output.

These measurements represent the amplifier with very conservative frequency compensation. Future study will involve more analysis of this compensation, and attempts to significantly lower distortion.

8. ACKNOWLEDGEMENTS

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9. REFERENCES

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