

Short collection of information regarding harmonic distortion

Intention of this text is to show and explain how a single tone signal is changed by distortion caused by different circuit topologies and combinations of these topologies to control the distortion pattern.

Simulation results are used to depict the effects that are theoretically derived. Because simulation models aren't perfect, the simulations will not be in perfect alignment with measurements on real circuitries. But that's no problem since it is not the intention here to give ready to use schematics but to show the basic working principles. In fact most of the circuitries shown here are quick hacks made with the sole intention to show an extremely simple circuitry and its basic working behaviour.

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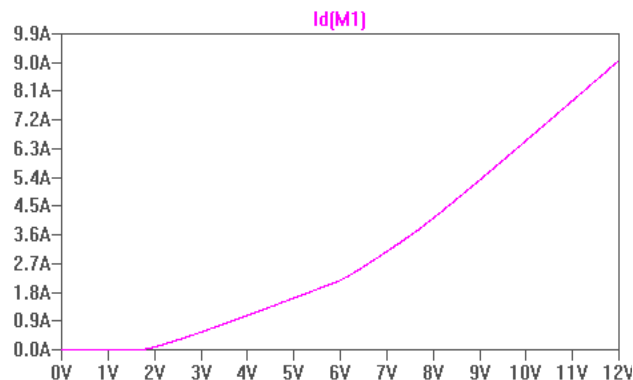
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A. Preferred transistor transfer characteristic

X = input signal (on MOSFETs that's U_{gs})

Y = output signal (and that would be I_d)

That could look like this:



Such a transfer curve can be approximated by a polynomial:

$$y = c_0 + c_1 \cdot x + c_2 \cdot x^2 + c_3 \cdot x^3 + \dots + c_n \cdot x^n$$

(An algorithm called “linear regression” can calculate the coefficients $c_0, c_1, c_2, \dots, c_n$ from the data points of the curve in the picture so that the polynomial fits best the curve. The sharper the edges in the curve are and for every change in steepness direction more higher order coefficients are necessary for a good fit. In contrast for a very smooth curve only low order coefficients are used. Below that becomes important.)

The picture above can be seen on a curve tracer, when the input voltage is increased from 0V to 12V and the Drain current is measured.

If that simple increased signal is replaced with a sinusoidal input signal $x = \sin(2 \cdot \pi \cdot f \cdot t)$ and the abbreviation $2 \cdot \pi \cdot f \cdot t = u$

the polynomial becomes

$$y = c_0 + c_1 \cdot \sin(u) + c_2 \cdot (\sin(u))^2 + c_3 \cdot (\sin(u))^3 + c_4 \cdot (\sin(u))^4 + \dots + c_n \cdot (\sin(u))^n$$

With the addition theorems

$$(\sin(u))^2 = \frac{1}{2} \cdot (1 - \cos(2 \cdot u))$$

$$(\sin(u))^3 = \frac{1}{4} \cdot (3 \cdot \sin(u) - \sin(3 \cdot u))$$

$$(\sin(u))^4 = \frac{1}{8} \cdot (\cos(4 \cdot u) - 4 \cdot \cos(2 \cdot u) + 3)$$

that becomes:

$$y = c_0 + c_1 \cdot \sin(u) + c_2 \cdot \frac{1}{2} \cdot (1 - \cos(2 \cdot u)) + c_3 \cdot (\sin(u))^3 + \frac{1}{8} \cdot (\cos(4 \cdot u) - 4 \cdot \cos(2 \cdot u) + 3) + \dots$$

or in short form (after a little reorganisation)

$$y = k_0 + k_1 \cdot \sin(u) + k_2 \cdot \sin(2 \cdot u) + k_3 \cdot \sin(3 \cdot u) + k_4 \cdot \sin(4 \cdot u) + \dots + k_n \cdot \sin(n \cdot u)$$

Result 1:

The non linear characteristic of the transistor creates new frequencies in the output signal that were not existent in the input signal. Their amount is given by the coefficients k_2 , k_3 , k_4 , ...

Result 2:

The order of each coefficient gives the order of its highest created harmonic, e.g. c_3 creates the third harmonic, c_4 creates the fourth harmonic and the second harmonic and so on.

Conclusion 1:

If we want to avoid that higher order harmonics are created (because the fourth, fifth, sixth and so on sound bad), we need to make sure that the higher order coefficients in the polynomial expression are as small as possible. That in return means, that there should be no sharp edges in the transfer curve of the transistor and that a strongly bent line (so to say a "bow" like for example $y = x^2$) is less disturbing than a line that is more or less linear but has small edges. The latter is created by cross over or when a fancy linearisation circuitry kicks in at certain signal levels. In addition, below is shown a method how to cancel even order harmonic with a simple circuit topology, that works best for low order harmonics k_2 , k_4 , k_6 .

Conclusion 2:

"there should be no sharp edges in the transfer curve of the transistor" also means that the transistor should not only be chosen for its smooth transfer characteristic and operated in a smooth region of that characteristic but also that the characteristic should not be modulated by the signal. That effect is known as "memory distortion" and can be found in the internet. Short form of the conclusion: the power (and heat) of the transistor should be held constant to avoid memory distortion.

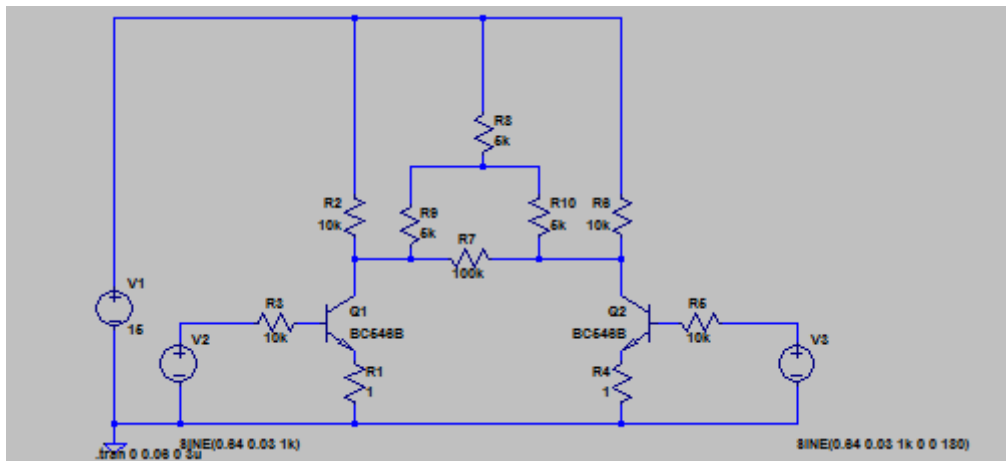
The next step is to combine transistors in basic circuitries and to see how they influence the distortion patterns.

B. Basic topologies influencing harmonic distortion

Transistors can be combined in different basic topologies:

a.) Differential stage:

The input signal is applied with opposite phase to 2 identical transistor stages (Q1 and Q2) and the output signal is taken between their 2 outputs (R7). Circuitry 1:



What happens, when the transfer characteristic of the transistors is pure linear (e.g. only c_1 is not 0)?

Let x be the input signal (positive for one transistor, negative for the other) and q the quiescent current and the transfer function is $y = c_1 * x$ (and even shorter with $c_1 = 1$): $y = x$

$$\text{output} = (q + x) - (q - x)$$

that evaluates to:

$$\text{output} = 2 * x$$

The output contains only the first harmonic (or k_1). No other harmonics are cancelled or created. There is no distortion.

And now let the transfer characteristic be pure square law:

Again, let x be the input signal (positive for one transistor, negative for the other) and q the quiescent current and the transfer function is $y = c_2 * x^2$ (and even shorter with $c_2 = 1$): $y = x^2$

So the output signal becomes:

$$\text{output} = (q + x)^2 - (q - x)^2$$

$$\text{output} = q^2 + 2 * x * q + x^2 - (q^2 - 2 * x * q + x^2)$$

$$\text{output} = 4 * x * q$$

Here we see, that the second harmonic that is created by the non linearity c_2 is cancelled and the output only contains a constant factor ($4 * q$) and the first harmonic. There is no distortion.

And now the same calculation with cubic transfer function, e.g. c_3 is not 0:

$$\text{output} = (q + x)^3 - (q - x)^3$$

$$\text{output} = q^3 + 3 * q^2 * x + 3 * q * x^2 + x^3 - (q^3 - 3 * q^2 * x + 3 * q * x^2 - x^3)$$

$$\text{output} = 2 * x^3 + 6 * q * x^2$$

The output signal contains the third and first harmonic; the second harmonic is created (as you can see in the terms containing x^2) and cancelled. The third harmonic is distortion and is not cancelled.

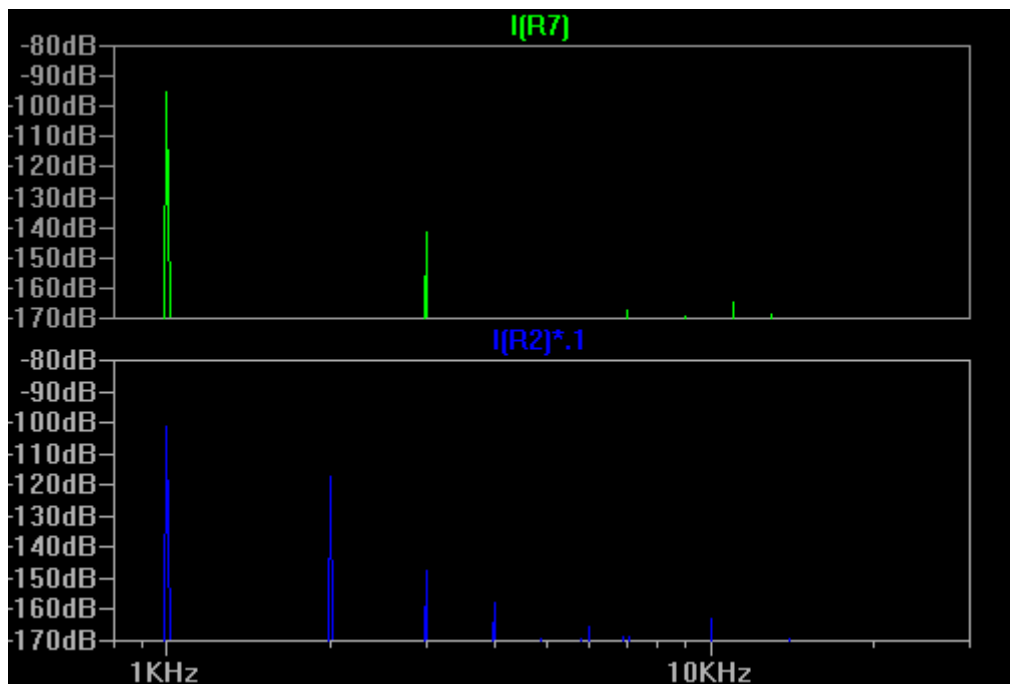
You can continue the calculation for c_4 , c_5 and so on. The result will be: even order harmonics are cancelled by the differential stages, odd harmonics not. (Result 2)

In the diagram below you can see that.

$I(R_2)$ is the output signal of one stage (Q_1) and it contains $k_1, k_2, k_3, k_4, k_5, k_6, k_7, \dots$

$I(R_7)$ is the differential output signal and contains only the signal frequencies 1kHz, 3kHz, 5kHz, 7kHz, ... e.g. k_1, k_3, k_5, k_7 and so on. The even order harmonics k_2, k_4, k_6, \dots which are present in $I(R_2)$ are cancelled in the signal $I(R_7)$.

This cancellation will work better the more similar the transistors of the differential stage are.



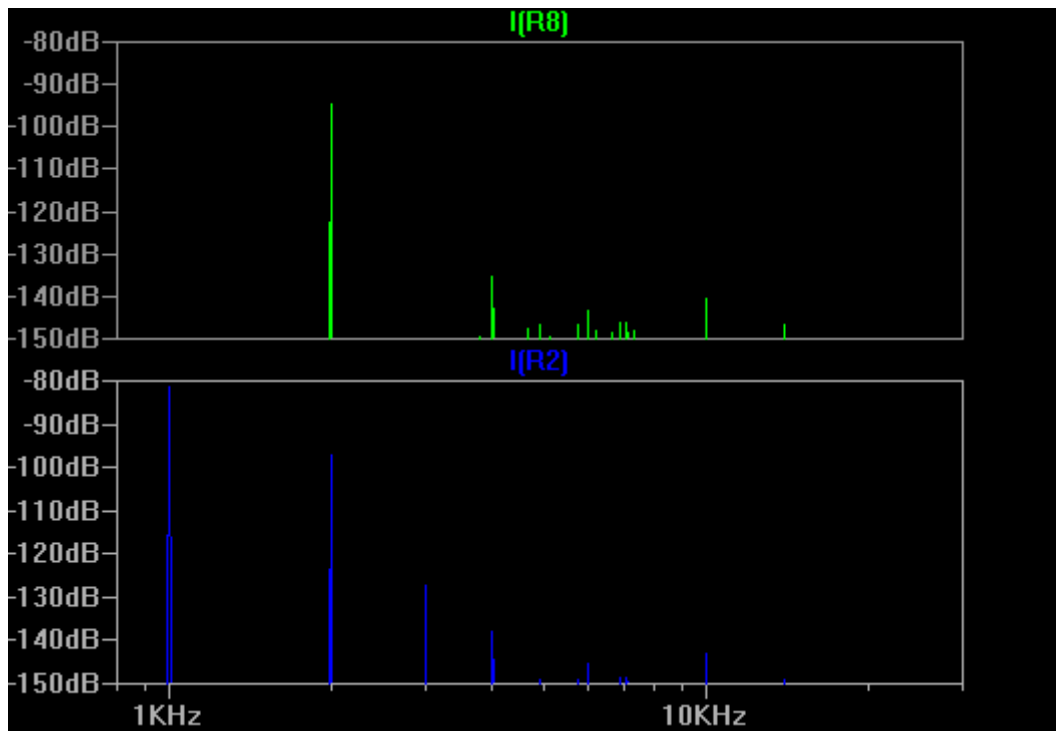
b.) summing stage

As shown it is possible to cancel the even order harmonics with a differential stage.

With a summing stage, it is possible to cancel the odd order harmonics. (Result 3)

The mathematics for that are the same as above, only the minus sign has to be changed into a plus sign. For example, $\text{output} = (q + x)^2 - (q - x)^2$ of the differential stage becomes $\text{output} = (q + x)^2 + (q - x)^2$ in the summing stage.

In the circuitry above the summing signal is generated with 2 current summing resistors R9 and R10 and their currents are summed up in R8. The picture below shows the distortion spectrum of the current through R8, $I(R8)$. There is no $k1, k3, k5, k7$ and so on, only $k2, k4, k6, \dots$ (except for a little "dirt" around $k6$, which is very likely simulation artefacts).



c.) multiplying stage

That is simply the function of one transistor stage amplifying the signal. The mathematics are shown in the formulas mentioned right above result 1.

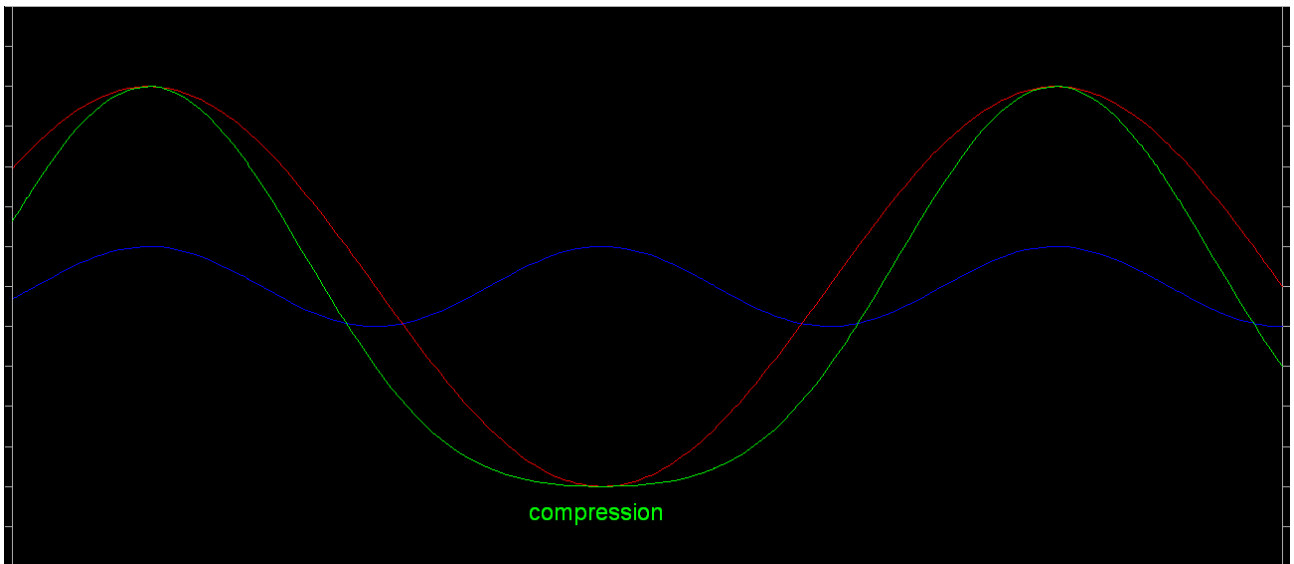
d.) dividing stage

Well that is a simple voltage divider made of two resistors. One example is a feedback network.

C. Phase of harmonics

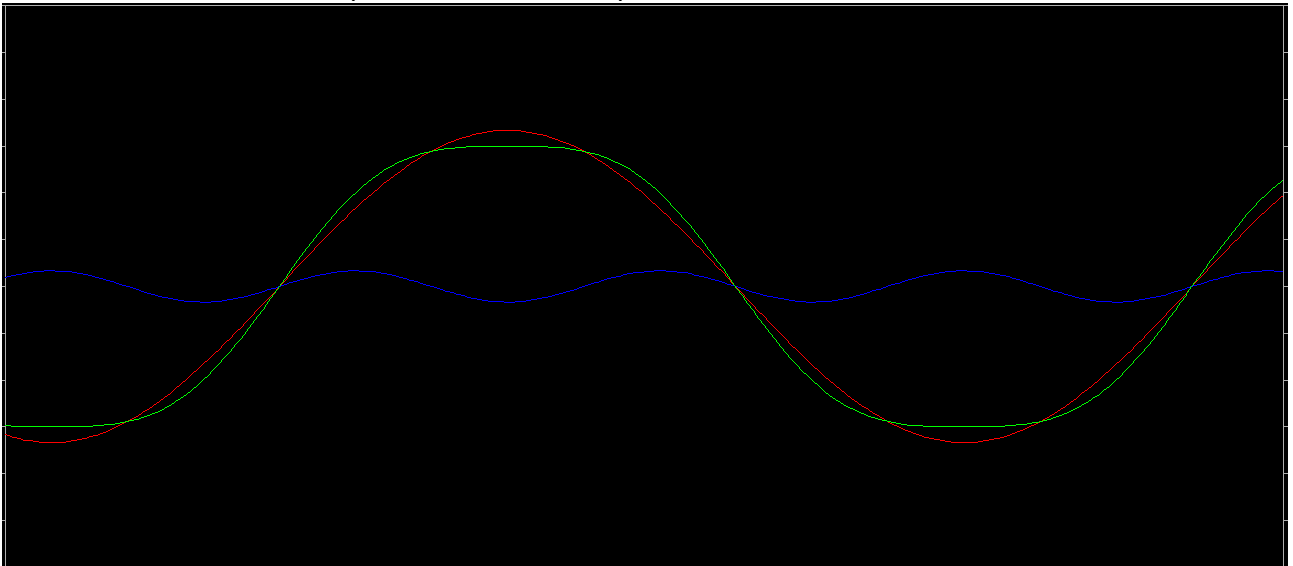
a.) K2

Before the mathematics of the theory of the creation of the distortions was discussed. In real life k_2 is a limit in excursion of the positive or the negative amplitude and k_3 is the limit for both amplitudes. For example a loudspeaker cone may easier move forward than backward due to its construction. In the picture below the movement of the cone is the green line. You can see where the compression occurs. For this constellation, where the compression occurs at the negative amplitude, k_1 and k_2 have the shown phase relation. For the other constellation, where the compression occurs at the positive amplitude, the k_2 is 180° shifted (or in other words reversed). (Want to see that picture? Simply turn this page around, upside down.)



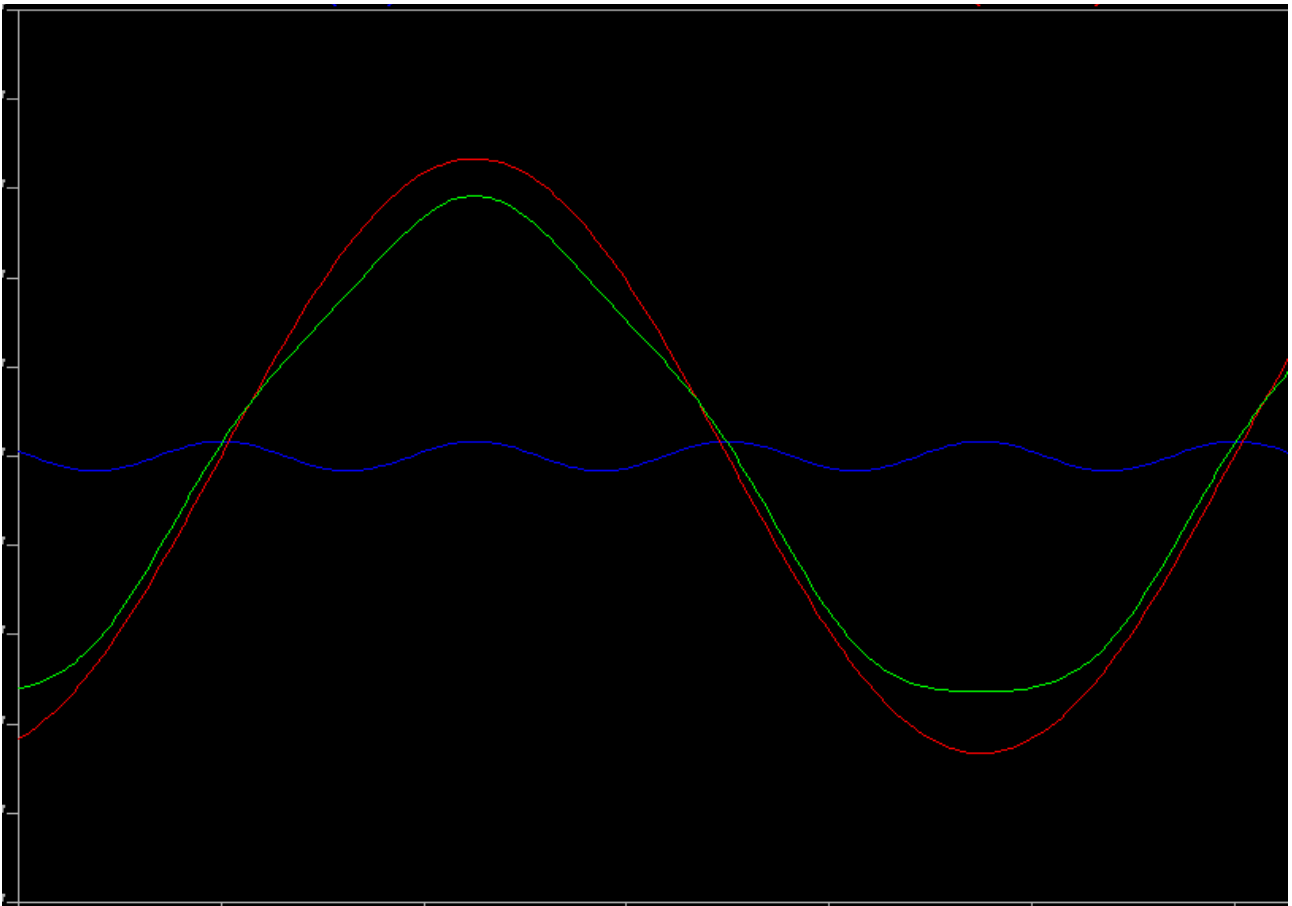
b.) K3

And here is k3 shown, compression on both amplitudes:



c.) K4

Here is a picture of k4. The compression looks strange and seems to have no natural equivalence. In addition, the amplitude of k4 is only half the value of k3 in the picture above. That was necessary to maintain a smooth curve with a visually dominant k1.



D. Collection of comments on the perception of distortions from various sources.

Because the perception is not identical for everybody this can only be a raw scheme and not a precise description.

- k_2 is audible as a separate tone when it becomes bigger than 1% of k_1 . Test was done with sine generators and constant signal.
- k_3 in the same test was audible at a far smaller level, 0.1% of k_1 when I remember correctly
- k_4 , k_5 , k_6 ,... were always regarded as disturbing
- k_2 with a compression at the negative amplitude has attack, while at the positive amplitude sounds distant
- k_2 brings soul
- k_3 is fast and crisp
- many natural sounding instruments have a harmonic spectrum of the form $k_1 > k_2 > k_3 > k_4 > k_5 > k_6 > \dots$ (of course ">" means "greater than") Because the spectrum creates the sound, the spectrum should not be changed in a way that is not natural.
- Some say the lower order distortions mask the higher order distortions and thus make them less audible. If $k_1 > k_2 > k_3 > k_4 > k_5 > k_6 > \dots$ is true, the sonic signature of the amplifier is similar to the natural sounds and thus is less disturbing. So if it is not possible in an amplifier to reduce the higher order distortions below the audible level, it would be in this sense better to create lower order harmonics to mask the higher order distortions.

- The higher distortion is, the higher is the amount of the mixing products of signals with different frequencies. Mixing products are completely unnatural and thus very disturbing.

In the next step, the basic circuitries are combined to form a complete amplifier and to see how it influences the distortion patterns.

E. Usage of basic topologies in complete amplifiers

The basic topologies to be put together for a complete amplifier are:

- multiplying stage
- differential stage
- dividing stage
- summing stage

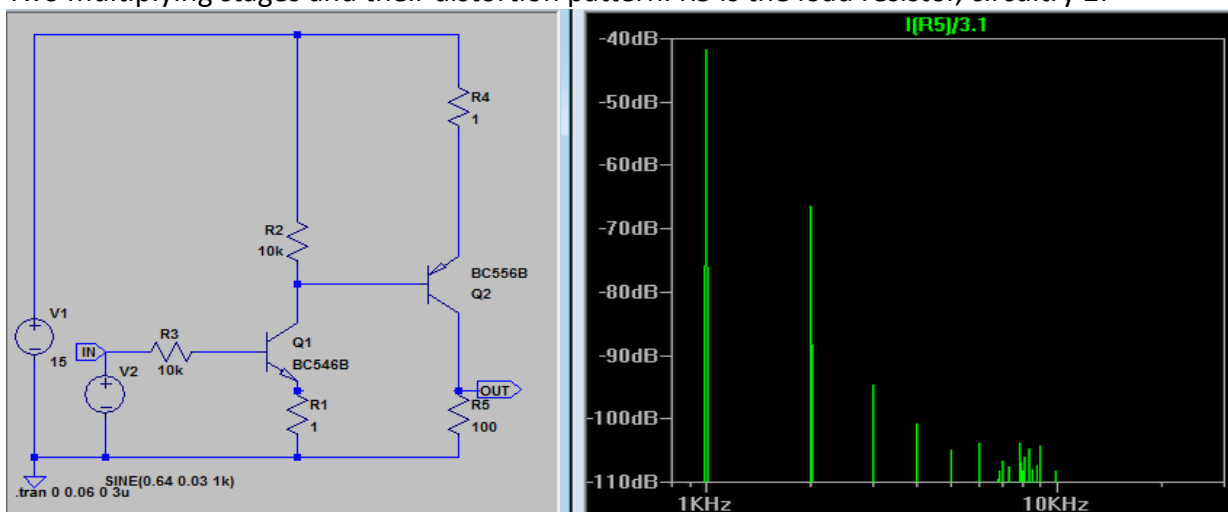
I will use bipolar transistors here because they have lots of distortion (which is helpful in this text). Of course the findings here are true for other type of transistors like MOSFETs for example.

The intension of the circuitries used here is to show in a simple way the effect of the combination of the different topologies. Everything that is necessary to make an amplifier reliable or suitable to drive real loudspeakers would have made the circuitries more complicated and hence was left out. So the amplifiers shown here are not suitable for real loudspeakers. But the conclusions derived here can be used for designing serious amplifiers for real loudspeakers.

a.) multiplying stages

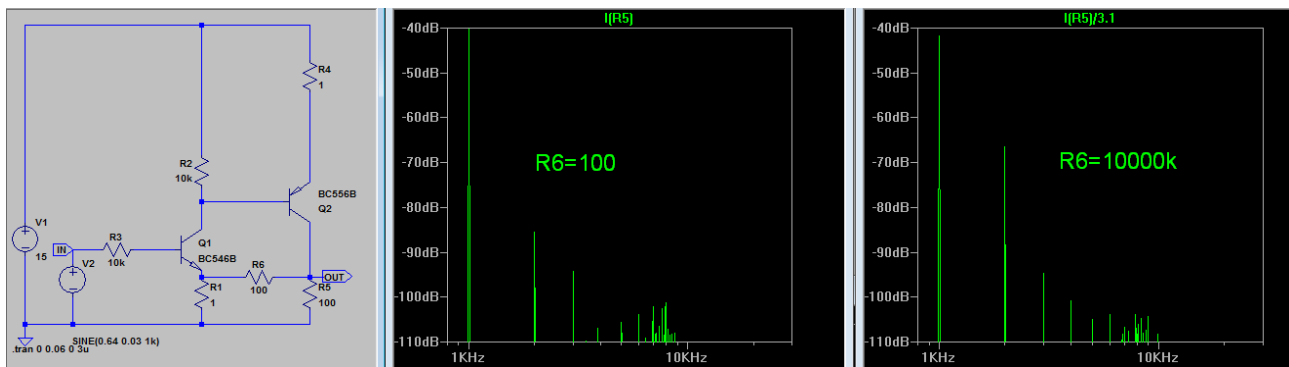
Here it starts with something very simple:

Two multiplying stages and their distortion pattern. R5 is the load resistor, circuitry 2:



b.) dividing stage

Adding a dividing stage as feedback, circuitry 3:



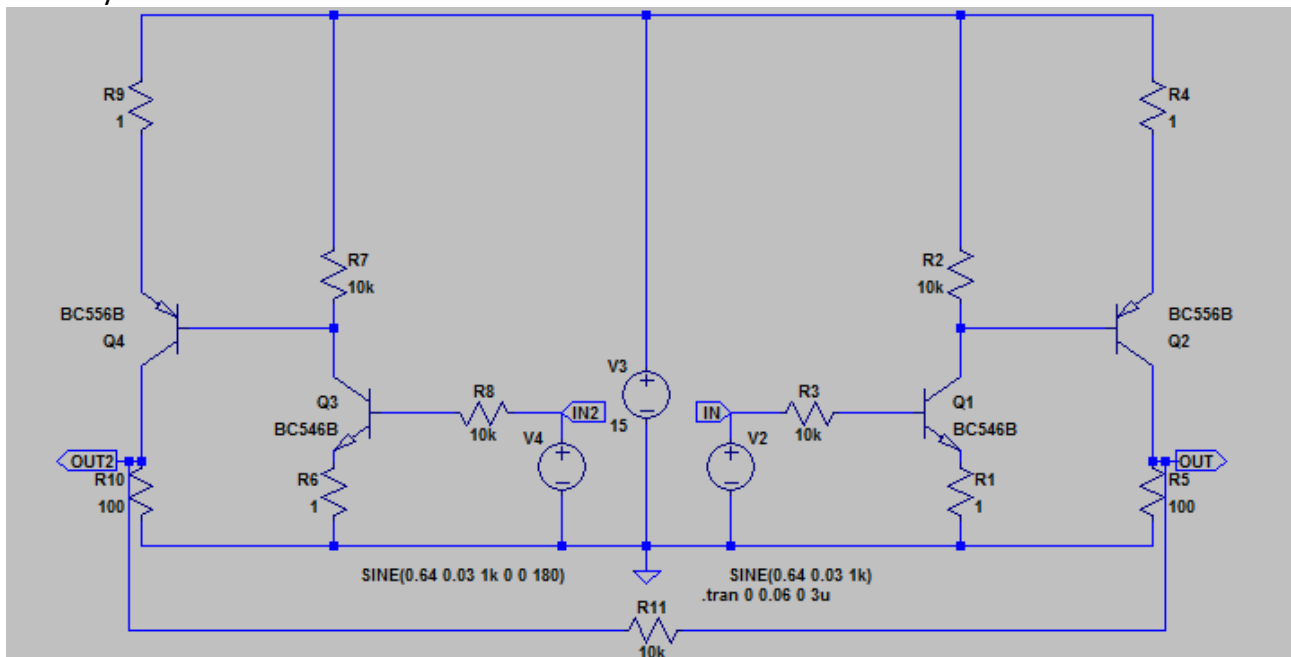
Distortion is reduced by feedback with $R_6=100$ (which forms a voltage divider with R_1). With $R_6=10000k$, R_6 is not relevant anymore, which is the same as if it is removed.

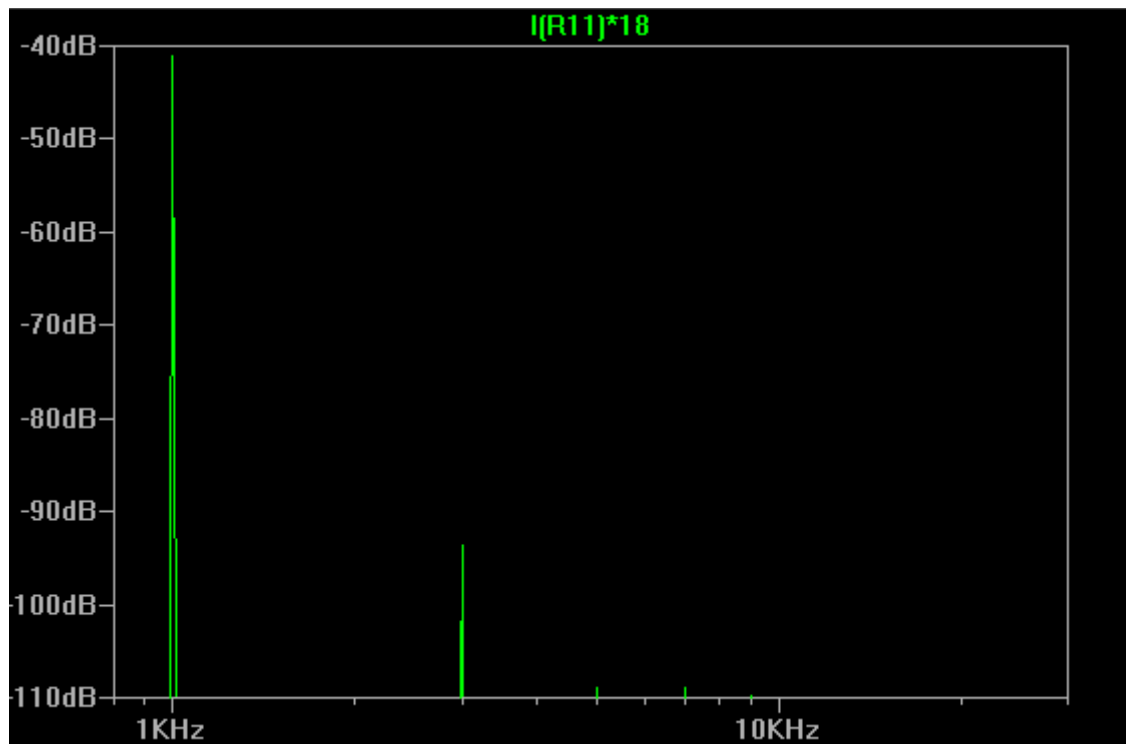
c.) differential stage, type 1

Now circuitry 4: Circuitry 2 is simply duplicated and driven with a differential, symmetrical signal. Thus circuitry 4 is a differential stage. Note: The distortion spectrum is a lot cleaner than circuitry 3 although the feedback resistor R6 is removed. The distortion is cancelled as described above in chapter B. a.)

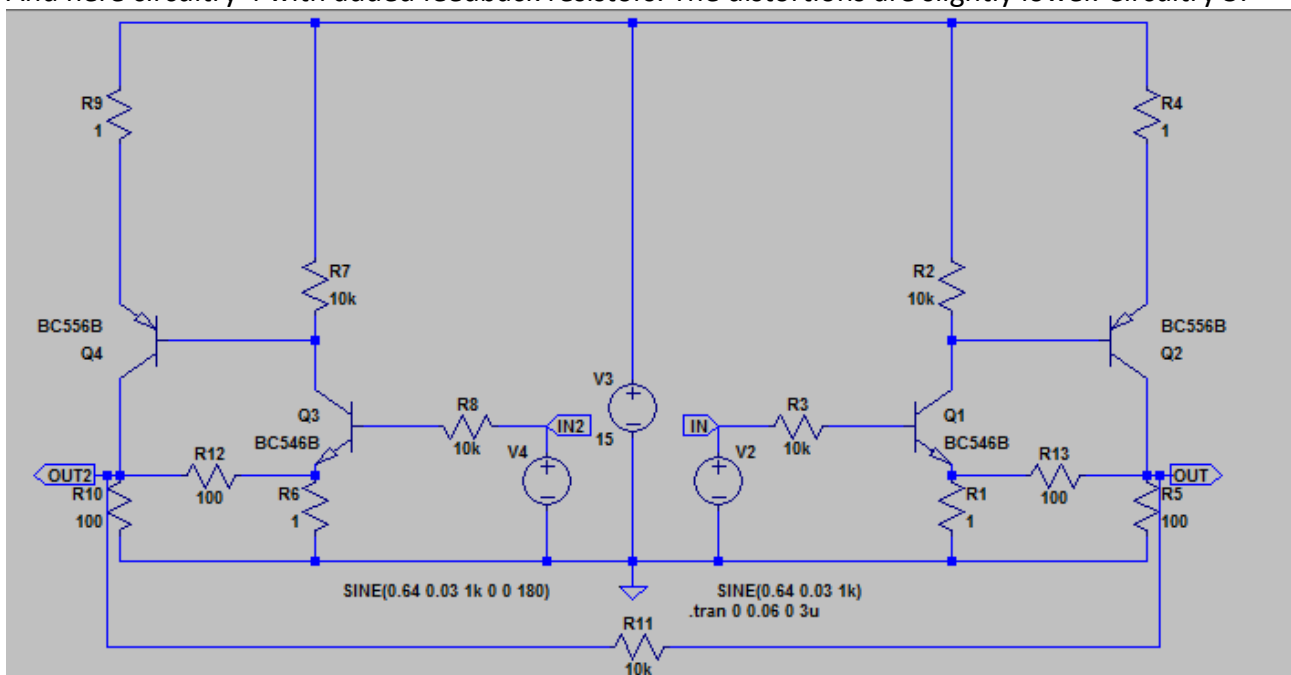
(R11 is used because there seems to be no way in LTspice to display the distortion pattern of a differential signal. So as a work around a high ohmic resistor can be used which does not interfere with the circuitry and its current is proportional to the differential voltage.)

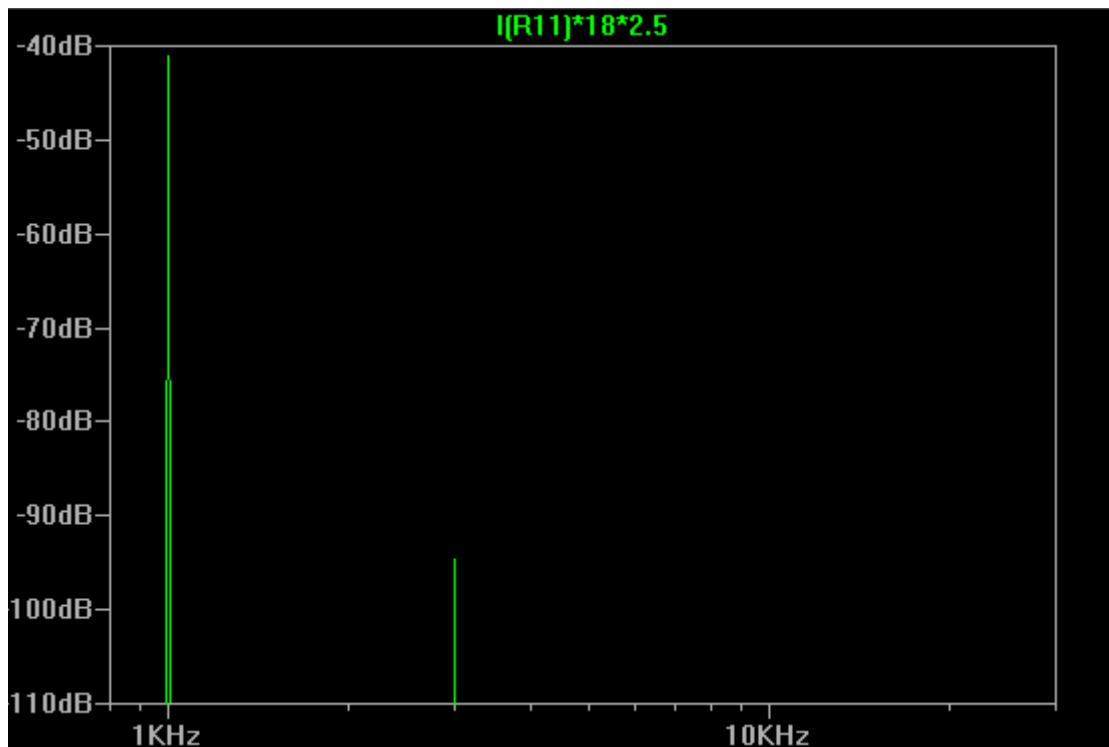
Circuitry 4:





And here circuitry 4 with added feedback resistors. The distortions are slightly lower. Circuitry 5:





In circuitries 4 and 5 the second harmonic ($= k_2$) is completely cancelled.

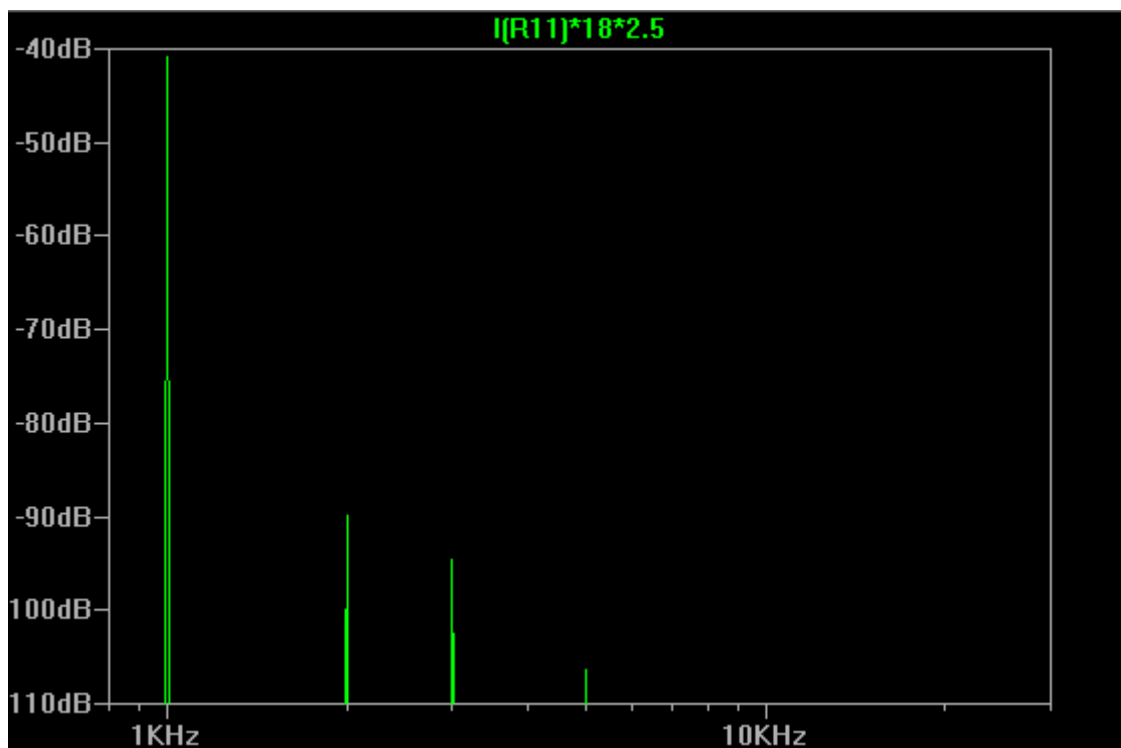
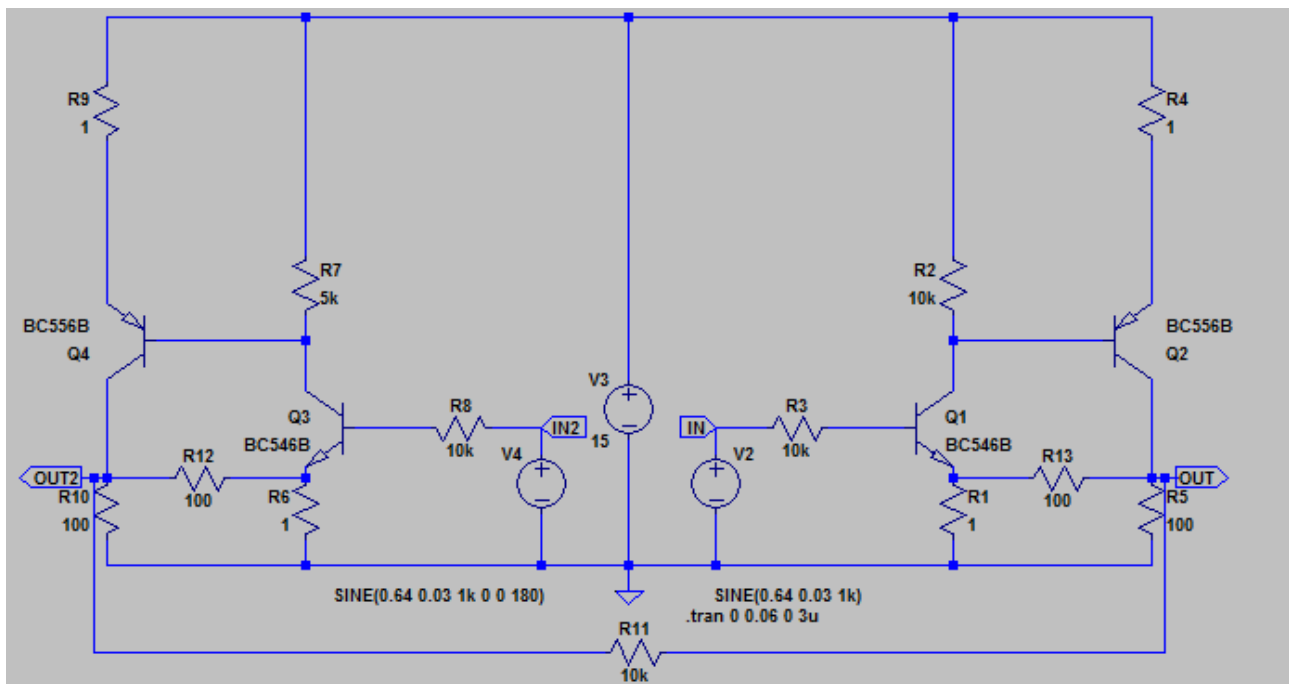
d.) controlling k_2

Because the amount and phase of k_2 changes the sound (see Chapter C), it is an advantage if k_2 can be controlled.

Here is an example, circuitry 6:

R7 is changed from 10k to 5k thus the current through R7 is doubled and not only the quiescent current through R9 is increased but also its amplitude ($\pm 30\text{mA}$ against $\pm 27\text{mA}$). Please note, that only R7 was changed and not its counterpart on the other side of the differential stage, R2! That non-equality creates an imbalance in the amplification factor of the two halves of the amplifier. As a result, the positive amplitude on OUT2 is amplified a little bit more than the one on OUT, so if we define OUT2 to be the + output post of the amplifier and OUT the negative, we see that the positive output amplitude of the amplifier is a little bit bigger than the negative. That is shown in the first picture in Chapter C, in which the negative amplitude is commented with "compression". If also R2 would be changed to 5k, the positive and the negative amplitude would be the same and the result would be the creation of k_3 in case of compression of both amplitudes as shown above, and not k_2 .

Circuitry 6:

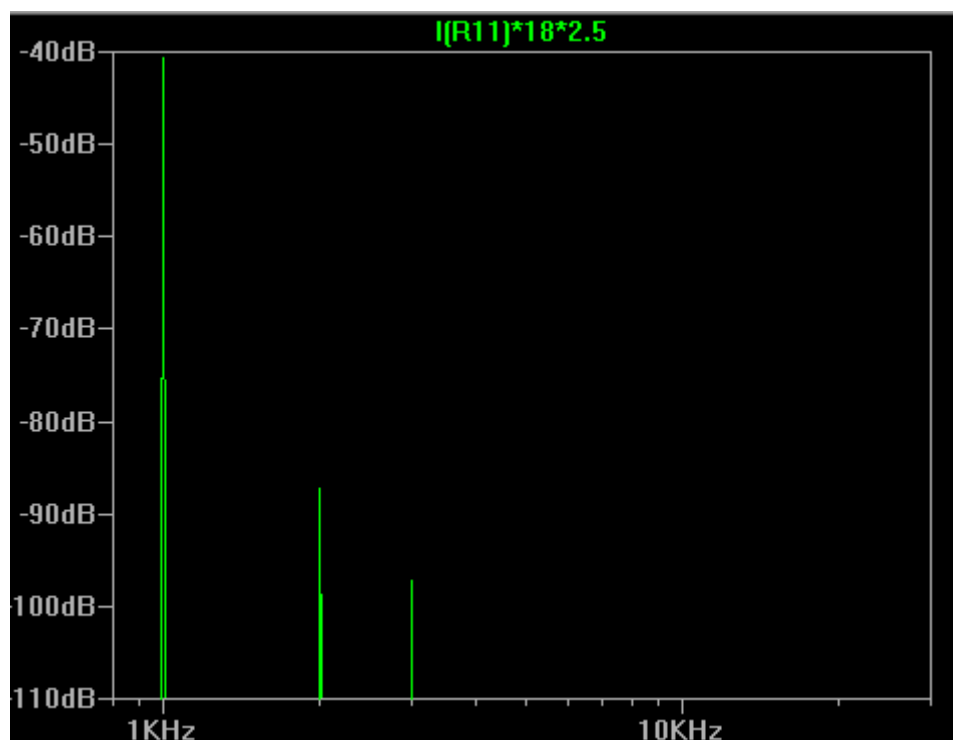
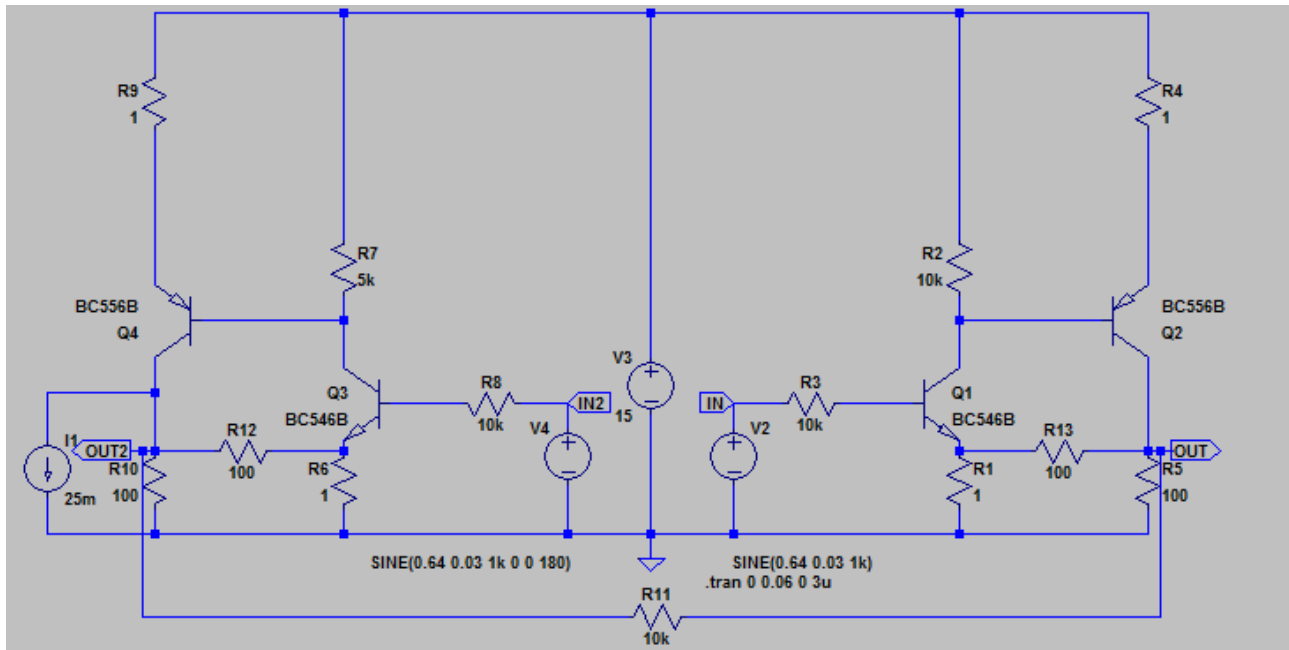


As an unwanted side effect, also k5 has raised a little bit.

e.) suppressing higher order distortions

In circuitry 7 a constant current source (I1) is added to suppress k5. As nice side effect, k2 is further

increased and k_3 is decreased. Position of I_1 (over load resistor or over Q_4 and R_9) was found in experiment and also the amount (25mA). There seems to be no strict or simple rule for position and amount.



In circuitry 7 the output signal of the differential stage is the voltage between the two outputs OUT and OUT2. This is here called a differential stage type 1. The minus operation as shown in the beginning of this text is performed while (or because) the output is the difference between the two outputs. Thus with one output this circuitry would not be a differential stage.

f.) differential stage, type 2

If you compare that with a standard differential input stage as shown in circuitry 8 (which is called type 2 here), you will see, that the type 2 uses only one output signal and not two. So type 2 circuitry must work in another way than circuitry 1. How does this stage perform the difference operation? When Q2 has a higher voltage at its base it conducts more emitter current and so it takes away that amount of current from Q1: $10\text{mA} - I_{EQ2} = I_{EQ1}$ (= the emitter current of Q1). The mathematics for this is a lot more complicated than the previous one.

(If you like here is a very simple (and not precise) attempt:

According to the formula mentioned above (for example output = $(q + x)^2 - (q - x)^2$)

here we can describe the transfer functions (only the square functions are shown here) as

$I_{EQ} = (q + x)^2$; here q is the quiescent voltage that causes an emitter quiescent current of 5mA and x is the input signal voltage.

x is nearly the same for Q1 and Q2 but with opposite sign.

Thus

$$I_{EQ1} = (q + x1)^2 \text{ and } I_{EQ2} = (q - x2)^2$$

$$10\text{mA} - (q - x2)^2 = (q + x1)^2 = I_{EQ1}$$

$$\Delta U_{in} = |x1| + |x2| = \text{Voltage between the bases}$$

x1 and x2 are not identical. To show that here is a trivial calculation with the assumption $q = 4$ and $x1 = x2 = 0$ = no input signal:

$$I_{EQ1} = 16 = (4 + 0)^2; \quad I_{EQ2} = 16 = (4 - 0)^2 \quad \Rightarrow I_{EQ1} + I_{EQ2} = 32 = \text{constant current}$$

now with input signal $x1 = x2 = 1$:

$$I_{EQ1} = 25 = (4 + 1)^2; \quad I_{EQ2} = 9 = (4 - 1)^2 \quad \Rightarrow I_{EQ1} + I_{EQ2} = 34 \leftarrow \text{wrong, must be 32}$$

\Rightarrow in case $x1 = 1$, how big is $x2$?

$$I_{EQ1} = 25 = (4 + 1)^2 \quad I_{EQ2} = 32 - 25 = 7 = (4 - x2)^2 \Rightarrow x2 = 1,4, \Delta U_{in} = 1 + 1,4 = 2,4\text{V}$$

$$x1 = \sqrt{32 - (4 - x2)^2} - 4$$

$$\Delta U_{in} = x1 + x2 = \sqrt{32 - (4 - x2)^2} - 4 + x2$$

translated into the 10mA example:

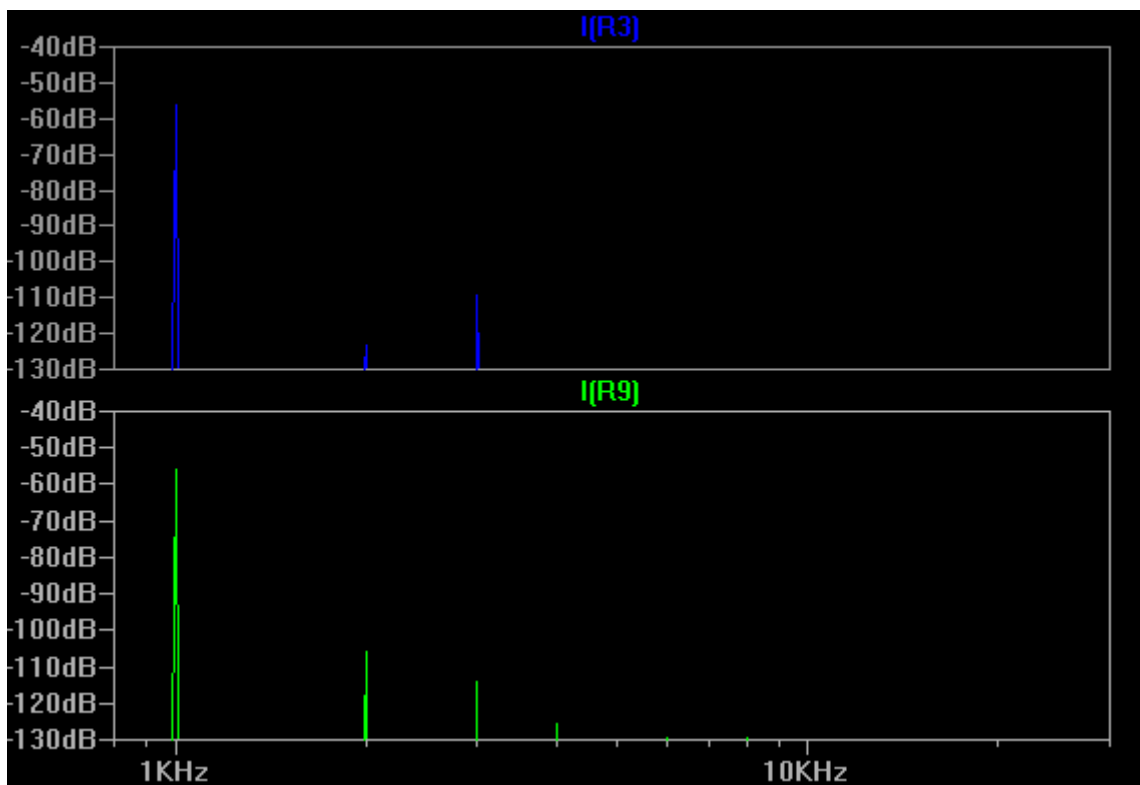
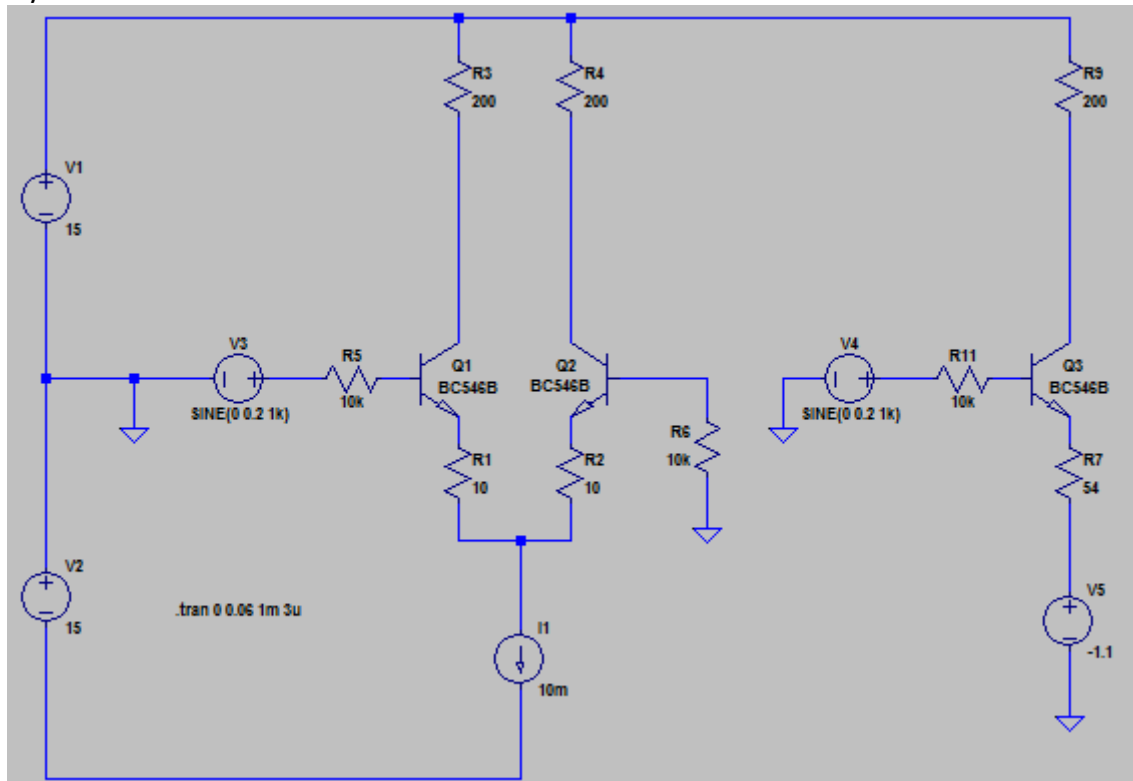
$$\Delta U_{in} = x2 + \sqrt{10\text{mA} - (q - x2)^2} - q \Rightarrow x2 = f(\Delta U_{in})$$

There are mathematical methods to solve that in approximation, but that would be too detailed here. The important conclusion is:

Differential stage type 1 and type 2 work and behave similar (but not identical) regarding distortion.

Below circuitry 8 the distortion distribution is shown. K2 is reduced and lower than k3 which is typical for the differential stage. To show that that pattern is not created by the transistors alone, the circuitry was copied and Q2 was removed. That resulted in the circuitry with Q3 where the surrounding parts were trimmed until the Q3 had the same collector current than Q1. The distortion pattern of Q3 is also shown. That proves that Q1 and Q2 really form a differential stage in the mathematical sense.

Circuitry 8:



g.) differential stage, type 3

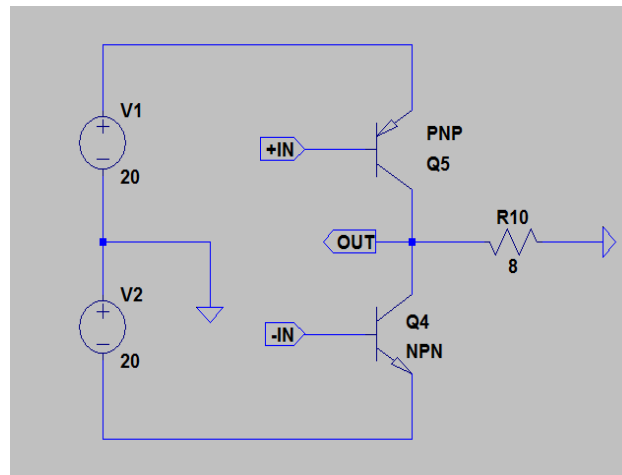
As shown above, a differential stage has 2 inputs, here called (+in) and (-in) and one output (out) or 2 outputs (+out) and (-out).

In a differential stage the signal at the input (-in) reduces the effect of the signal at the input (+in) to the output (out) of the differential stage, so that the output of the differential stage is 0, when

both inputs are driven with the same signal strength.

So here is another example, circuitry 8a. Two inputs, one output. To drive both inputs with the same signal strength, here a current has to be delivered into input -IN and at the same time a current of opposite polarity (but same amount or strength) has to be supplied to +IN. A load R10 connected to the output OUT gets the difference of the collector currents of the 2 transistors. Hence this is a differential stage. In chapter "G. Push/Pull stages" this and other type 3 differential stages are examined. As expected, also type 3 differential stages cancel even order harmonics as shown above.

Circuitry 8a:



h.) summing stage

No simple (only a complex) example available yet.

F. Comparison of different loads

In the chapter "Preferred transistor transfer characteristic" this very general question is asked (and answered) in the most basic way: The transistor should have a very smooth transfer curve and no changed in the direction of the steepness. That answer is true without naming the type of a transistor or how the load of a transistor should look like.

Here a look at the different (possible) loads for a transistor is taken.

Resistor:

The most simple load is a resistor. This is R7 and is shown in circuitry 9. R7 is the load resistor for Q3 and R9 is the output resistor (of cause also a load resistor). R7 sets the quiescent current for Q3 and delivers the current for the positive output swing on the output resistor. Q3 has to work hard when it pulls the output to negative output swing because it delivers not only the output current into R9 and the quiescent current through R7 but also an increased current through R7 because its voltage is increased by a negative output swing. Not very effective and the transistor has to work through a big area of its transfer curves, which creates lots of distortion because its transfer curve is the less smooth as the transistor has to work in a larger area of this transfer curve.

Constant current source:

Obviously this situation can be improved when that simple load resistor is changed to a constant current source, as implemented as I1 and Q2.

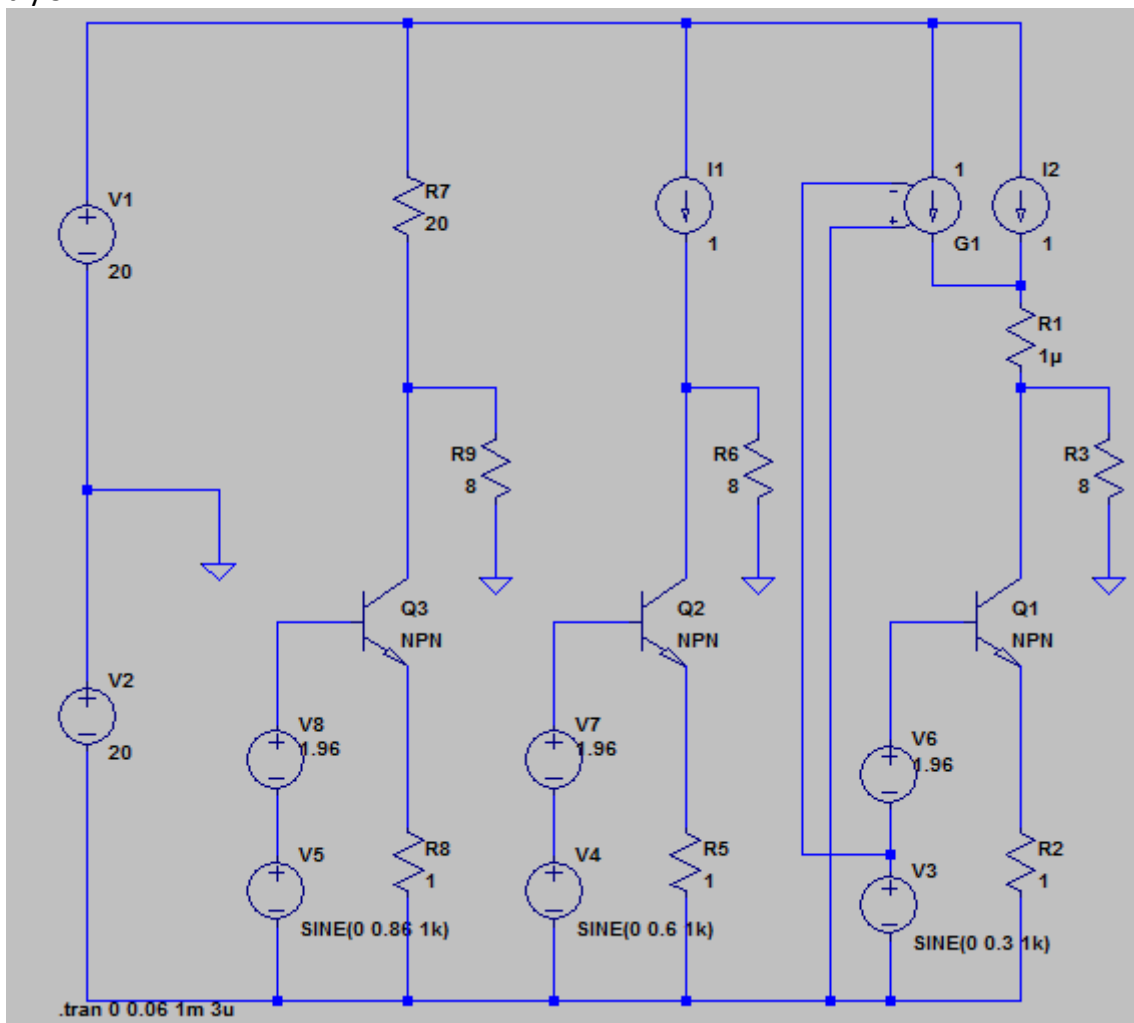
All the above mentioned is also true here except that the transistor delivers only the output current into R9 and the constant quiescent current I7 – there is no increased current through a load resistor, thus the transistor has to work less hard and the distortion is reduced.

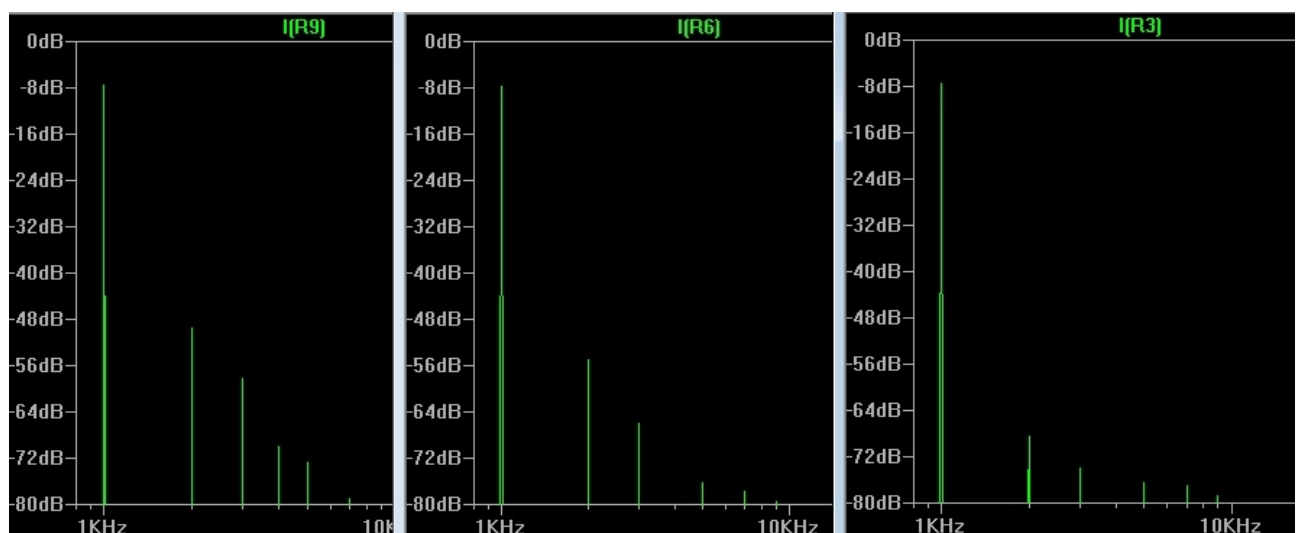
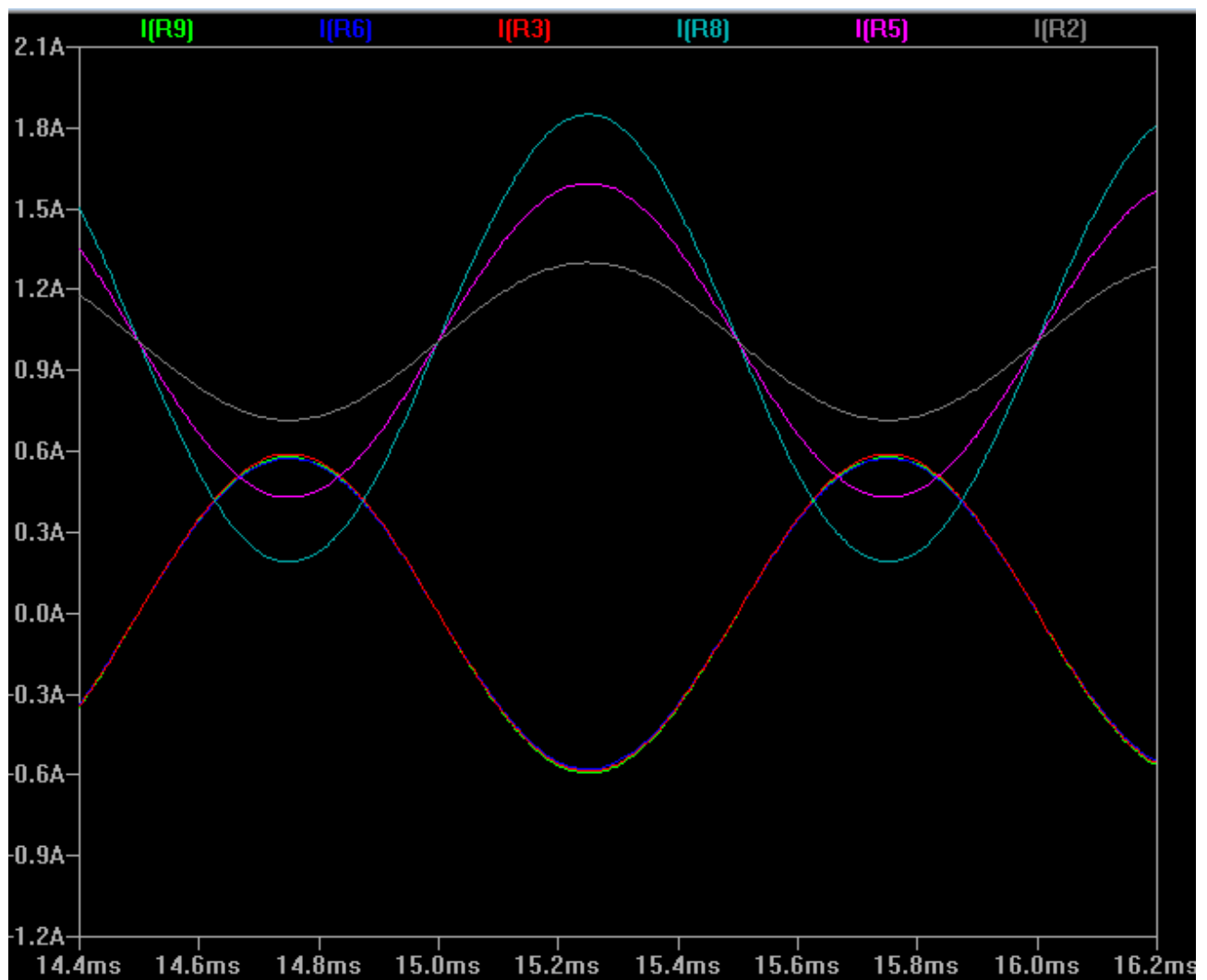
Modulated current source:

The next step to increase efficiency is to reduce the current of the current source on a negative output swing. The transistor would have to deliver the output current into the load and a (heavily) reduced quiescent current into the constant current source. The distortion will hence be reduced even more. This modulated current source is I2 and G1, the transistor is Q1.

In the diagram below the identical output currents are shown ($I(R3)$, $I(R6)$ and $I(R9)$) and the load currents of the three transistors ($I(R8)$, $I(R5)$ and $I(R2)$): $I(R8)$ (= current through Q3) has the biggest swing, $I(R5)$ (= current through Q2) is medium and $I(R2)$ (= current through Q1) has got the lowest swing. Below that the distortion patterns are shown. They reflect the amount of the current swing: Q3 has the highest current swing and distorts the most, Q2 is medium and Q1 has the smallest swing and the smallest distortion.

Circuitry 9:



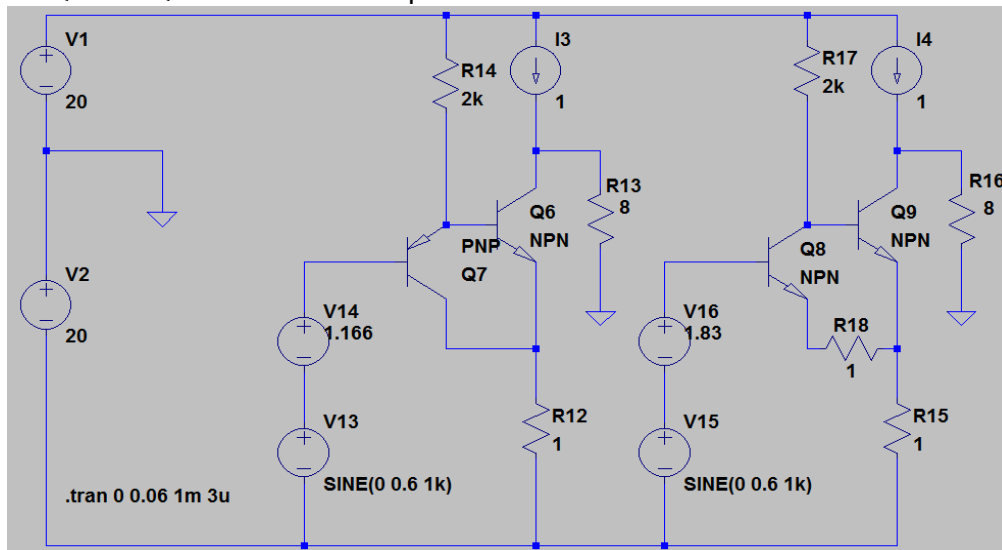


Voltage clamping

Circuitries that keep the voltage over the transistor constant (like cascodes, folded cascodes, super

pairs,...) are not really a kind of a load for a transistor but influence its operation in similar strong way. Cascodes are described in: <https://passlabs.com/articles/cascode-amp-design>

A super pair is shown below with Q6 and Q7. The operating collector emitter voltage of Q7 is held nearly constant at 0.6V by base emitter voltage of Q6. With that basic idea I quickly created the circuitry with Q8 and Q9 as another example.



Constant power

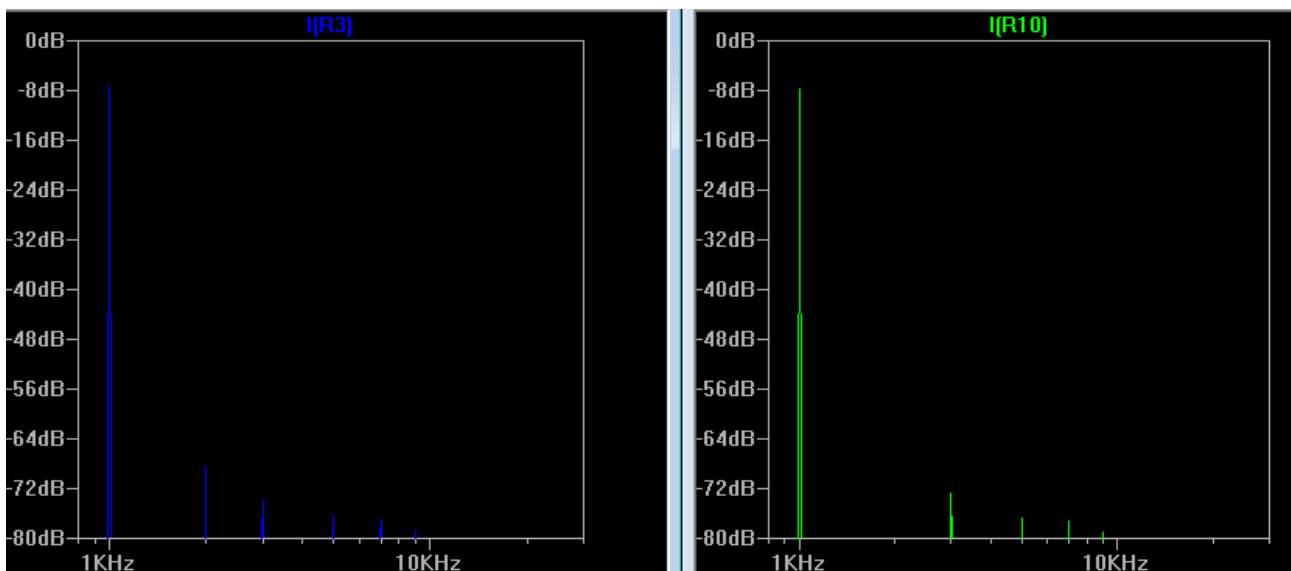
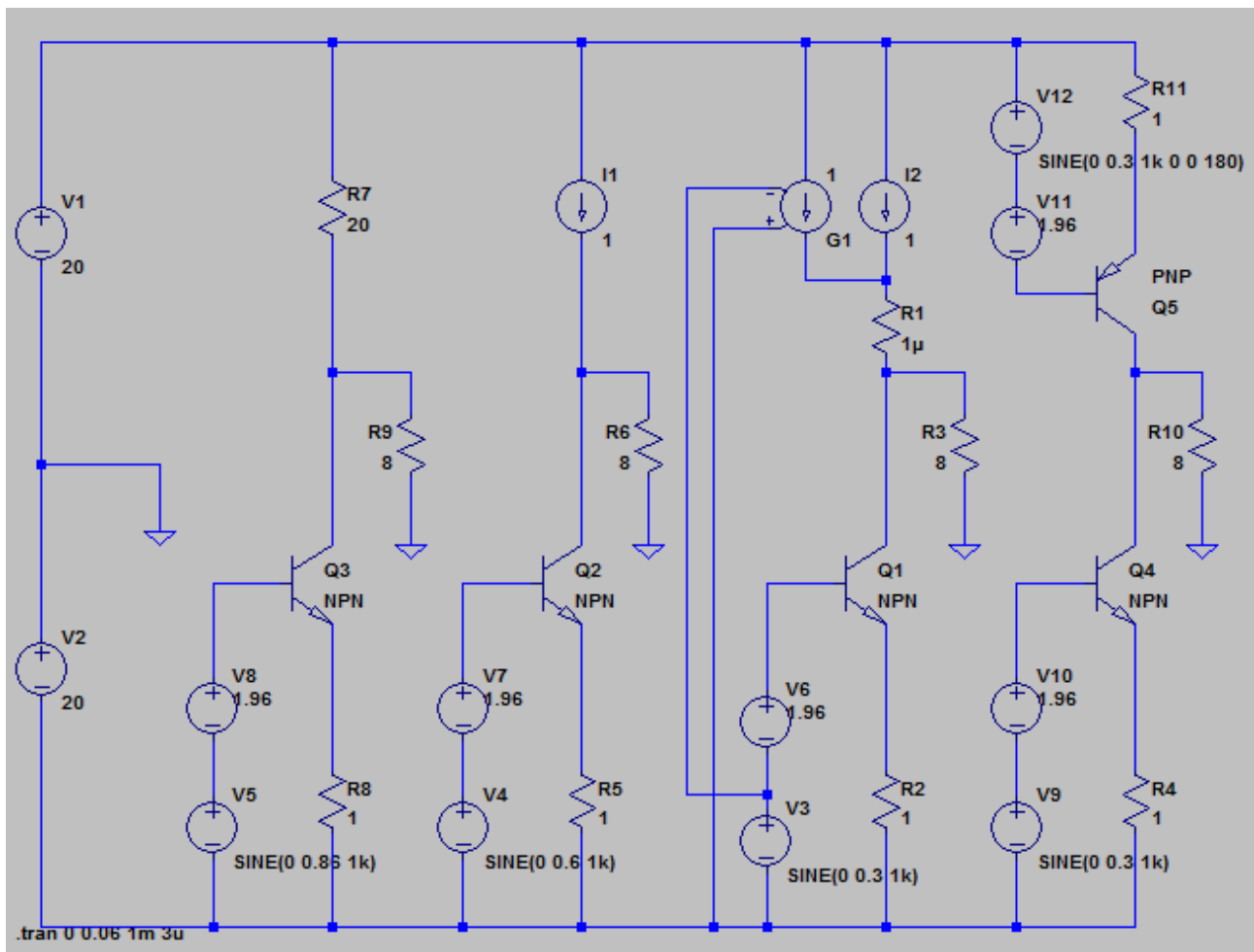
Another influence of the distortion pattern is the change of their operating point caused by a temperature change after driving the amplifier with a signal. This is called memory distortion and mentioned before.

G. Push/Pull stages

See also chapter “g.) differential stage, type 3”.

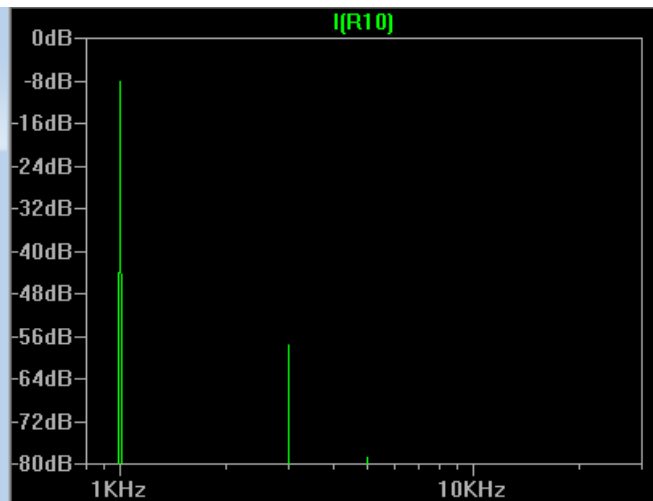
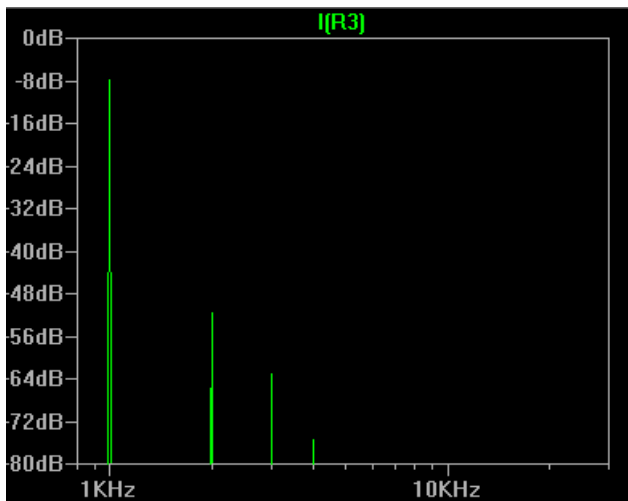
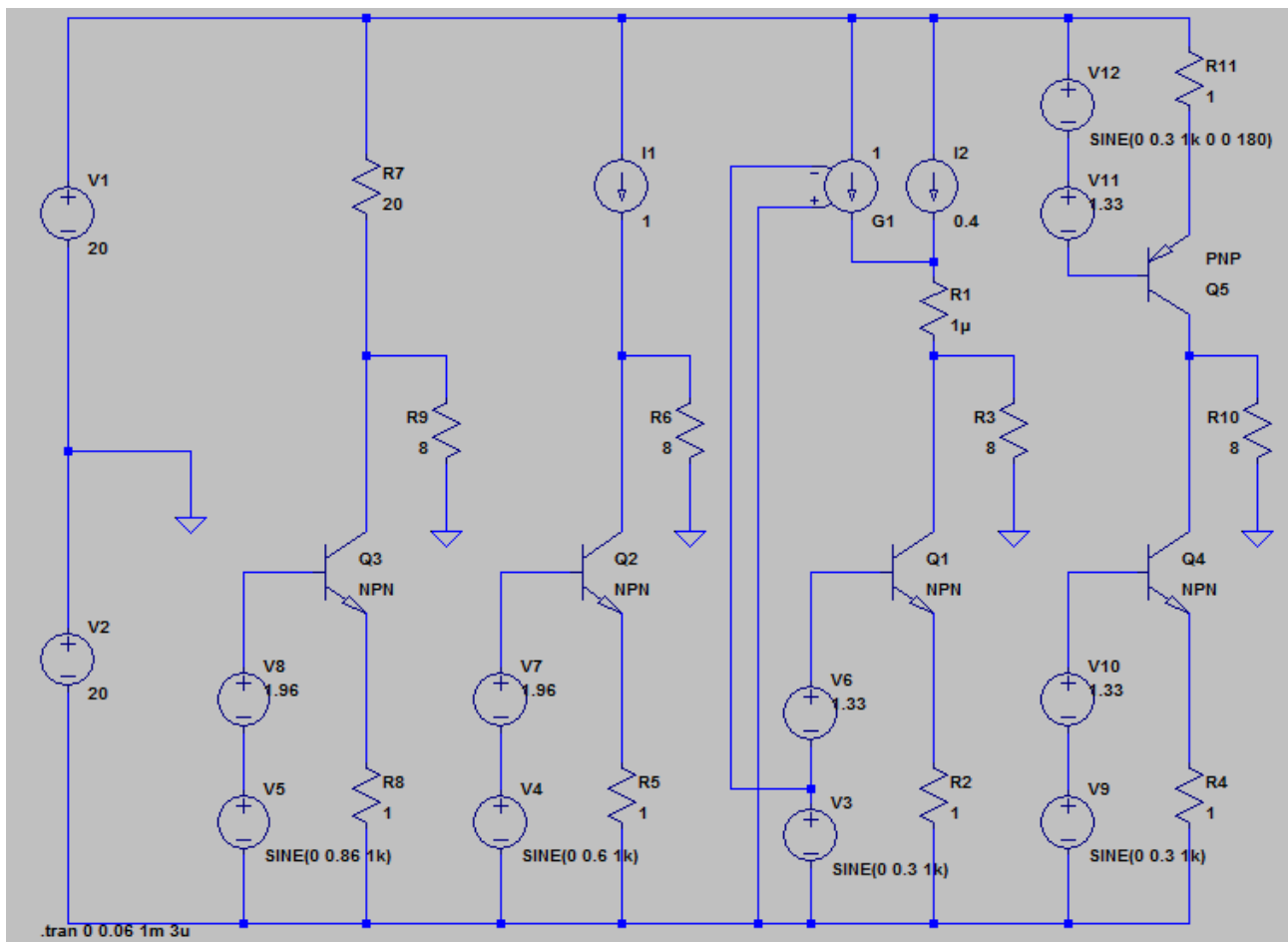
The modulated current source acts together with Q1 as a push/pull stage. But there is a difference to the standard push/pull stage. In circuitry 10 this is added with Q4 and Q5 and the parts around them are set to get the same output swing as G1,I2 with Q1. Their distortion patterns are shown below. They massively differ in the amount of k2. G1,I2 with Q1 create plenty of k2, but Q4 and Q5 create none! The reason for that is the unbalance or low similarity in the transfer function of G1,I2 on the one hand and Q1 on the other (In this simulation I2 and G1 are ideal, flawless current sources with perfect linearity, but Q1 is a non linear device). In contrast to that Q4 and Q5 are similar (both non linear devices but both have the same non linearities) and the calculation in chapter “B. a.) differential stage” is true: differential stages cancel even order harmonics.

Circuitry 10:



Because the distortion pattern really looked bad, I did some tweaking:

Reducing k5,k7,k9 by changing the quiescent current from 1A to 0,4A for Q1 and Q4 (reducing or increasing V1 and V2 does not improve the distortion pattern but worsens it), circuitry 11:

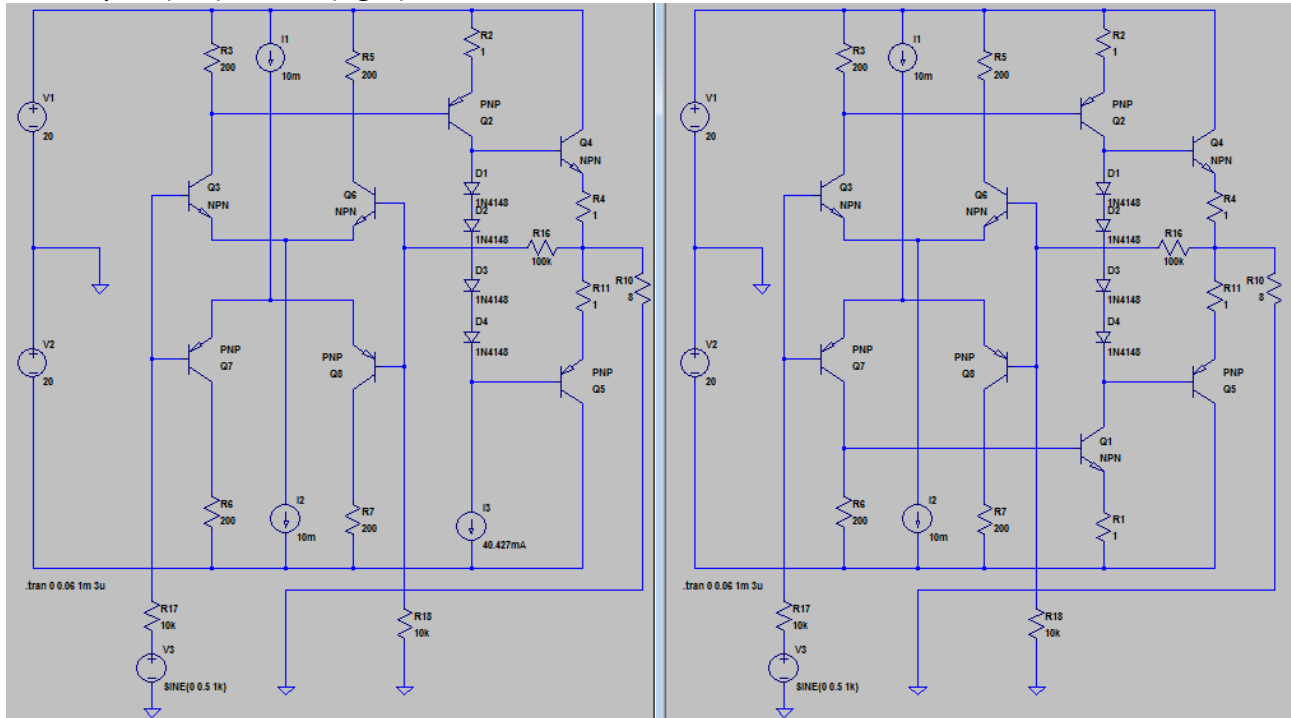


H. Complete Amplifiers

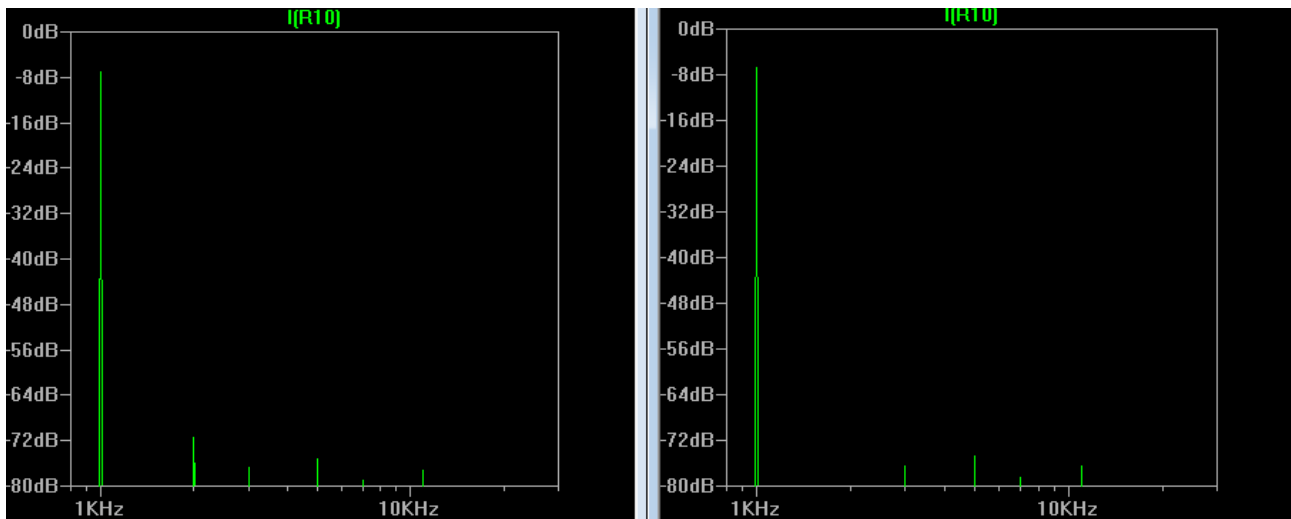
a.) Dual differential input stage with single ended or push pull driver and push pull output stage

Now a look into complete amplifiers of common design. With the information given above, it should be easy to guess their performance.

Circuitry 12 (left) and 13 (right):



They are identical except for the lower part of the driver stage. In the left circuitry it is the constant current source I3 and in the right circuitry it is transistor Q1 which forms together with Q2 a push and pull stage. In the left circuitry I3 is a single ended load for Q2, so we can expect that the driver stage of left circuitry will create k2 (and k3) and the right circuitry k2 will be cancelled if no other stage creates k2. The other stages are the differential npn input stage Q3 and Q6 (cancels k2), the differential pnp input stage Q7 and Q8 (cancels k2) and the differential output stage Q4 and Q5 (also cancels k2). As a result, we can expect that in the distortion pattern of the right circuitry we will find no k2 but k3 (and probably more odd order harmonics like k5, k7, ...). In the circuitry on the left only the driver stage is single ended, so we can expect to see k2, k3 (and probably more odd and even order harmonics like k4, k5, k6, k7, ...) Here are the results (left spectrum corresponds to circuitry 12, the right one to number 13):



As shown before, we could add some bias to reduce the higher order harmonics. That is not repeated here.

b.) negative feedback

Negative feedback reduces the low order distortions more than the the high order distortions. (Note: Eventually when too much feedback is applied the high order distortions may even rise. One reason for that might be: Before clipping high order distortions will rise stronger than low order distortions. So when too much feedback is applied and the higher order harmonics rise it is an indication that one of the stages of the amplifier is driven too hard and it is close to clipping. Especially when the slowest stage (in most cases this is the driver stage) is driven hard by the preceding stage (e.g. the input stage) because the the output signal does not follow the input signal quick enough, this overdrive might happen. But this slew rate caused distortion is not the topic of this article.)

Circuitry 12 with different amount of feedback. All input levels adjusted to get the same output level. From left to right the amount of feedback is increased but only the lower order harmonics are reduced. So only the disturbing higher order distortions remain.

