Evolve TLB – Power amplifier with Trans-Linear Bias

By Shinichi-Kamijo Source: http://www.ne.jp/asahi/evo/amp/TLB/memo0.htm

Table of contents

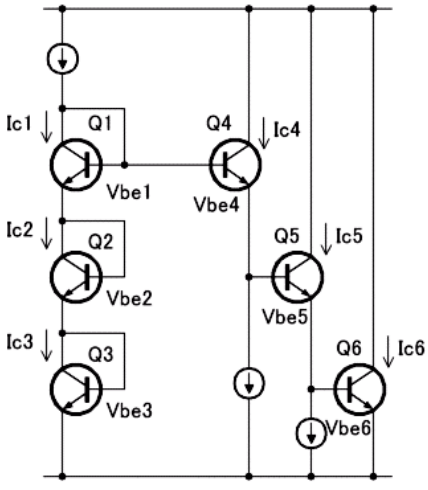
This method controls the bias voltage so that the product of the currents of the output elements of the push-pull circuit is constant. Therefore, it has the features of no temperature compensation, no thermal runaway, and no cutoff.

The transformer linear circuit is the bias voltage generation circuit used in the amplifier that controls the idling current in the November 2006 issue of Radio Technology to eliminate the emitter resistance.
The theory that switching distortion does not occur because the complementary push-pull circuit without emitter resistance does not cut off is also sensational.

I also tried an emitter resistanceless amplifier before. At that time, the method of stabilizing the idling current was to remove the output current component and detect the idling current by adding the collector currents on the plus side I and the minus side of the output stage transistor. This method was incomplete because of the non-linearity of the transistor, the detected value increased and the idling current decreased as the output increased even in class A operation .

What is Translinear *?*

For the trans-linear circuit, refer to the October 2004 issue of Transistor Technology, pages 241-245.
A translinear circuit is a circuit that utilizes the exponential characteristics of a bipolar transistor.
Translinear means transconductance linear with current , and was invented by Mr. Barrie Gilbert, who is famous for Gilbert cells.
According to the translinear principle, the products of Ic of circuits with the same sum of Vbe are equal as shown in the figure below. From this principle, it is applied to various circuits such as multiplication and division.



Vbe1+Vbe2+Vbe3=Vbe4+Vbe5+Vbe6
Ic1・Ic2・Ic3=Ic4・Ic5・Ic6

Figure 1

An example of a power amplifier circuit with a **transformer linear bias**

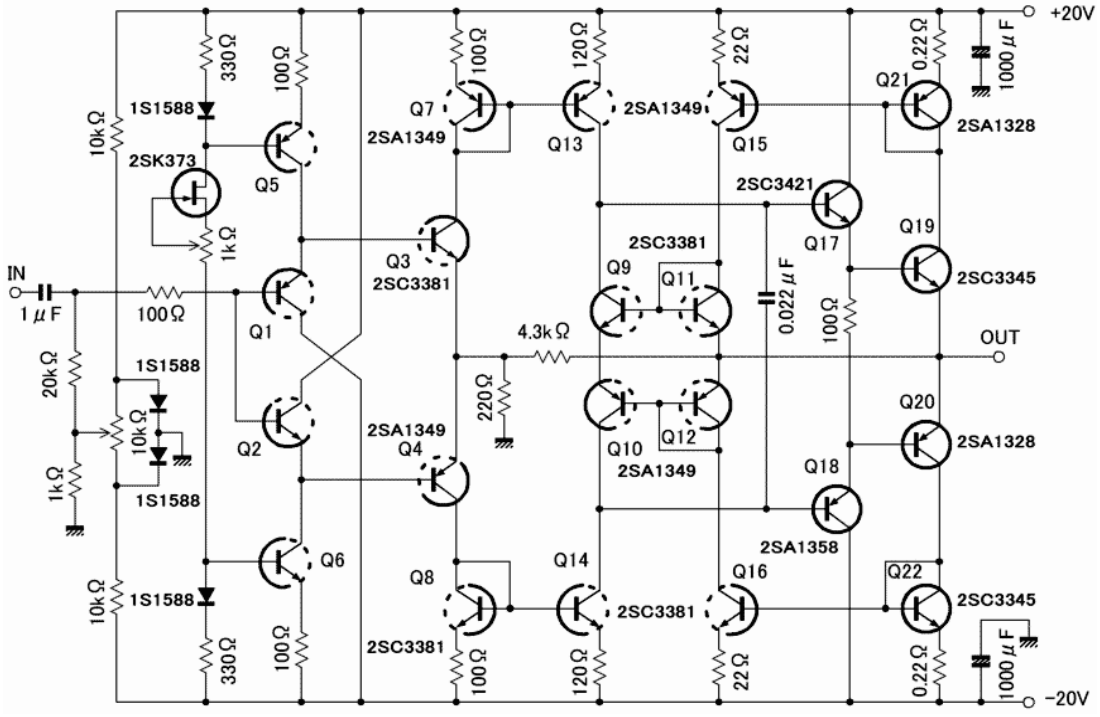


Figure 2

The current mirror is also a type of transformer linear circuit, but the transformer linear circuit that calculates the product of the collector currents of the output transistors required to determine the bias voltage is the part of Q9, Q10, Q11, and Q12.
The current mirror circuit of Q21 (Q22) and Q15 (Q16) gives a current proportional to the collector current of the output stage transistor Q19 (Q20) to Q11 (Q12).
Then, according to the translinear principle, the product of the collector currents of Q11 and Q12 and the product of the collector currents of Q9 and Q10 are equal, so the collector currents of Q9 and Q10 are the same value, so the collector current of Q9 (Q10) is , It is the value obtained by opening (rooting) the product of the collector currents of Q11 and Q12.
Q17 (Q18) → Q19 (Q20) → Q21 (Q22) → Q15 (Q16) → Q11 (Q12) → Q9 (Q10) so that the collector current of Q9 (Q10) and the collector current of Q13 (Q14) match. It is controlled by the NFB loop of.
The idling current of Q19 (Q20) is determined by the current ratio of the collector current of Q13 (Q14) and the current mirror circuit of Q21 (Q22) and Q15 (Q16).

(photo1)[removed]

Simulation of **transformer linear bias circuit**

Emitter resistance to **1** output transistor

The upper side of the simulation circuit in the figure below has no emitter resistance of the output transistor, and the lower side has a 1Ω emitter resistance.
XX1 to XX4 are ideal current mirror circuits called current control current sources, and their coefficients are set to 0.01, so if the output transistor current is 1A, 10mA will be given to the translinear bias circuit.
Since the Iref of the transformer linear bias circuit is set to 2mA, the idling current of the output transistor is 2mA / 0.01 = 0.2A if the error due to the base current is ignored.
The power supply voltage is positive and negative 20V, and the result of DC sweeping the input signal voltage V1 from -20V to + 20V is shown on the right.

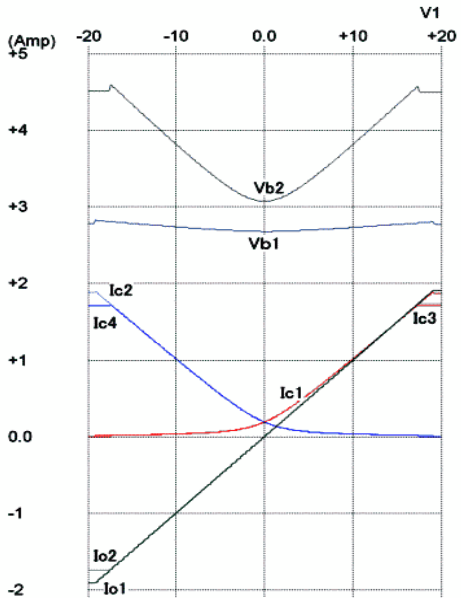


Fig. 3. Fig. 4

Since the transmission characteristic of the output transistor is an exponential characteristic, the bias voltage Vb1 of the output stage does not change significantly even if the output current changes.
On the other hand, the bias voltage Vb2 on the side where the emitter resistor is inserted in the output transistor changes significantly. This is natural because the gm of the output stage is reduced by the emitter resistance.
However, the collector current of the output transistor does not cut off in the same curve regardless of the presence of the emitter resistor.
From the above, it can be seen that the bias voltage is controlled so that the product of the collector currents of the output transistors becomes constant by the action of the transformer linear circuit.
From this, it can be expected that the same result will be obtained no matter what element is used for the output.

2 Emitter resistance in a transformer linear circuit

If you put an emitter resistor in the transistor of the transformer linear circuit as shown in the figure below, the result is as shown on the right.

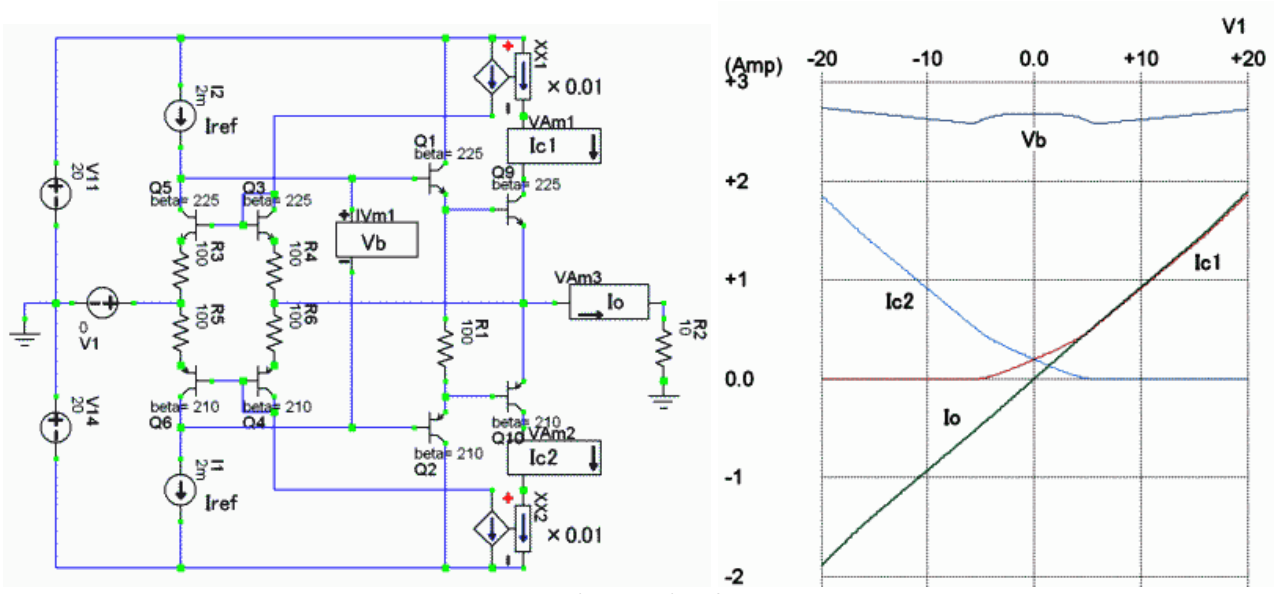
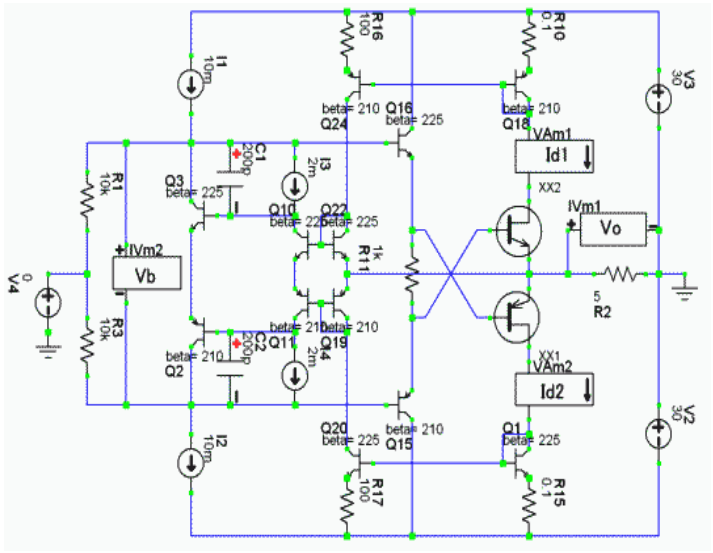


Fig. 5. Fig. 6

Application to SIT

I thought about the circuit when SIT is used for the output element.
The waveform on the right shows the output voltage Vo at the 5Ω load resistor, the drain currents Id1 and Id2 of the SIT, and the bias voltage Vb when the input V4 is a 20Vp-p 1kHz sine wave.



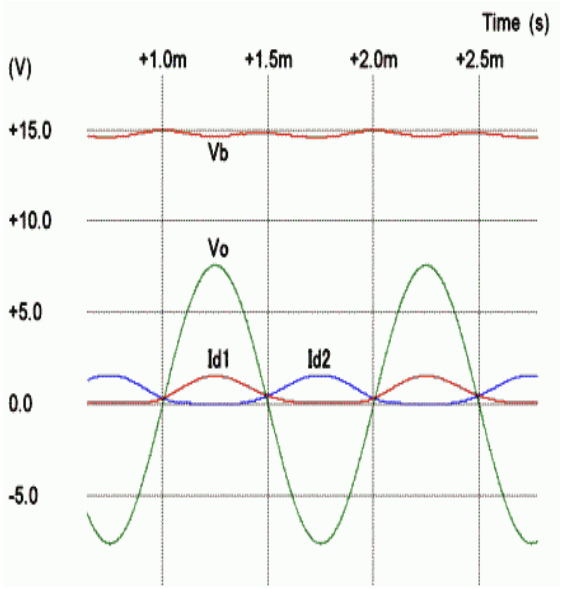
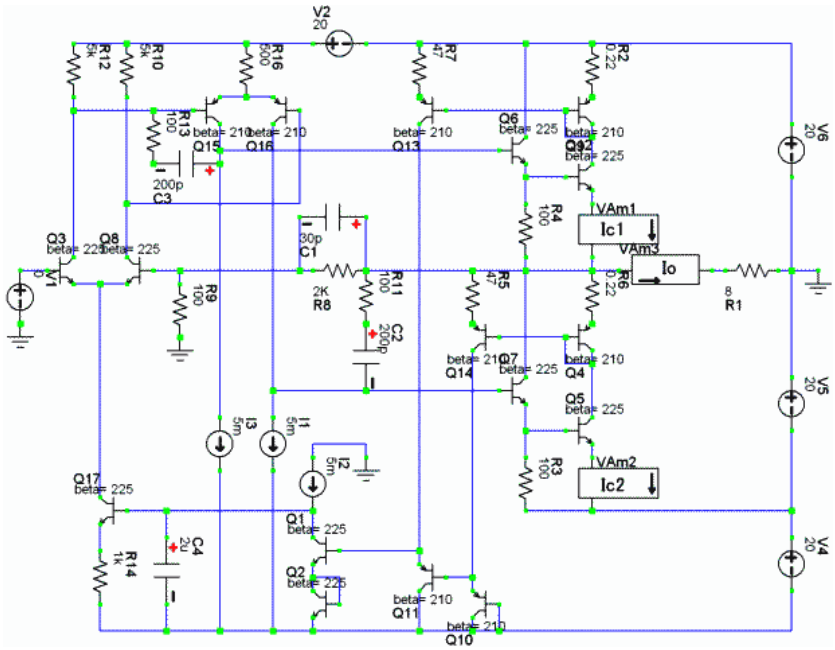


Fig. 7. Fig. 8.

Application to **Kaneda type perfectly symmetrical wind circuit**

The collector current of the output transistor is detected by the current mirror, multiplied by Q10 and Q11, flattened by Q1 and Q2, and the constant current circuit on the emitter side of the first stage differential circuit is controlled so that it matches the 5mA of I2.

The waveform on the right shows the output current and output transistor current at an 8Ω load resistance when the input V1 is a 1Vp-p 1kHz sine wave.



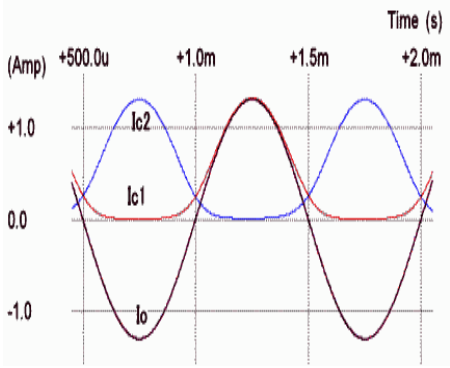


Fig. 9. Fig. 10.

It seems that it can be used for CSPP circuits and ordinary push-pull circuits such as tube amps in this way.

Application to **BTL circuit**

Theoretically, a circuit with zero output resistance and zero distortion.

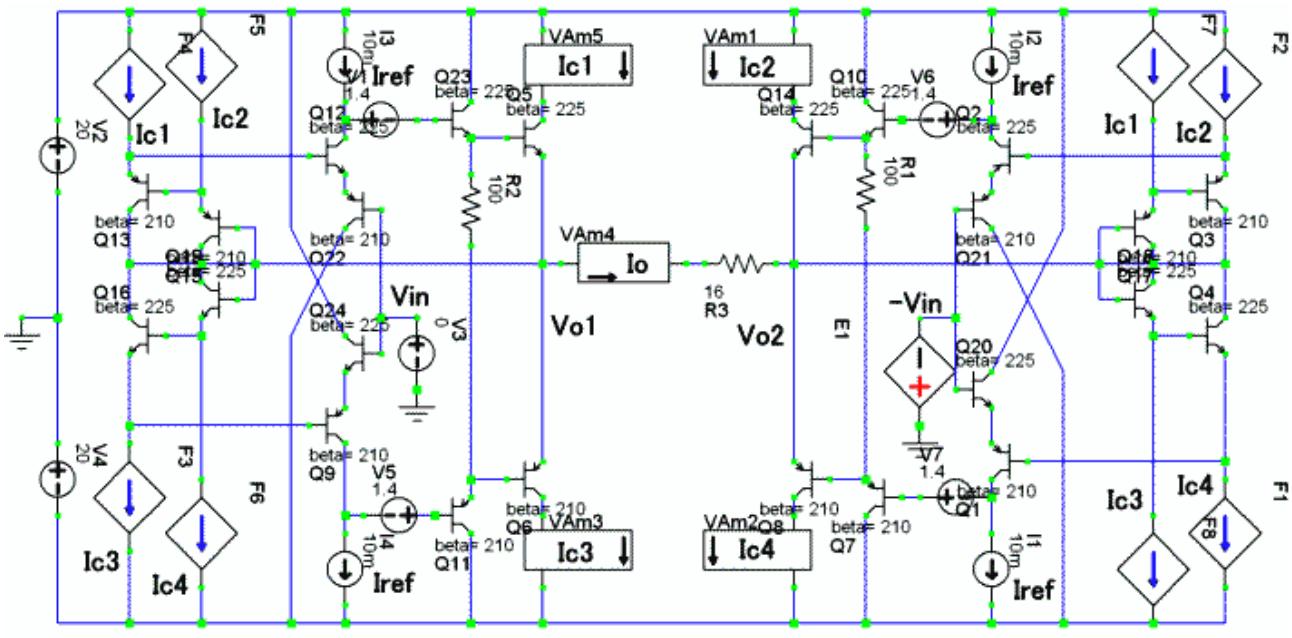


Fig. 11

This connection crosses the left and right collector currents to the left and right bias circuits and gives them as control currents, but since the left (right) bias circuit can only control the left (right) idling current, the idling currents are unclear on the left and right. It becomes a balance and it is a failure.
It may be a misunderstanding that I thought.

In the part where Ic1 and Ic2 are multiplied in the figure below, the base current Ib1 of Q1 is added to Ic2 and given to Q2, so Ic3 increases by that amount. That itself is cancelled by the point-symmetrical BTL circuit in the above figure and does not affect the output.

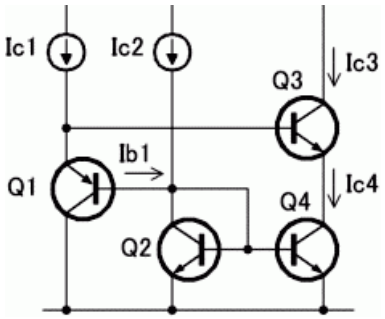


Fig. 12

Assuming that Ic2 is controlled by the loop of this bias circuit and Ic1 is not controlled, Ib1 of Ic1 / hfe is included in Q2 even if Ic2 is controlled properly when Ic1> Ic2. Then, Ic3Ic4 = Ic1 (Ic2 + Ic1 / hfe). There is no problem if Ic1 / hfe is negligibly small compared to Ic2, but otherwise Ic2 is controlled unreasonably less and the product of Ic1 and Ic2 is controlled to be constant, so Ic2 with respect to it increases. I noticed that the collector current of the BTL output is biased to the left and right.

The figure below is a useless example of bias.

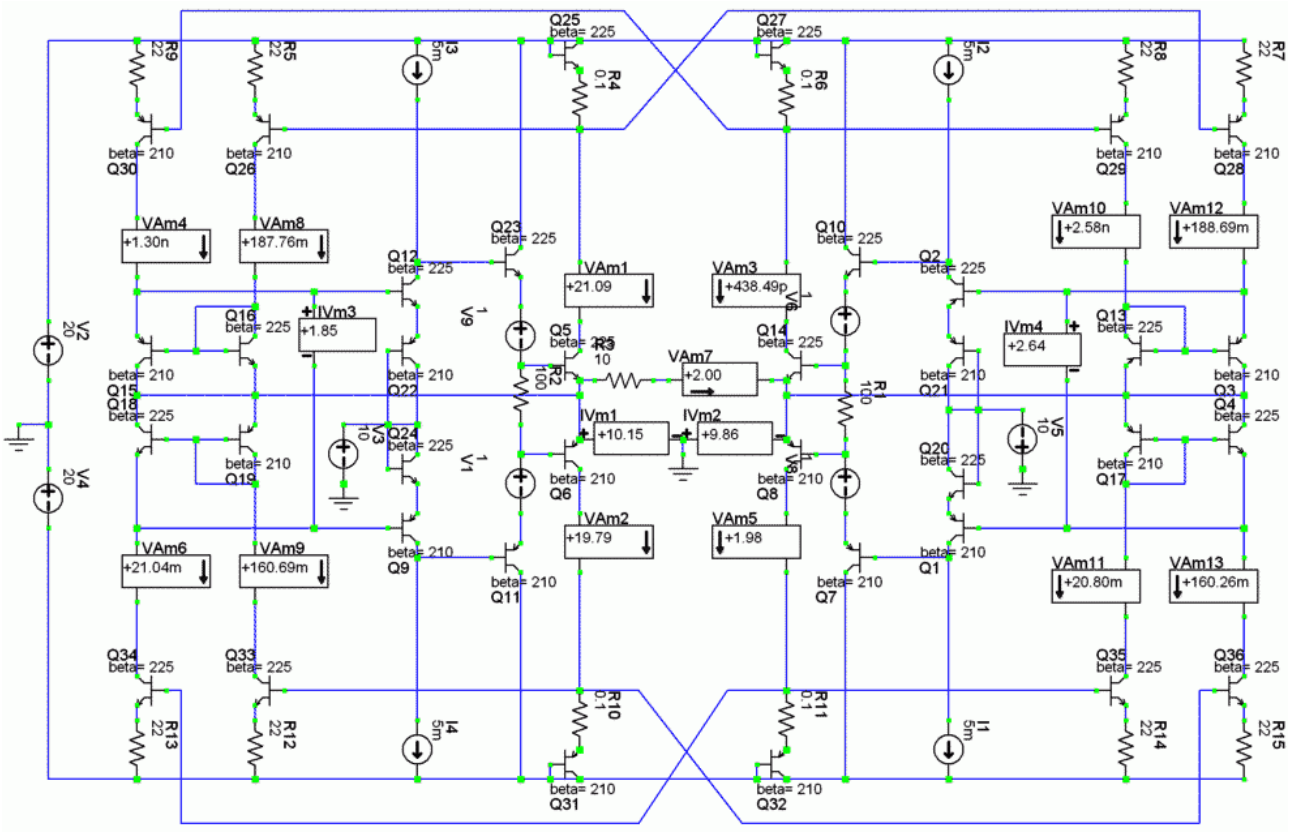


Fig. 13

If the connection is correct based on the cause of the failure, it will work properly as shown in the figure below.

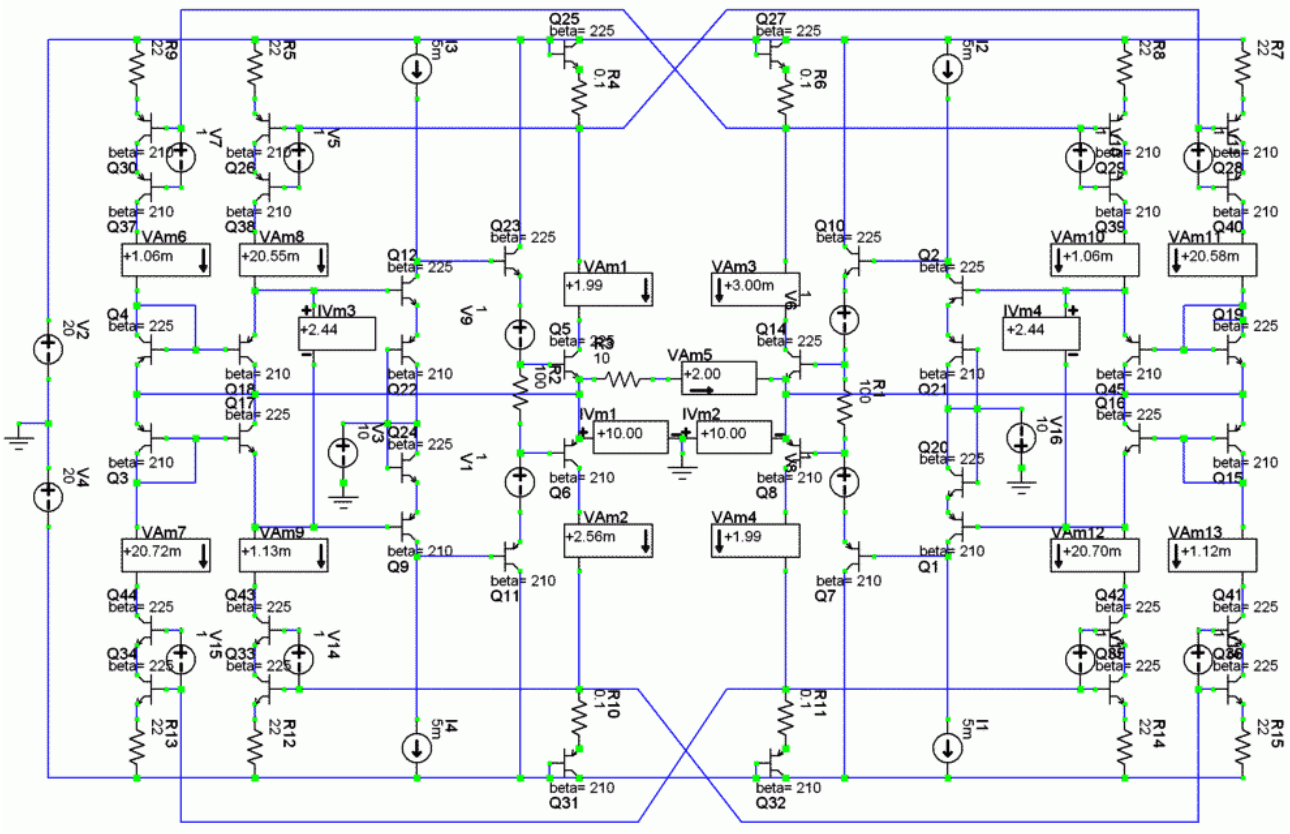


Fig. 14

The current mirror for current detection is cascoded to keep Vce constant. Still, there is a slight current imbalance.

The experiment failed. (Photo 2)[removed]

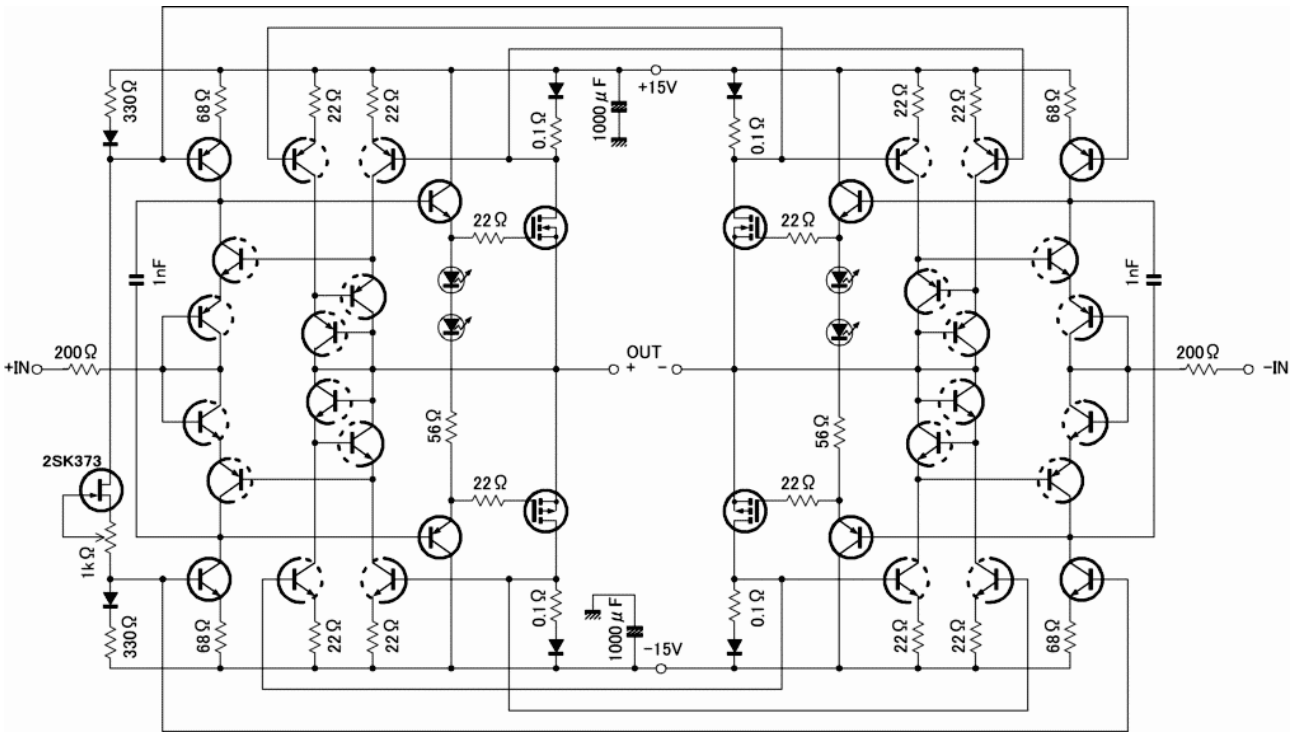


Fig. 15

The idling currents on the left and right of the bridge are not balanced and are biased like a flip-flop circuit. Added a circuit to balance the left and right of the bridge.

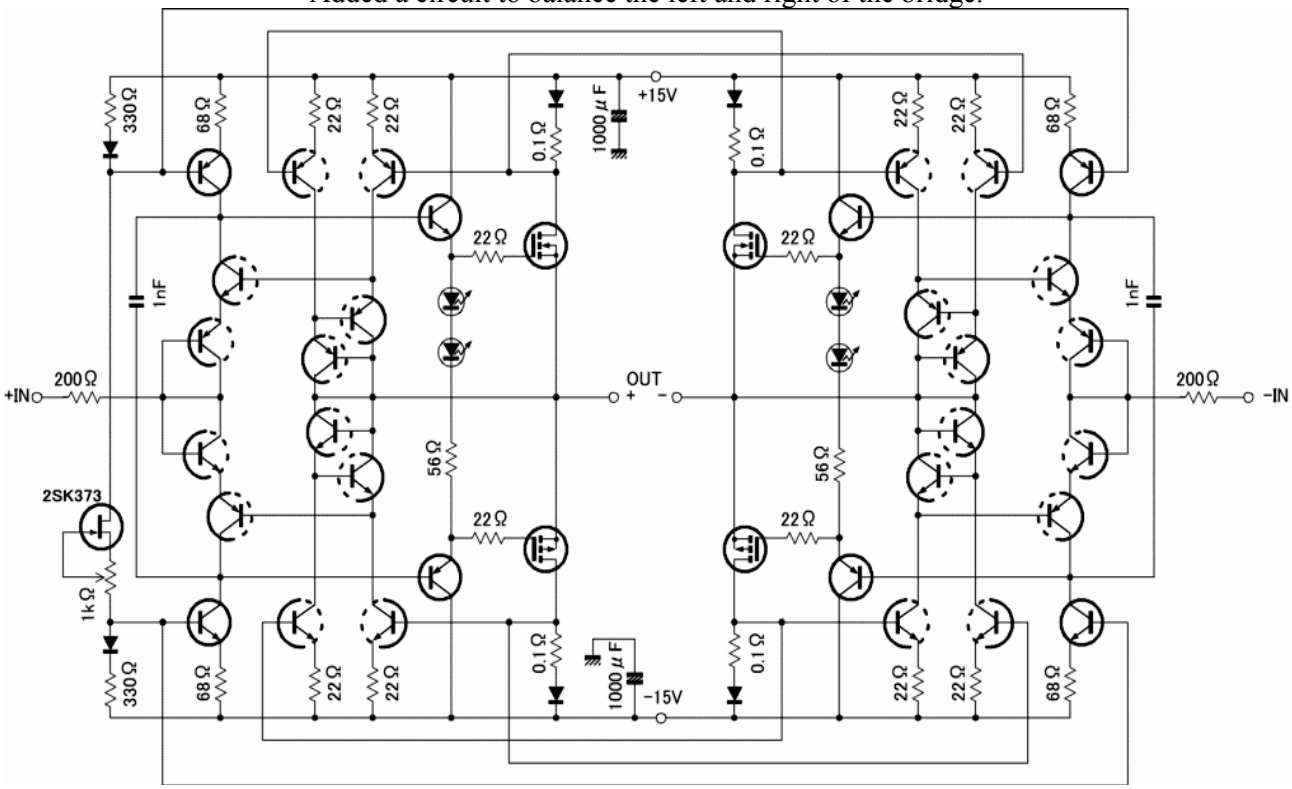


Fig. 16

The reference current on the right side of the bridge was controlled so that the left and right idling currents were balanced, but in this circuit, the reference current on the right side of the bridge becomes unbalanced at the top and bottom, so the -OUT waveform is severely distorted.

Aside from that countermeasure, since there is a current mirror circuit on the power supply side of the output stage, if the voltage required for the operation of the current mirror circuit is pressed by the amplitude of the signal voltage, it becomes unstable, so the amplitude of the signal voltage must be limited. It is a waste of power that is not output.

This bridge method gives up once and restarts once a good idea comes up.

Circuit with **distortion rate = 0 and output impedance = 0**

Radio Technology I thought about applying it to the above-mentioned BTL circuit as a means to embody the method shown in Fig. 2 on page 138 of the December 2006 issue , but since that was just a failure, I thought about another means. .

Linear Technology LT1166 inserts a resistor on the emitter side of the output transistor and detects the current with a differential amplifier. I got this idea and tried to draw the circuit in the figure below.

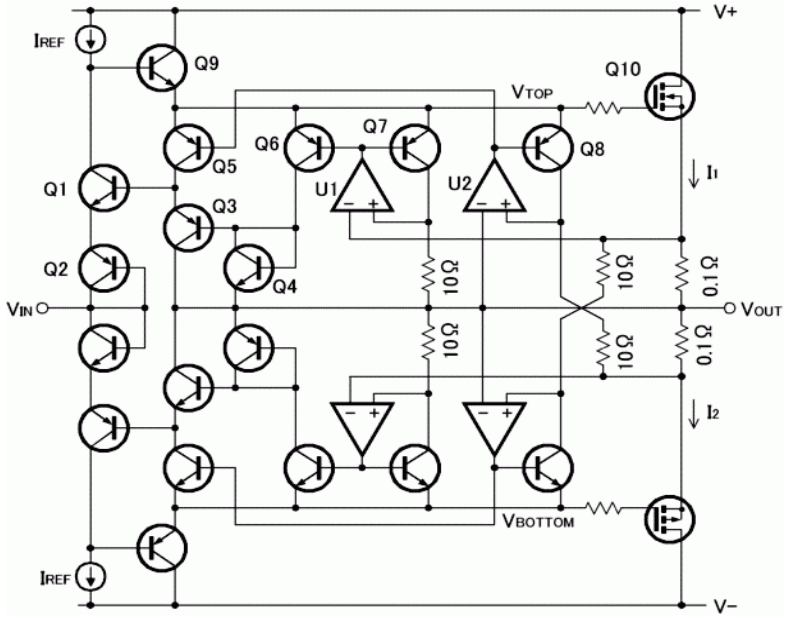


Fig. 17

Since U1 sets the collector current of Q7 to I1 / 100, the collector current of Q7 and Q6 of the current mirror is also I1 / 100.

Since U2 sets the collector current of Q8 to I2 / 100, the collector current of Q8 and Q5 of the current mirror is also I2 / 100.

The collector current of Q5 is given to Q3 of the transformer linear circuit of Q1 to Q4, and the collector current of Q6 is given to Q4.

If the lower side operates in the same way, the bias of Q9 and Q10 is controlled so that the Q1 collector current and Iref match, and √I1 □ I2 = 100Iref.

According to the translinear principle, the sum of Vbe of Q1 and Q2 is equal to the sum of Vbe of Q3 and Q4, so Vin = Vout.

However, since this depends on the accuracy of the pair characteristics of the transistors, it seems difficult to actually achieve decent performance with this principle alone, so semiconductor manufacturers are a showcase of their technological capabilities.

Today (November 24, 2006) I realized that if I monitor the currents of Q3 and Q4 of the above circuit with U1 and U2, I can omit Q7 and Q8, so I redrawn the circuit.

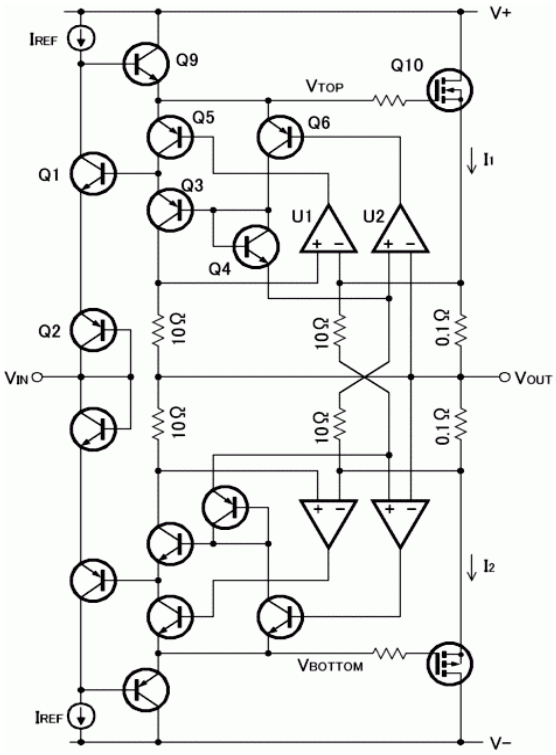


Fig. 18

The emitter of Q4 is kept at the same potential as Vout by U2.
The upper limit of the voltage generated in the current detection resistor in this circuit must be lower than the sum of Vbe of Q3 and Q4 minus the saturation voltage between collector and emitter of Q3.

Today (November 25, 2006) I came up with another one, so I redrawn it.
Since the currents of Q3 and Q4 are symmetrically equal on the upper side and the lower side, they are cross-connected.

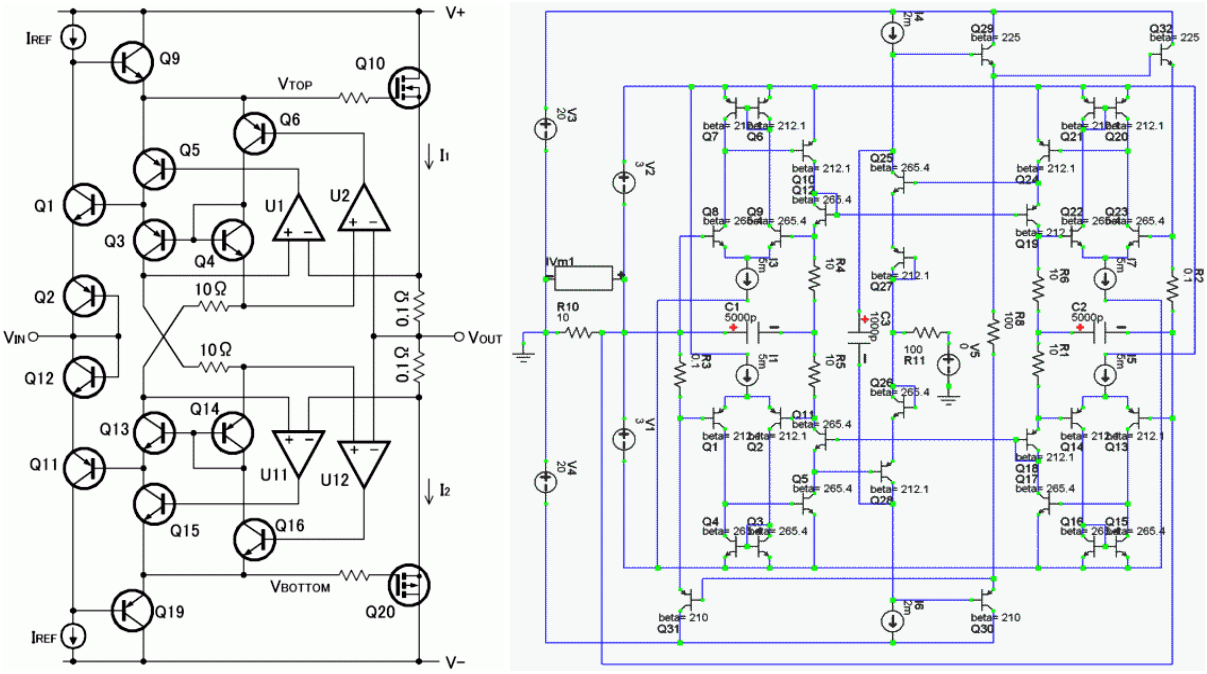


Fig. 19. Fig. 20 Sim1

I think it's quite sophisticated, but in order to see if it's worth making such a troublesome circuit, compare the distortion factor with the circuit in the figure below, omitting the U1 and U11 system parts in the figure above. Saw.

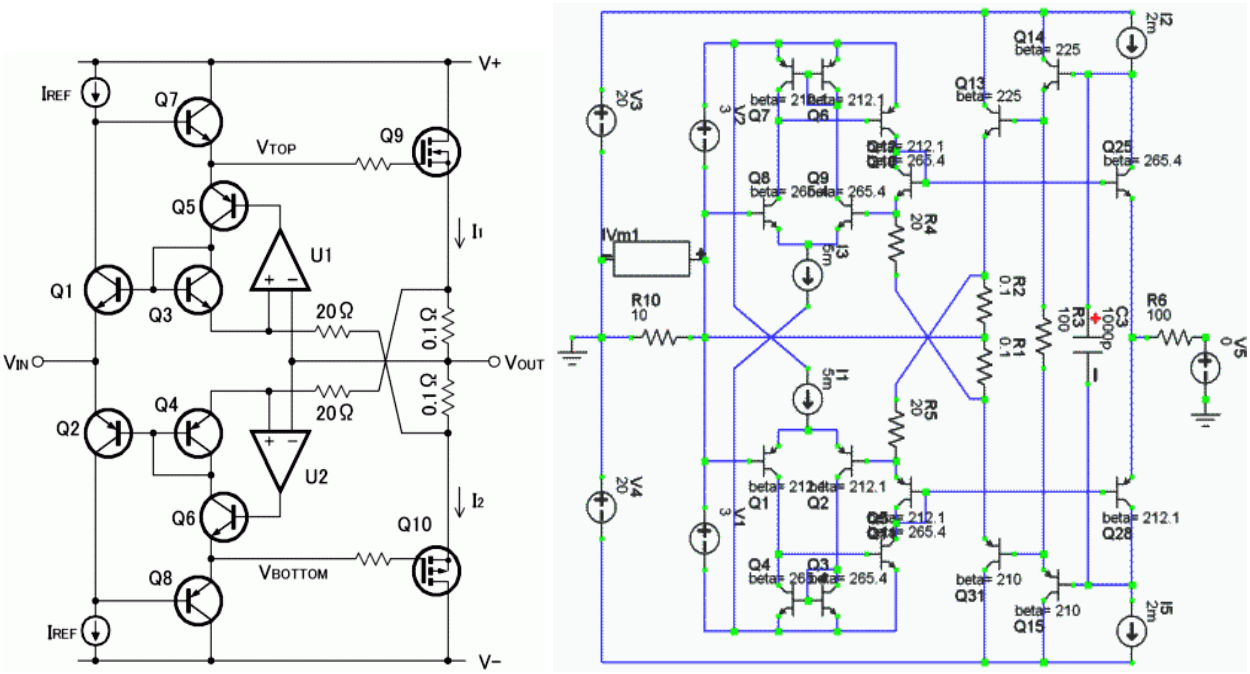


Fig. 21 Fig. 22 Sim2

The table below shows the amplitude data sampled by Fourier-analyzing the output voltage with a load resistance of 10Ω by inputting a sine wave of 1kHz and 20Vp-p. Replace the unit u with μ

Table 1

FREQ (Hz)	Sim1 norm_mag	Sim2 norm_mag
0.0	0.0	0.0
+ 1.00k	+1.00	+1.00
+ 2.00k	+ 4.54u	+ 23.54u
+ 3.00k	+ 19.69u	+ 126.12u
+ 4.00k	+ 1.62u	+ 1.23u
+ 5.00k	+ 365.79n	+ 11.27u
+ 6.00k	+ 134.94n	+ 349.90n
+ 7.00k	+ 95.74n	+ 1.54u
+ 8.00k	+ 141.05n	+ 73.65n
+ 9.00k	+ 133.18n	+ 239.79n

In both circuits, the largest third harmonic, Sim1 was about 1/6, and the odd-numbered components were improved to a low level overall, confirming that it was effective.

Today (2006/12/13) The circuit I came up with

When detecting current on the power supply side using a differential input amplifier, such a circuit is possible.

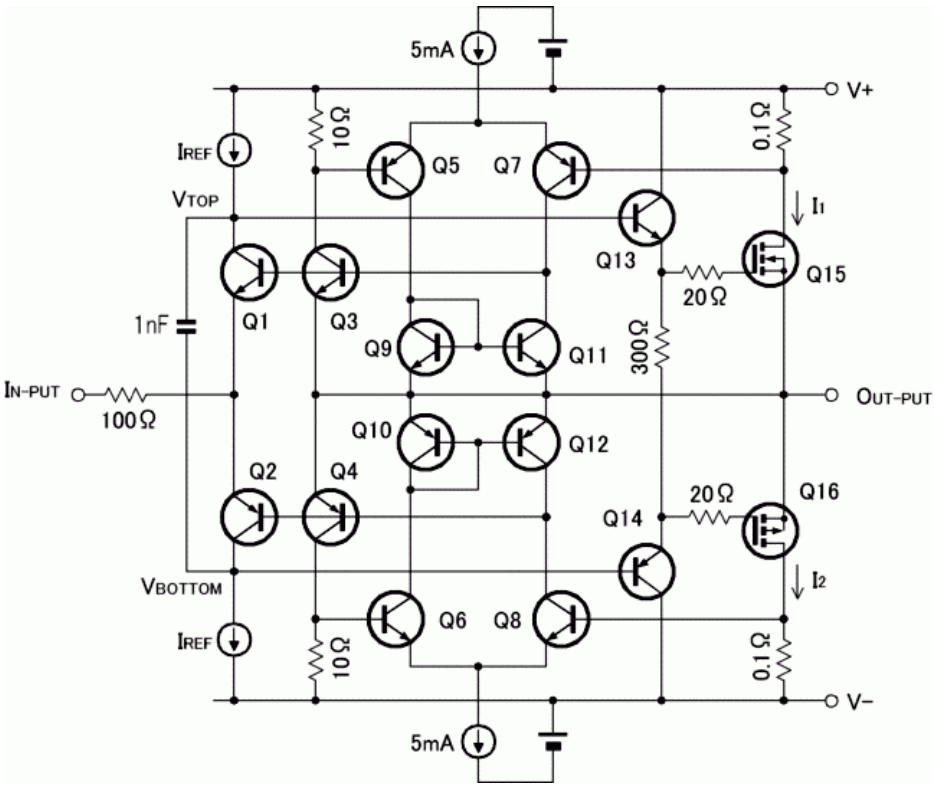


Fig. 23

The current of Q3 (Q4) is proportional to the current of Q15 (Q16). The currents of Q1 and Q2 that connect the bases to Q3 and Q4 are the values obtained by multiplying the currents of Q3 and Q4 and square root extraction.

The idea of developing a method that gives a signal to the base of the current multiplying transistor like the circuit above.

If an OP amplifier that can also suck current into U2 of the circuit below is used, the emitter current of Q3 is absorbed by U2, so Q4 is not affected by the Q3 side.

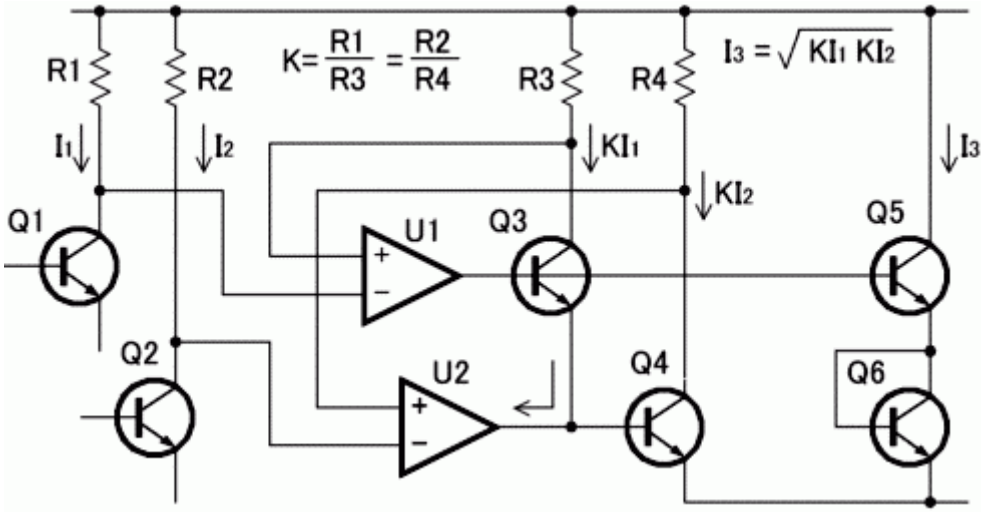


Fig. 24

Simplify **trans-linear bias circuit**

As shown in the figure below, by reducing the current of the output transistor by the resistance ratio of the current mirror circuit, etc., omitting the part that matches the level of the reference current, and using an element with an appropriate current ratio for the reference current side transistor and the output transistor current detection diode. I wondered if I could make a simple circuit.

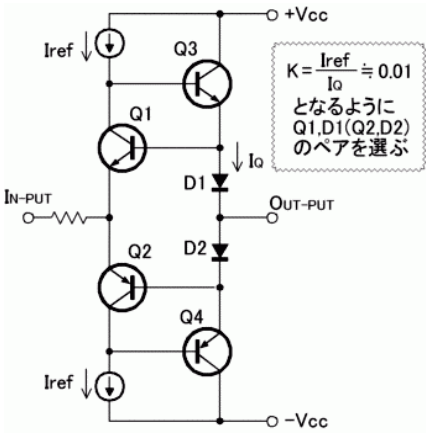


Fig. 25

In order to select Q1, D1 (Q2, D2), the current was measured with the circuit shown below.

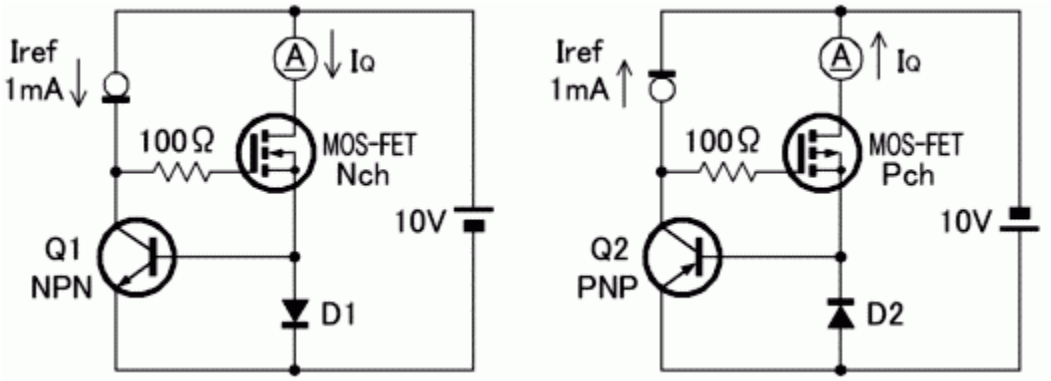


Fig. 26

I was lucky to find a pair of elements I had that could be used immediately.
Therefore, I haven't tried so many combinations, but I think it's a good line to guess by the ratio of the maximum rated current.
Low on-resistance MOS-FET body diodes can be used for D1 and D2. Q1 and Q2 are suitable for general-purpose small current transistors.
If Q1 and D1 and Q2 and D2 are not thermally coupled, there will be a difference in temperature change and the current will fluctuate, so it is convenient to use a type with mounting holes.

So, I made a prototype of the amplifier shown below using 2SC3423 / 2SA1680 for Q1 / Q2 and 2SK3844 for D1 and D2.
The pairing is not strictly done (it is not really unsorted, so it is not possible to match it by chance), but there is no particular problem.

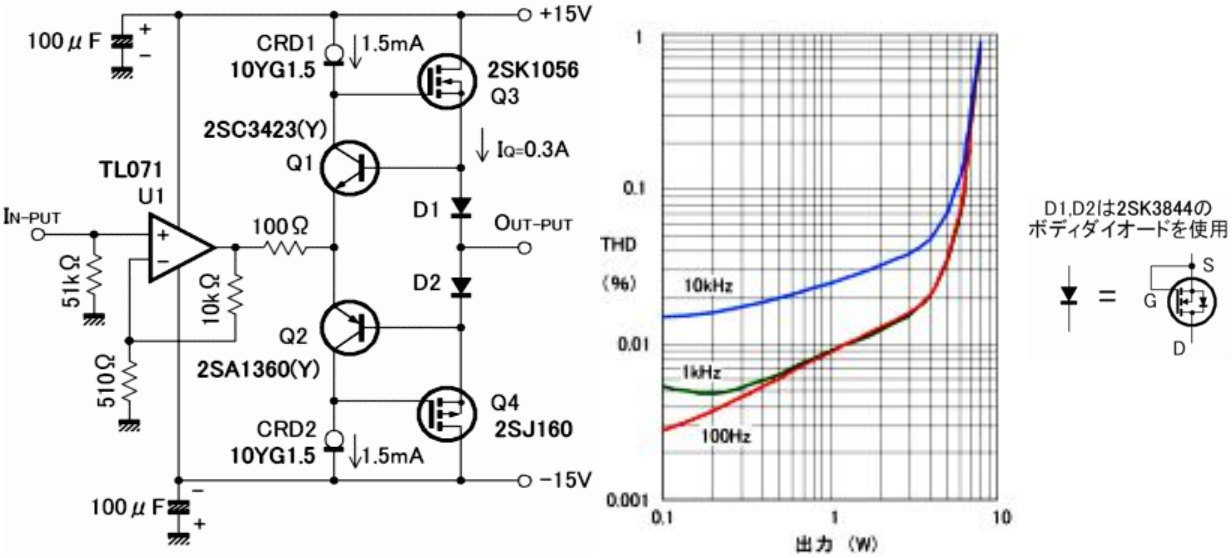


Fig. 27. Fig. 28. Distortion characteristics (8Ω load)

Frequency characteristics: 1kHz: 0dB, 100kHz: -1.5dB, 150kHz: -3dB

Output DC offset voltage: Immediately after power-on 15.6mV 30 minutes later 14.5mV
Idling current: Immediately after power-on 326mA 30 minutes later 296mA

The circuit configuration of this output stage seems to be a Wilson type current mirror circuit connected by complementary push-pull.
Then, when I thought that a Widlar [] type current mirror circuit could be used, I remembered that there was an article about an emitter resistanceless power amplifier in such a circuit in the sidewinder of MJ Radio and the experiment several years ago. January 2001 In the issue and the July 2003 issue, I was surprised that the poster was Mr. Minoru Shirakura, who was the same as the October 2006 issue of Radio Technology .
I think the trans-linear bias had already been created at this point, and despite my circumvention, the eyes of all MJ readers, who no one else talked about, were sad and sad.

Interpret the **translinear bias circuit as** *follows*

The transformer linear bias circuit shown below is a combination of two sets of complementary push-pull circuits with the base voltage connected in common.

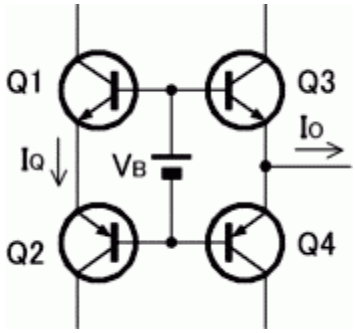


Fig. 29

The output current flows on the right side, but since there is no output current on the left side, it is always in the idling current state only.
If the left and right elements have the same characteristics, the idling currents of the left and right circuits are the same, so if you look at the current of the left circuit, you can read the idling current of the right circuit.
In this way, the circuit (Q1, Q2 part) that imitates a part of the operation of the controlled object (Q3, Q4 part) seems to be called a replica circuit in the streets.
In other words, it is just an analogy with the left circuit based on the base voltage without directly looking at the current in the right circuit.
Therefore, the characteristics and conditions (temperature, etc.) of the left and right elements must be the same.

This principle is the same as the method of simulating the bias voltage in Fig. 4 here , but it is wonderful that the circuit is much simpler than that.

This means that the bias voltage can be controlled by feedforward based on the base voltage of the output transistor without feeding back from the current of the output transistor as in the past.
The figure below stabilizes the idling current of output transistors operating at the same bias voltage by controlling the idling current of Q16 and Q17 to be constant.

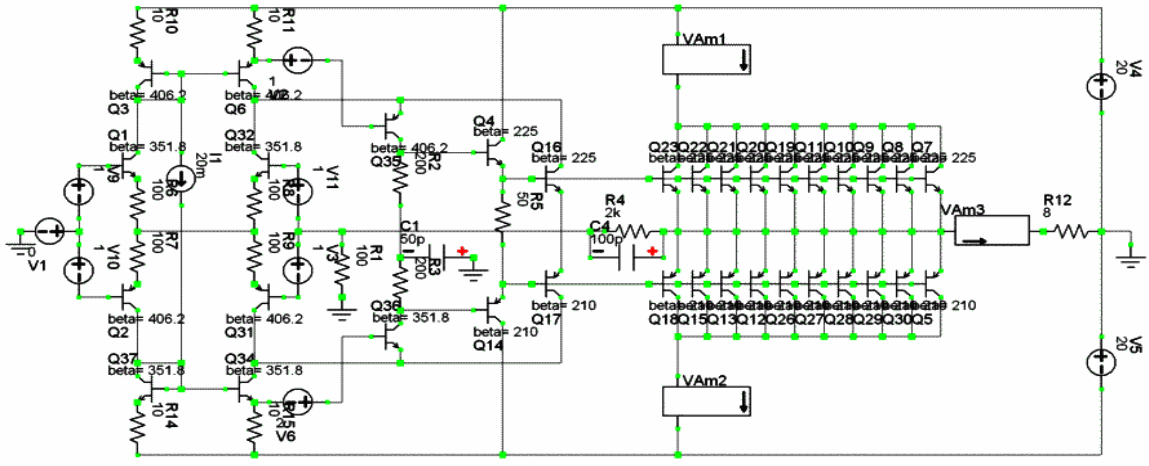


Fig 30

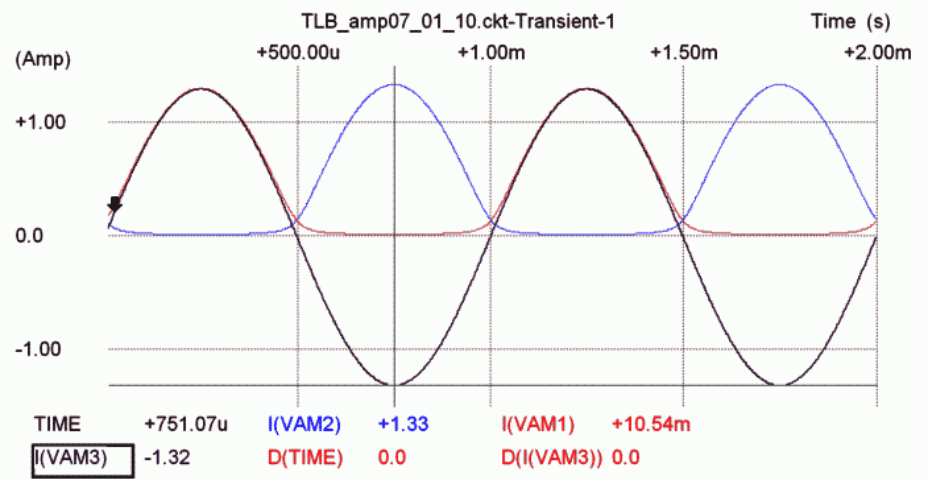


Fig. 30 Simulation of power amplifier by replica bias circuit (Q16 and Q17 are replicas of output stage)

The other side of the **trans linear bias circuit**

The replica circuit will be replaced with model data from the actual parts and saved in memory for use. Furthermore, it can be expected that the system will develop into a system that automatically tests the actual output element, collects model data, and updates the model contents as needed.