DAC simplified: the Synchronized Exponential Settling DAC

The basic function of the DAC is to convert the digital value as recorded into a proportional signal voltage at the correct moment.

Common errors
On the recording side:

- Insufficient limitation of frequency range to half the sample frequency
- Numerical calculation errors in the low-pass filter, adding distortion
- AD-converter timing errors (jitter)
- AD-converter linearity error (distortion)
- Dither amplitude error

On the playback side:

- DAC linearity
- DAC settling behavior
- Timing of sample output
- Low-pass filter errors

Common use
The sound quality of digital sources is suspicious. Many people prefer the sound of analog vinyl recordings for reason of reality and live awareness, despite the limited frequency response, poor channel separation, hum and rumble, scratches and poor signal to noise ratio of analog playback systems.
High-demanding audio purists use special CD-players, stabilized with marble platform, use of low-jitter clock systems and an external DAC with minimum low-pass filter and class-A vacuum tube amplifiers without feedback.

The best thing a DAC can do is the conversion of the digital signal representation in an analog voltage, without distortion addition and on the correct moment in time. Not more and not less; you can't do better with the available information.

SES-DAC-system
Proposed in this document is a simple NOS-DAC with unique settling error correction and unique time error correction. The design allows a solution where jitter can be corrected without control of the master clock.
The system name is ***Synchronized Exponential Settling DAC system.***

The unique properties of this system follow from a very simple basic approach that does not require special education or experience to understand fully.

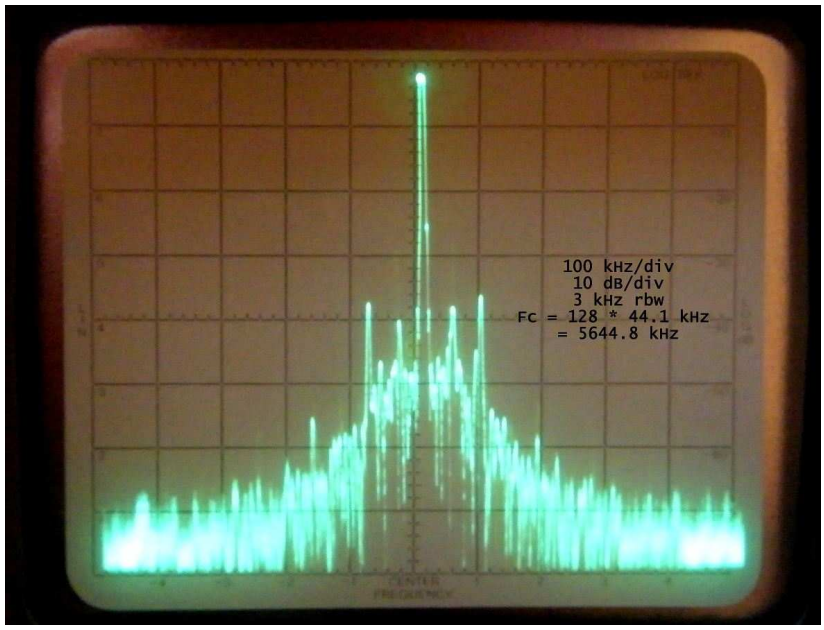
Step 1 in understanding is the synchronization. Existing DAC systems give the next audio sample in the rhythm of the word select signal. The DAC converts the digital 16-bit value into a voltage and the voltages, left and right stereo channel, maintain their value up to the availability of the next sample. The time duration of a sample is one over the sample frequency and is 22.67 µs for CD playback systems without oversample filter systems. Jitter on this word-select clock signal affects the moment and the amplitude of the obtained output signal. Jitter is caused by the digital

playback source: compact disc player, computer clock, media player and when used an S/P-DIF receiver. The jitter of such sources is in the order of nanoseconds.

DIR9001 output pin 4 SCKO 5644.8 kHz regenerated clock from S/P-DIF

Strong spurious at 88.2 kHz offset from carrier.
Spur value -35 dBc corresponds to modulation index = (-29 dB =) 0.035. Time error for this peak-phase is 0.0056 period time or 1 nanosecond peak, 700 ps rms.

(Specification 50 ps rms, probably on a non-SPDIF clock or only valid for the wideband noise floor).



The synchronization system is a sample-hold that takes a sample of the settled value of the DAC output. The sample-hold clock is derived from a high-performance synchronized oscillator. The oscillator synchronization is obtained by means of a PLL system with very low loop bandwidth. The sample duration is (example value) 10 µs where the sample moment can vary over (22.67 – 10 =) 12.67 µs. This gives plenty of time for a synchronization system. There are almost no requirements for the jitter of the source system; any player with an S/P-DIF output can be used. Also the S/P-DIF receiver is without special requirements. The only requirement is that the digital value is available at the output (word select, bit clock and serial data) as a bit-true copy of the data on the disc[1].

The outcome: the sample-hold gives the settled output value of the DAC at a moment that is not depending on jitter from the digital source. The final jitter is solely depending on the regenerated clock that is used for the sample moment.

Step 2 in understanding is the exponential settling of the DAC. The output voltage per sample, not the energy, of a DAC sample is proportional with momentary voltage and proportional with sample duration. The translation from jitter to unwanted output is in this way very simple, just like the conversion in a pulse-width modulator or amplifier. The error voltage contribution for each sample is proportional with the rms-jitter value divided by the audio sample period time. This is also true for the settling of the DAC from the actual output voltage value to a new voltage. This settling must be without distortion addition. There are two solutions: (1) fixed settling time, independent from the size of the voltage jump and (2) exponential settling, like an RC-low-pass filter.

[1] Bit-true: this excludes S/P-DIF systems that contain a digital volume control. Also players with concealment are not recommended (all CD and DVD players!). Use of media players with read from SD-card or hard-drive storage with low bit error rate is preferred.

The only practical solution, exponential settling, guarantees a constant group delay for the signal, independent from the actual voltage or the size of the voltage jump.

The problem in DAC's is that settling can deviate from the preferred exponential settling due to a slew-rate limitation of that settling or due to an output capacitance that depends on the connected current sources for the specific binary input word. *That explains why settling behavior depends also on the termination or load impedance of the DAC output. This is probably an explanation for the minor sound differences when DAC's are used with different load impedance.*

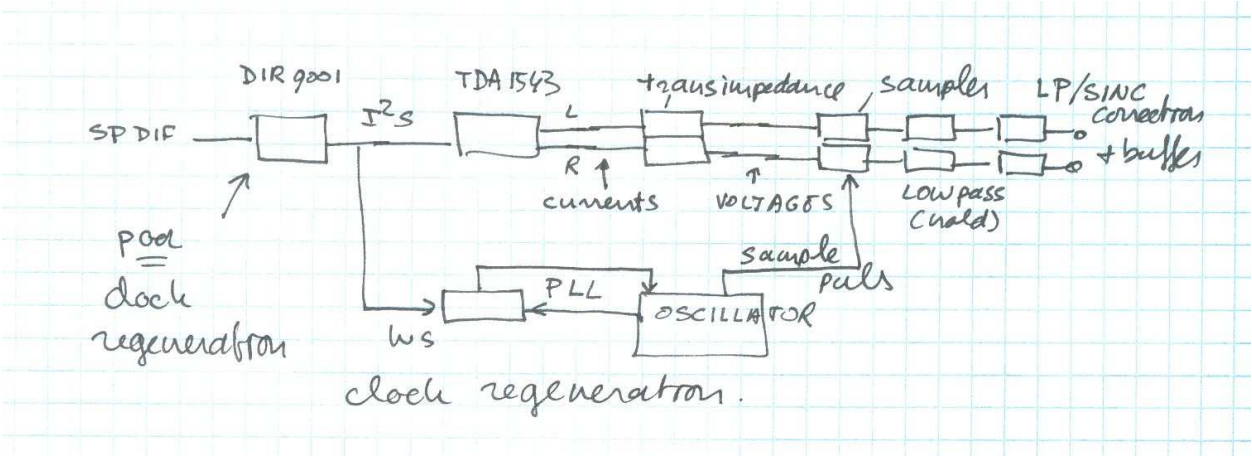
The **Synchronized Exponentional Settling** system makes use of a sample-hold circuit without slew-rate limitation. The sample-hold takes a sample of the settled DAC value. In this way the sample value accuracy corresponds to the static performance of the DAC, without any settling artifact of the DAC itself. The timing accuracy of the output sample sequence is not depending on momentary jitter of the digital source clock. The timing is solely determined by the S-H-clock.

The Synchronized Exponential Settling system is in this way a very accurate NOS (non-oversample filter) DAC with linearity that is as good as the static DAC performance, and jitter down to the level of a clock source that is easy to understand and easy to adapt to your own wishes. The SES-DAC system can be used with all flash-DAC systems, NOS and also 4 or 8 times oversample systems, but not with sigma-delta DAC systems.

Hardware example

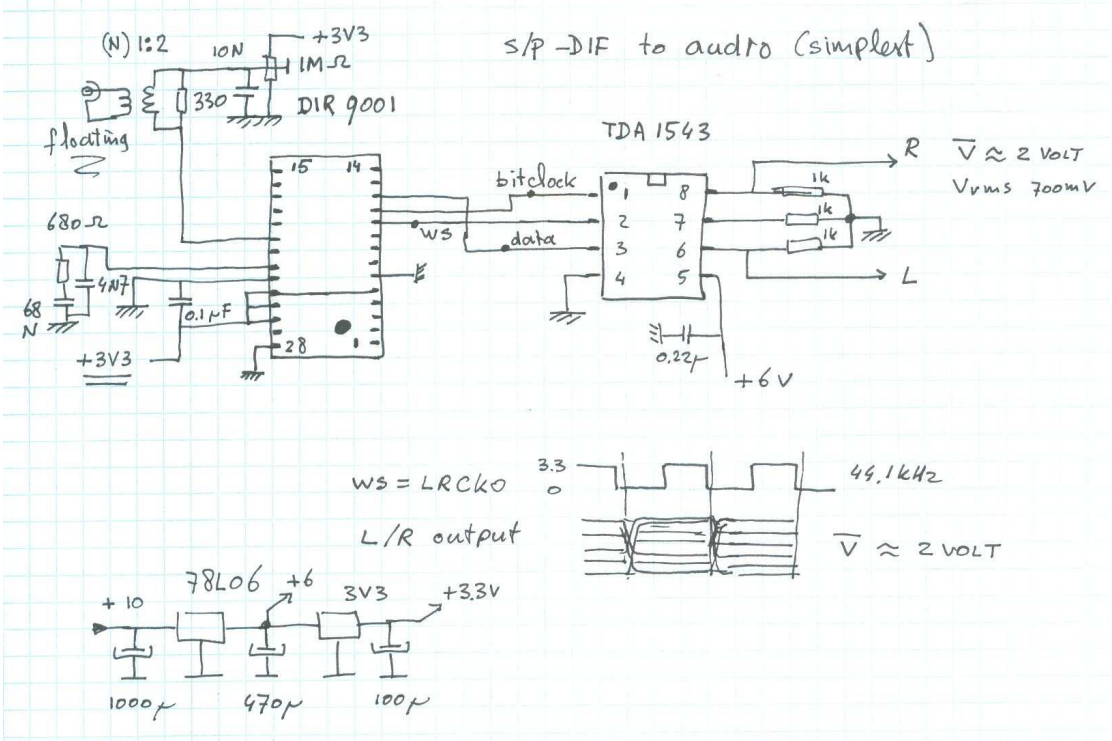
- S/P-DIF receiver based on DIR9001
- DAC is TDA1543 with low load impedance termination (trans-impedance amplifier with low input-impedance or in other words a I_to_V-converter)
- The sample-hold is realized with 74HC4066. The signal peak current in the switch is limited to maximum 1.5 mA to prevent non-linear response (current limitation, leading to modulation of the effective time constant of the sampler). This is the base for sampling with exponential settling, without distortion due to slew-rate limitation.
- All amplifiers are OPA2134. The first module was built with discrete transistor amplifiers without feedback. The OPA2134 is not at all causing degradation in the given hardware example
- The simple analog low-pass filter reduces the slew-rate of the output signal to be able to connect moderate-slew-rate power amplifiers
- The analog low-pass filter contains a SINC frequency transfer correction
- The regenerated clock is based on a simple low-frequency VCO system running at 8 times F_sample (352.8 kHz for CD or WAV playback). The range of this oscillator is 256 to 384 kHz to allow all sample rates between 32 and 48 kHz.
- The simple VCO clock signal can be replaced by a high-performance VCXO system running at an integer multiple of the 8*Fs-clock. The on-board PLL components can be used (after modification) to control the VCXO with loop bandwidth at your choice. *When you are jitter-sensitive then this design can solve your last problem.*

System overview:



Supply voltages for hardware: +9 volt, 110 mA (+30 mA, see below), +6 volt, 70 mA, +3.3 volt, 20 mA.
Optional: output buffer/headphone amplifier: plus and minus 9 volt, 30 mA each.

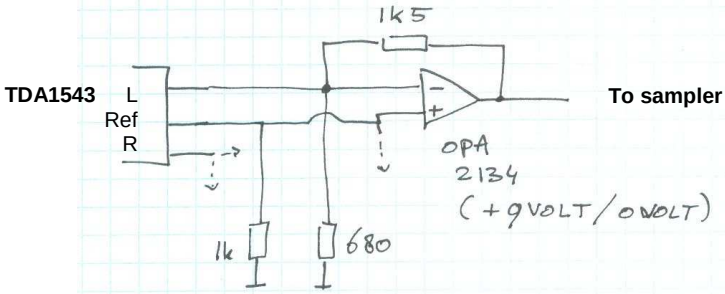
DIR9001 + TDA1543



DAC output trans-impedance amplifier (or virtual zero input amplifier or I-to-V-converter)

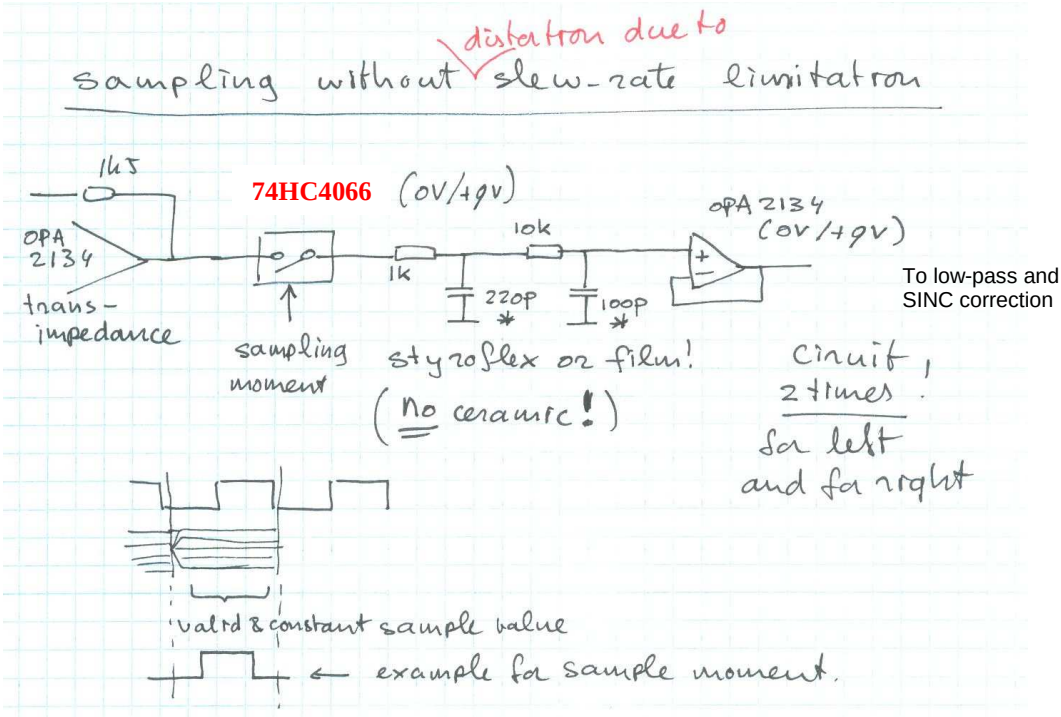
TDA 1543

The output current can be converted into a voltage by means of a resistor. Since the output impedance is not infinite (capacitance is DAC current switches setting dependent) it is recommended to use a virtual-zero (trans-impedance amplifier) or low termination impedance.

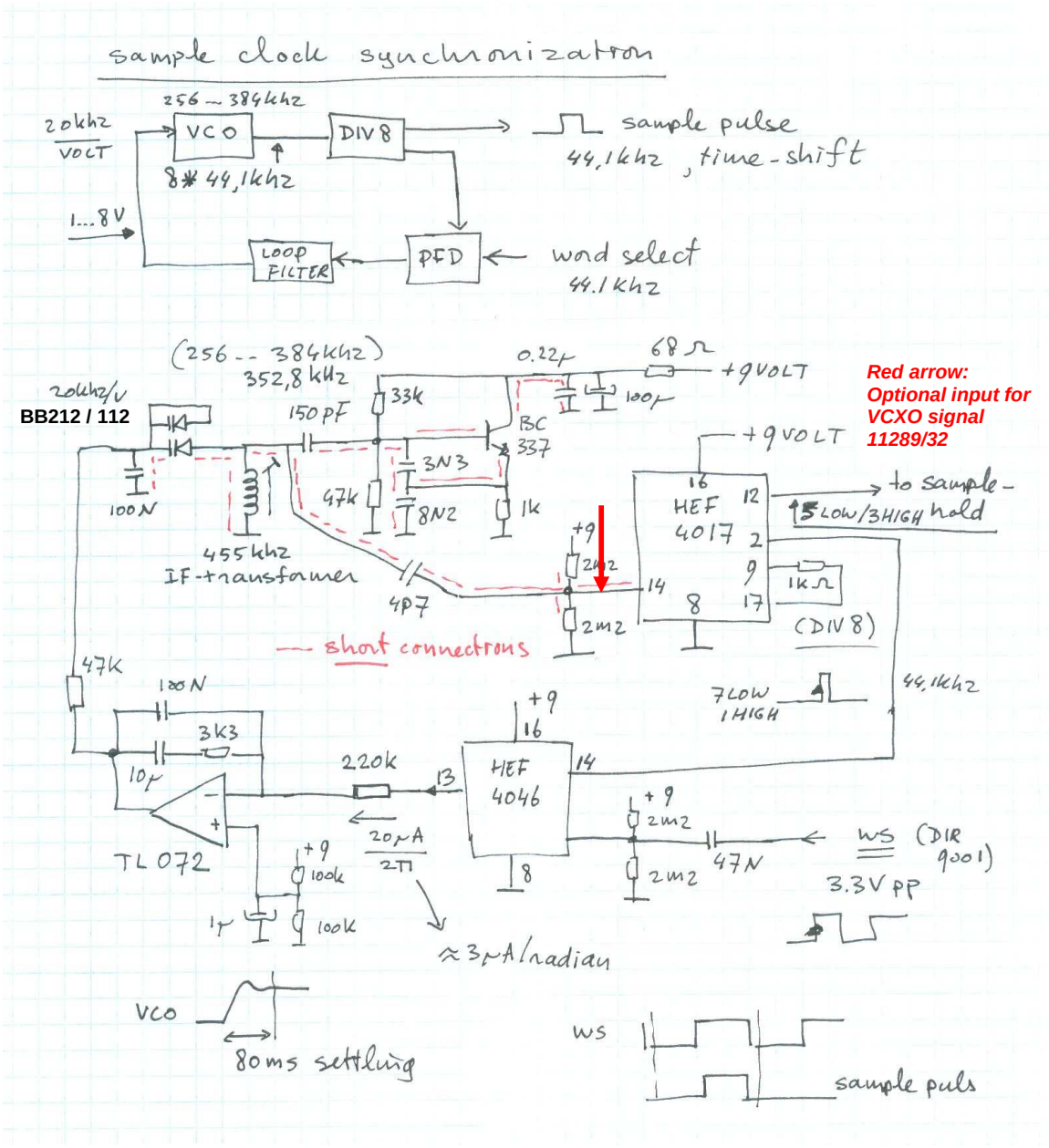


This amplifier is almost fast enough to follow the fast settling of the DAC.
Since SES uses a sample-hold on the settled value there is no problem with this minor short coming.

Sample-Hold without slew-rate-caused distortion

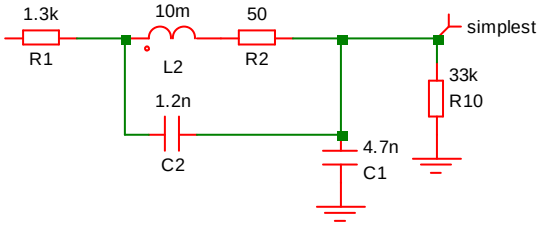


Clock regeneration and sample-hold timing



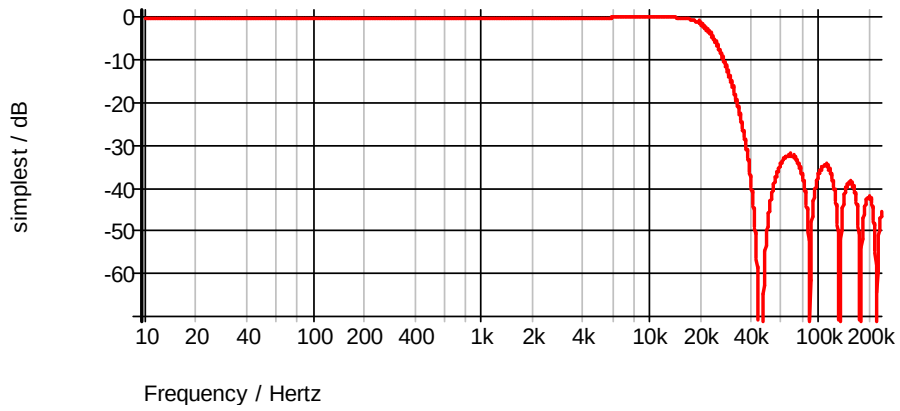
Red arrow: Optional input for VCXO signal 11289/32

Low-pass filter with SINC correction



(50 Ω is the DC-resistance of the inductor)
(33 kΩ is potentiometer 50k and 100k parallel. Check the potentiometer resistance!)

Frequency transfer when connected to a DAC with first-order hold (Fs = 44.1 kHz)



Discussion for Synchronized Exponential Settling DAC as described

Sound quality: can it be better? The recorded data is represented as correct number at the correct moment. There is no more data available.

Errors in the system:

- Limited linearity of the DAC TDA1543. Example for DAC replacement: Burr-Brown TI flash-DAC (1704)
- Non-perfect oscillator for the clock regeneration. Example for clock modification: 11289 kHz VCXO with (modified) low-bandwidth PLL

General on digital audio: is the presence of unwanted high-frequency spectrum above 20 kHz audible or is the perceived audio performance affected by these frequencies? When the answer is no, then the SES-DAC is the ultimate DAC.
Note: output slew-rate of low-pass filter is maximum (worst-case signal condition) 0.2 volt/µs

Information that can help you:

- The use of parallel DAC's to improve the conversion accuracy (www: Pavouk, DDDAC and others) makes little sense. A common mistake in using multiple TDA1543 DAC's is the connection of the reference current setting pin of all the parallel chips to one single resistor. The reference voltage of separate chips is around 2.18 volt but there is a production tolerance per chip, just like zener diodes do have. The actual reference current setting per chip is almost undefined, at least insecure, when all pins are connected to one resistor. The output pins can be connected together.
- The use of a current to voltage converter at the output of a (current-output) DAC makes more sense than putting the DAC's in parallel. The DAC settling and the slew-rate of the I_to_V-converter must fit. Use of a vacuum tube is not a bad idea at all. ***The SES-DAC takes a sample after DAC-settling and the slew-rate of the I_to_V converter is not a limitation!***

End of document.
Frans Sessink, 2010 May/June