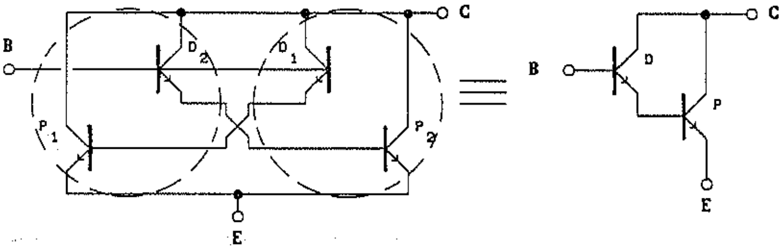

Fig. 9. Thermally cross-coupled Darlington transistor to extend SOAR. Driver D_1 (D_2) is thermally coupled to power transistor P_2 (P_1) [12].

TABLE I
MEASURED TOTAL HARMONIC DISTORTION

Total harmonic distortion + noise (THD+N) in dB					
Breadboard (P_o max = 12W)			ACBA-chip (P_o max = 2.5W)		
f=1kHz	10 kHz	20 kHz	f=1kHz	10 kHz	20 kHz
-87	-86	-84	-81	-79	-77
-90	-86	-83	-88	-82	-76
-91	-86	-83	-88	-81	-75

TABLE II
PERFORMANCE FIGURES

Parameter		Breadboard (V_S=± 15V)	ACBA-chip (V_S=± 8V)
Bandwidth	A_V = 30 dB	1.2MHz	700 kHz
Gain-margin		12 dB	21 dB
Phase-margin		57°	75°
$\|Z_{out}\|$ ($f \leq$ 20 kHz)		30 mΩ	15 mΩ
Open-loop gain (DC)		92 dB	88 dB
Slew-rate		20 V/μs	12 V/μs
Quiescent current		58 mA	57 mA

process and next integrated on our semicustom bipolar analog cell-based array (ACBA) [10], [11] which is manufactured in an 18-V process. A photomicrograph of the ACBA chip realization is shown in Fig. 8. A suitable reference current circuit was included. The large output Darlington transistors Q_1, Q_{1a} and Q_2, Q_{2a} were external devices fabricated in a power IC process. Also the sensing transistors Q_5 and Q_6 were kept external to enable mounting in close thermal contact with the output transistors. Capacitor C_2 (220 pF) was external as well. In a final chip design all these components would be integrated.

The power Darlington transistors used have a thermally cross-coupled structure to extend the safe operating area (SOAR) as shown in Fig. 9.

It has been shown [12] that this technique of using the driver of the one power transistor to sense the temperature of the other power transistor is a simple yet effective method to ward off destructive secondary breakdown. The operating mechanism is based on changing the thermal runaway characteristic inherent to bipolar transistors to an electrothermal negative feedback loop which is stable up to significantly larger temperature gradients.

VIII. Measured Results

The breadboard and ACBA prototype were operated with a resistive load of 7 Ω and symmetrical supply voltages of ±15 and ±8 V, respectively. These supply voltages were dictated by the process used and restrict the maximum achievable output power to 12 and 2.5 W, respectively. However, the design is intended for a 60-V process thus enabling more than 40 W to be achieved, as was verified by computer simulation. Closed-loop gain used was 30 dB.

The expected class *AB* biasing behavior as depicted in Fig. 6 was verified.

Total harmonic distortion was measured with an AA501 Tektronix distortion analyzer. No filters were used, therefore noise was included in the measurement. The results are shown in Table I. Simulations performed for various power levels up to 40 W indicate a constant level of distortion comparable to the measured result.

Open-loop gain and phase margin and closed-loop output impedance were measured using a network analyzer. The results, together with additional performance figures, are listed in Table II. We see that gain and phase margin are satisfactory, indicating a stable design. The chip realization is somewhat overcompensated as a result of choosing $C_c = 9$ pF instead of 6.8 pF as in the case of the breadboard. Nevertheless, the slew rate and closed-loop bandwidth are adequate. From Table I we see that low-frequency distortion for breadboard and ACBA realization are very similar. For higher frequencies the latter case produces somewhat more distortion due to the overcompensation which reduces the high-frequency loop gain. Nevertheless, the total harmonic distortion is around −80 dB at 20 kHz, which is very satisfactory.

Fig. 10 shows the residual distortion signal plus noise measured with the distortion analyzer at 20 kHz both for the breadboard and for the chip prototype. We see mainly some noise and slight, well-behaved crossover distortion.

Finally, an attempt was made to measure the intermodulation distortion (SMPTE, 60 Hz, 7 kHz, 4:1). It could not be measured with the equipment used, indicating a level of less than −87 dB.