

Fig. 7. Circuit diagram of complete power amplifier.

illustrates the nearly ideal class *AB* behavior obtained with the harmonic-mean control law (6), and compares it to the conventional technique.

## VI. COMPLETE POWER AMPLIFIER CIRCUIT

Fig. 7 shows the circuit diagram of the complete power amplifier except for some dc bias current sources.

The capacitor  $C_c$  provides conventional pole-splitting phase compensation for closed-loop stability. Capacitor  $C_2$  provides high-frequency signal feedforward to  $Q_2$ . This eliminates the phase shift at high frequencies caused by the amplifier stage  $Q_3, Q_4$ . In addition, these capacitors serve to stabilize the bias control loop by providing dominant poles at the collectors of  $Q_3$  and  $Q_4$ . The remaining circuitry has been discussed in the preceding sections.

Note that the output can swing down to  $V_{BE} + V_{CEsat}$  above the negative supply and up to  $2V_{BE} + V_{CEsat}$  below the positive supply. The output swing can be made symmetrical by bootstrapping the current source driving to the base of  $Q_{1a}$ . The output swing can be further increased by also bootstrapping the collector of  $Q_{1a}$  and by connecting the collector of  $Q_{2a}$  to  $+V_s$ .

## VII. EXPERIMENTAL CIRCUIT REALIZATION

In order to experimentally test the new design concepts, the circuit of Fig. 7 was first breadboarded using transistor arrays (kit parts) manufactured in a 40-V bipolar IC

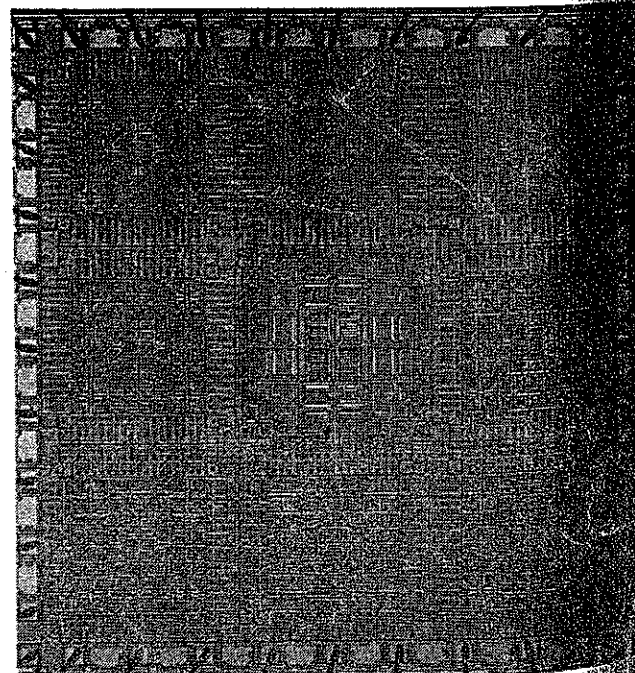


Fig. 8. Photomicrograph of prototype chip realization using our custom ACBA [10], [11] which measures  $4 \times 4 \text{ mm}^2$  and contains 450 transistors, 400 resistors, and 50 capacitors, evenly distributed in nine highly symmetrical clusters or tiles.