

1-2: Surprise  
(momentary button)

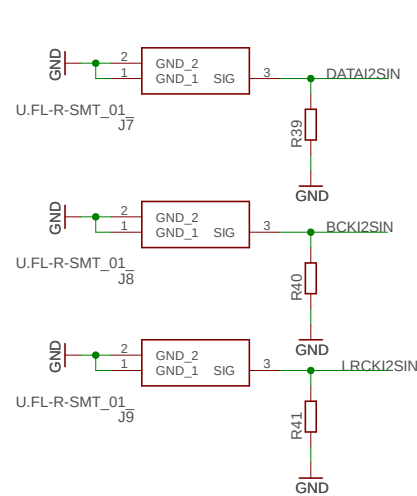
1-2: Loud  
3-4: Medium  
5-6: Soft

For future

Filter type  
1-2: halfband  
3-4: apodizing  
5-6: steep  
7-8: surprise

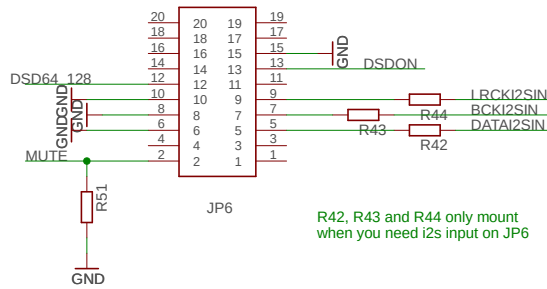
Delta-sigma method  
1-2: surprise  
3-4: PWM9  
5-6: PWM5  
7-8: chaos

1-2: de-emphasis

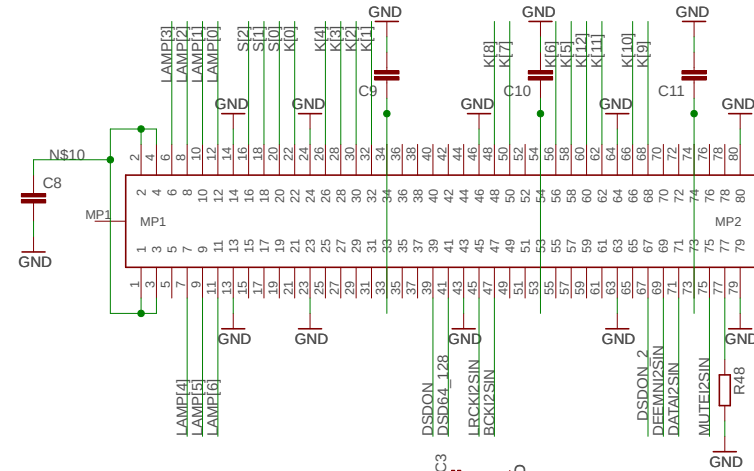
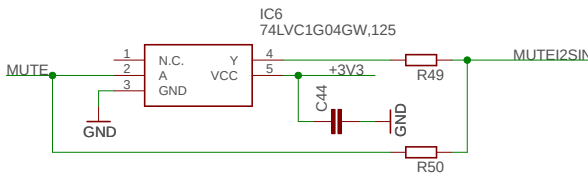


DSDON, must be 0 for PCM or DoP,  
1 for raw DSD.

DSD64\_128, must be 0 for DSD64 and 1 for DSD128  
when the raw DSD interface is used.

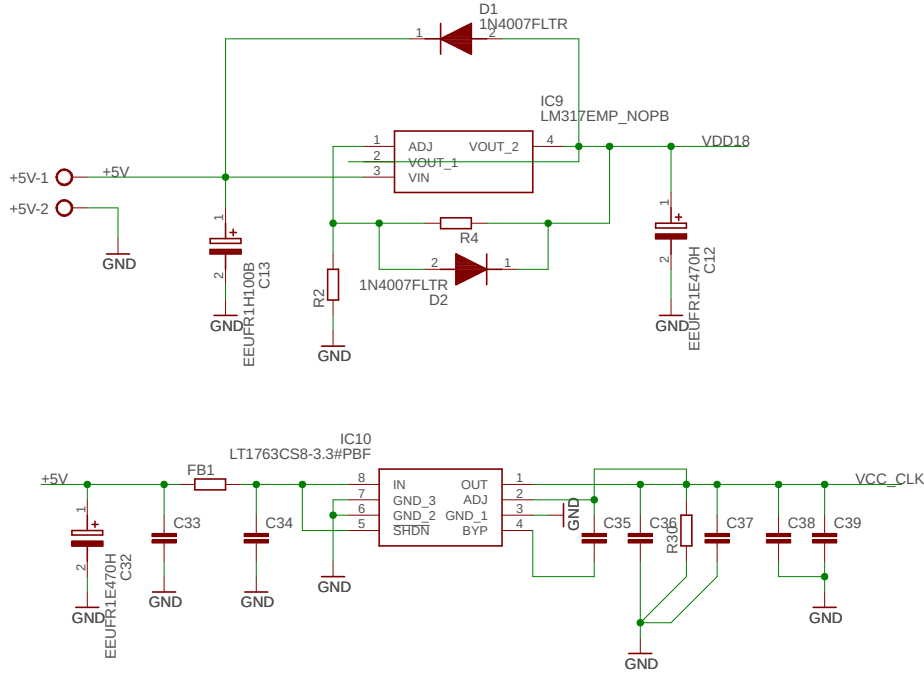
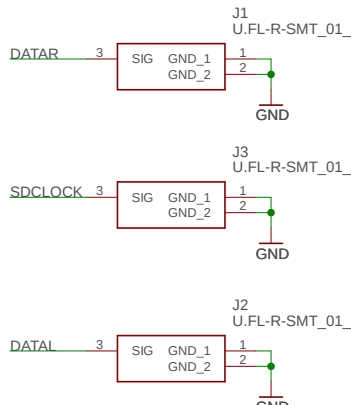
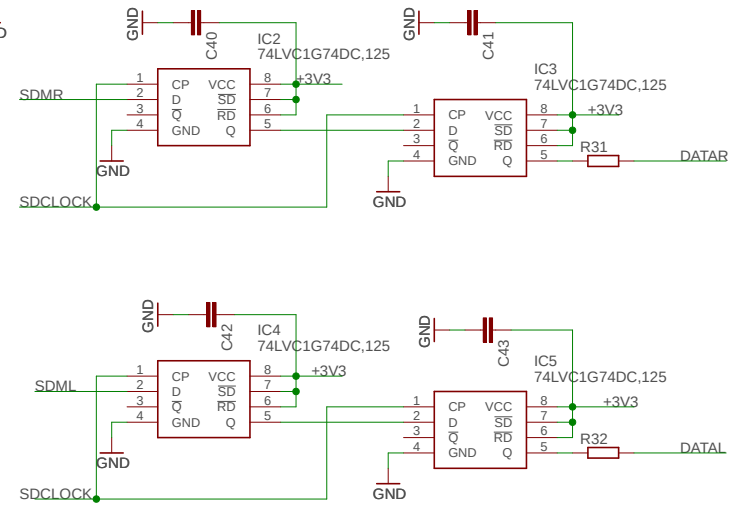
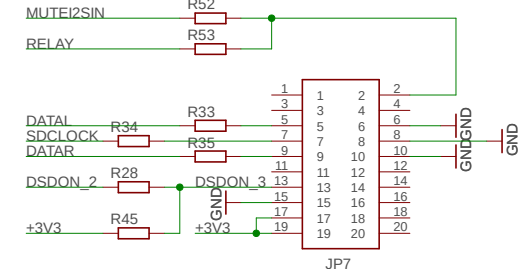


One and only one of R49 and R50  
to be mounted:  
R50 for Input MUTE active-high  
R49 for Input MUTE active-low

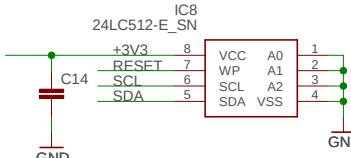
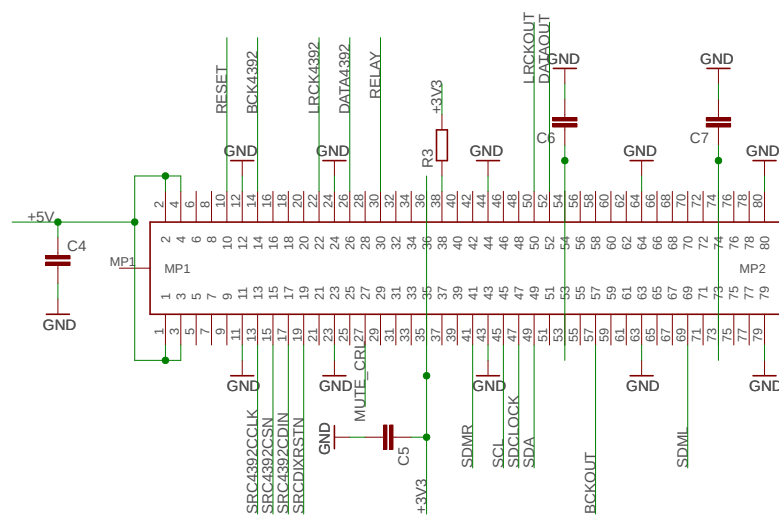
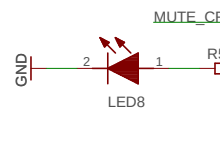


J4, J5: connectors to equally-named connectors on FPGA module  
(TE06030 module with XC6SLX75 or XC6SLX45)

R33, R34 and R35 only mount  
when you need i2s output on JP7



R47 mounted by default  
R46 for future use (NM)



One and only one of R36 and R37  
to be mounted:  
R36 for internal clock  
R37 for external clock

