Low Distortion Oscillator Design

Master Thesis in Music

submitted by

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Abstract

Verifying the quality of audio recording and playback devices typically involves harmonic distortion measurements. In such measurements the resolution is limited by the residual contribution of the used sinusoidal oscillator. Known oscillator designs cannot offer sufficiently low distortion contribution for the evaluation of contemporary high-performance audio devices; this applies in particular to fundamental frequencies of more than a decade below or above 1 kHz where the usually employed RC oscillator topologies show increased distortion. The results of this thesis are new methodologies for design and realisation of very low distortion RC oscillators. In particular electronic circuits for operational amplifiers, multipliers and level detectors with negligible distortion contribution at the −140 dBc level are presented. For each circuit the quality of the applied design procedures and theoretical models is supported by quantitative measurements across an appropriate range of frequencies and operating levels. Furthermore a measurement procedure for the evaluation of passive components is presented which exceeds the resolution of previous measurement methods by an order of magnitude. A full oscillator design using the new low distortion design methodologies is discussed; while the distortion residual of this new oscillator design is below the resolution of available distortion analyzers measurements of known distortion sources in isolation indicate that its overall distortion performance exceeds the −140 dBc level.

Acknowledgements

The presented work has been carried out from July 2009 to May 2010. My sincere thanks are given to Daniel Weiss (Weiss Engineering Ltd., Uster, Switzerland) for the provision of an Audio Precision SYS-2722 audio analyzer which was a necessary measurement tool for performance verification. I am very grateful to Bruce E. Hofer (Audio Precision Inc., Beaverton, USA) who has contributed invaluable information on low distortion oscillator design. Also I'd like to thank my parents and friends who have supported me during the work for this thesis.

Contents

Chapter 1

Introduction

1.1 Motivation

In recent years the technical quality of audio recording and playback devices (such as AD- and DA-converters, preamplifiers, power amplifiers and equalisers) has reached a very high standard. With contemporary electronic components it is now routinely possible to design analogue circuits with distortion levels of $-110\,\mathrm{dBc}$ to $-130\,\mathrm{dBc}$ within the audio frequency range (20 Hz to 20 kHz). Along with this progress goes an increasing demand for high-resolution measurement equipment to verify the achieved distortion levels.

The most common distortion measurement procedures are based on sinusoidal excitation [1]. Thereby the input of the device under test is connected to an oscillator and the output routed to a distortion analyzer. This analyzer contains a notch filter which suppresses the fundamental frequency. The residual signal consists of distortion products and noise from the device under test. The amplitude of the residual may then be set in relation to the amplitude of the fundamental; the amplitude ratio is typically expressed in percent or in Decibels. A total harmonic distortion and noise (THD+N) measurement A_{THD+N} is defined as follows:

$$A_{THD+N} = \frac{\sqrt{\sum a_i^2 + a_N^2}}{a_1} \quad \text{for } i = 2 \ldots n+1 \tag{1.1}$$

where a_1 is the amplitude of the fundamental frequency, a_i the amplitude of the harmonics and a_N the amplitude of the residual noise. The number of included harmonics n and the bandwidth of the residual noise a_N is defined by a low pass filter ahead of the level meter.

By means of a spectrum analyzer it is possible to observe the magnitude of the individual harmonics and thereby to eliminate the residual noise a_N.

This leads to a total harmonic distortion (THD) measurement A_{THD} which is analogously defined as follows:

$$A_{THD} = \frac{\sqrt{\sum a_i^2}}{a_1} \quad \text{for } i = 2 \ldots n+1 \tag{1.2}$$

For these measurements it is important to apprechiate that the individual harmonics of oscillator and device under test interact and accordingly alter the observed distortion level of the device under test. Depending on their phase relationship Θ the amplitude of the individual harmonics of the device under test x_{dut} and the oscillator source x_{osc} may either add arithmetically, add geometrically or cancel in the distortion measurement y [5]:

$$y = \begin{cases} x_{dut} + x_{osc} & \text{if } \Theta = 0 \\ \sqrt{x_{dut}^2 + x_{osc}^2} & \text{if } \Theta = \pm\frac{\pi}{4} \\ x_{dut} - x_{osc} & \text{if } \Theta = \frac{\pi}{2} \end{cases} \tag{1.3}$$

More generally speaking, the distortion sum of oscillator and device under test is calculated by treating x_{dut} and x_{osc} as complex variables and the use of vector addition:

$$y = |x_{dut} + x_{osc}| \tag{1.4}$$

If amplitude and phase of the oscillator source harmonics are known it is hence possible to calculate the true distorion characteristics of the device under test by vector subtraction of the oscillator residual. However the problem is further complicated by the fact that the analyzer will also contribute some distortion which has so far been assumed to be negligible. If the device under test has unity gain a composite residual measurement for oscillator and analyzer may be made by bypassing the device under test. However the device under test will in general have gain other than unity; this leads to different operating levels of the analyzer when the device under test is bypassed which invalidates the result. Additionally load and source impedances of the device under test introduce variables which are difficult to incorporate.

In practice it is hence necessary to make the oscillator contribution negligible by reducing the level of its contribution. Acceptable accuracy requires at least 10 dB and preferably 20 dB lower distortion than the device under test. To measure a device with distortion levels of -130 dBc an oscillator source with distortion at -140 dBc or less is therefore needed. Even the best commercially available oscillator (the Audio Precision SYS-2700 Series [7])

achieves only typical (but not guaranteed) levels of −130 dBc (1 kHz) and −120 dBc (25 Hz to 20 kHz) of the individual harmonics.

A further limitation of typical low distortion oscillators is their limited frequency range of usually 20 Hz to 100 kHz. Distortion measurements beyond this range are useful for testing audio equipment as they may give evidence e.g. of particular sensitivity to radio frequency interference or thermal modulation effects. The distortion requirements may be relaxed though in this extended frequency range as the figures observed are typically higher than in the audio frequency range. The goal of this thesis is the development of an oscillator with a distortion level of the individual harmonics at or below −140 dBc for fundamentals in the audio frequency range and an extend frequency range of 3 Hz to 300 kHz in order to provide a tool that allows accurate measurement of low distortion analogue circuits.

1.2 Task Description

This thesis comprises the design of an oscillator which has both very low distortion within the audio frequency range and an extended frequency range. Its main specifications may be characterised as follows:

Frequency range:	3 Hz to 300 kHz
Amplitude range:	−60 dBu to +20 dBu
Individual harmonics:	≤ −140 dBc 20 Hz to 20 kHz ≤ −100 dBc 3 Hz to 300 kHz

The thesis should include the following design steps:

- Compilation of detailed specifications based on above table.
- Design and realisation of a suitable oscillator.
- Performance verification with consideration of measurement uncertainty; comparison with the specifications and justification of not reached goals.
- Writing of a report which demonstrates both used methodology for design, realisation and verification and provides a comprehensive documentation for operation, servicing and further development of the oscillator.

1.3 Preliminary Notes

Verification of the oscillator performance presents a substantial difficulty—namely the availability of a notch filter (or any other means to measure distortion) with itself negligible distortion contribution. At the residual levels intended and for the current state of the art it is very difficult to design such a notch filter; furthermore the lack of a distortion-free standard prohibits notch filter performance verification. Hence particular attention to the isolation of the main distortion sources present in the chosen oscillator topology is given in this thesis. By several techniques which are detailed in the following chapters it is verified that each main distortion source contributes substantially less distortion than the design goal. By adding up the measured contribution of the isolated main distortion sources it is possible to derive a worst-case estimate of their total sum.

An oscillator suitable for laboratory use includes—besides the basic oscillator circuitry—an output stage with sufficient load drive capability and level switching as well as a power supply. In this thesis we will only discuss the design of the basic oscillator circuit; output stage and power supply implementation must be left for future research.

1.4 Notation

In this thesis we will commonly refere to the Decibel. dBu denotes an amplitude unit with reference to the $0.7746\,\mathrm{V_{RMS}}$ level. dBc is used for distortion and noise measurements and references to the level of the carrier signal (i.e. here typically the oscillator signal). For the dBr an explicit reference level is given in the context.

1.5 Document Outline

In chapter 2 we will present the detailed specifications for the oscillator design and outline the fundamental concepts of the intended implementation. The following chapter discusses the implementation of the main oscillator loop. The design of the operational amplifiers used in the main signal path of the oscillator is presented in chapter 4. Chapter 5 presents the level detector circuitry which is used to sense and stabilise the oscillator amplitude; also included in this chapter are the error integrator, the startup circuit and the indicator for amplitude settling. Chapter 6 considers the realisation of the multiplier circuit while chapter 7 presents measurements of the overall oscillator performance. Finally chapter 8 summarises the results of this thesis and suggests some topics for future research.

Due to their considerable size and for the convenience of the reader the schematic diagrams and overlay prints are combined in a separate document.

Chapter 2

Specifications and Overall Design Concept

In this chapter we will present the extended specifications set out for the oscillator design and elaborate on the overall design concept. In particular this includes a discussion of the basic oscillator design problems and the suitability of available oscillator topologies.

2.1 Specifications

The tables on page 10 and 11 present the detailed specifications for the oscillator design. These were defined after consideration of the published prior art and measurement of a first prototype. The specifications are composed for a full oscillator design including output stage, mix input for multi-tone measurements and a sync output. However in this thesis we will only consider design and verification of the actual oscillator board.

2.2 Distortion Limitations in Oscillator Design

There are a number of possible ways to generate analogue sinusoidal waveforms [1]:

- RC oscillator
- Function generator
- Frequency synthesiser
- Digital synthesis and subsequent digital-to-analogue conversion

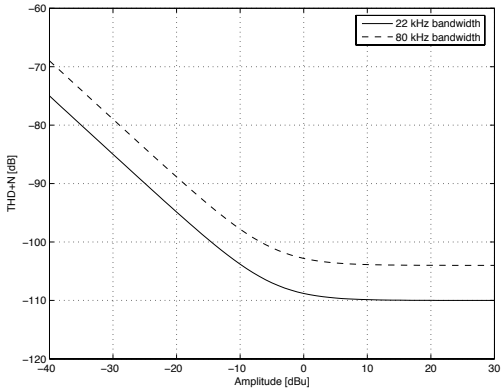
Of these four means only the RC oscillator is suitable for the residual levels and frequency range intended. It does however have the disadvantage

Output Characteristics	
Output Impedance	
Balanced Output	50 Ω, 150 Ω, 200 Ω or 600 Ω
Unbalanced Output	25 Ω, 75 Ω, 100 Ω or 300 Ω
Accuracy	±0.5%
Floating Voltage	≥ 10 Vpk
Rated Load Impedance	
Balanced Output	600 Ω
Unbalanced Output	300 Ω

Frequency	
Range	3 Hz to 300 kHz
Accuracy	±2%
Resolution	15%

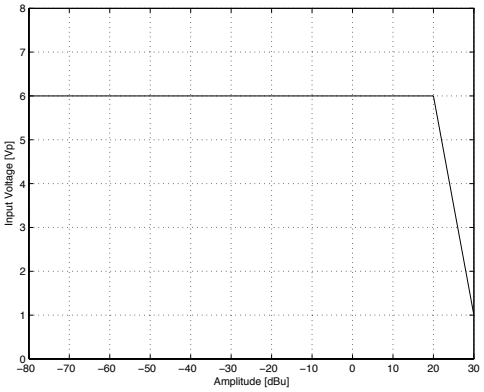
Amplitude	
Range	
Balanced Output	−80 dBu to +30 dBu [77.46 μVrms to 24.50 Vrms]
Unbalanced Output	−86.02 dBu to +23.98 dBu [38.73 μVrms to 12.25 Vrms]
Accuracy	±0.05 dB [±0.58%] at 1 kHz
Flatness	
3 Hz–30 kHz	±0.1 dB [±1.2%] relative to 1 kHz
3 Hz–300 kHz	±0.5 dB [±5.9%] relative to 1 kHz
Resolution	0.1 dB [1.2%]

Residual Distortion And Noise	
Individual Harmonics	
20 Hz–20 kHz	≤ −140 dBc [0.00001%]
3 Hz–300 kHz	≤ −100 dBc [0.001%]
THD+N	
20 Hz–20 kHz	see graph below; for unbalanced output reduce amplitude by 6.02 dBu.

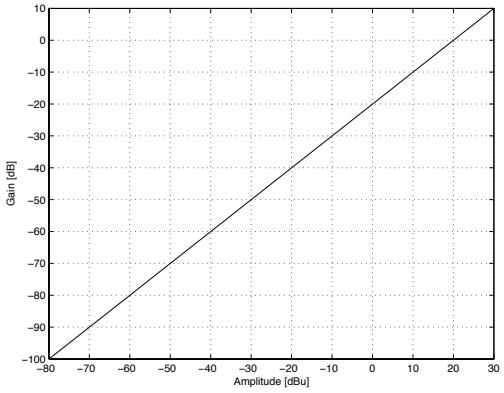


Settling Time	
3 Hz–300 kHz	≤ 10 sec to 0.1 dB [1.2%] of final value after frequency change
30 Hz–300 kHz	≤ 1 sec to 0.1 dB [1.2%] of final value after frequency change

Mix Input	
Input Impedance	$\geq 10\,\mathrm{k}\Omega$
Rated Input Amplitude	see graph below; rated input amplitude is given as function of oscillator amplitude setting. For unbalanced output reduce amplitude by 6.02 dBu.



Gain	see graph below; gain is given relative to main output and as function of oscillator amplitude setting. For unbalanced output reduce amplitude by 6.02 dBu.



Gain Accuracy	± 0.05 dB [$\pm 0.58\%$] at 1 kHz
Flatness	
3 Hz–30 kHz	± 0.1 dB [$\pm 1.2\%$] relative to 1 kHz
3 Hz–300 kHz	± 1 dB [$\pm 12\%$] relative to 1 kHz
Sync Output	
Output Impedance	$\leq 100\,\Omega$
Floating Voltage	≥ 5 Vpk relative to main output common
Rated Load Impedance	$2\,\mathrm{k}\Omega$
Amplitude	+4 dBu [1.228 Vrms], ± 1 dB [$\pm 12\%$]

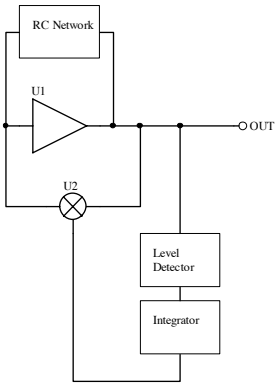


Figure 2.1: Conceptual RC oscillator schematic.

of potentially considerable amplitude settling time after a frequency change and the lack of inherently accurate frequency setting. Early RC oscillators have employed amplitude stabilisation by means of a lamp or thermistor [2][3][4][5]. These amplitude stabilisation schemes result in long amplitude settling, high low-frequency distortion and a considerable level temperature coefficient and are not considered further. Figure 2.1 shows a conceptual diagram of a RC oscillator with linear amplitude control. The key elements involved are the RC filter network, an amplifier (usually several are needed for a practical implementation), a level detector, an integrator and a multiplier. The level detector senses the actual amplitude and outputs an error voltage which is the difference to the nominal oscillator amplitude. This error voltage is fed to the integrator stage whos high DC gain ensures low steady-state level error. The output of the integrator controls a multiplier; by adjustment of the multiplier gain the Q of the filter is enhanced or reduced which results in growing or decaying oscillator amplitude. If the Q is adjusted to infinity the amplitude is stabilised. However because of inevitable small parameter changes which occur in the RC filter network, the amplifiers or the multiplier during operation of the oscillator continuous amplitude stabilisation is necessary.

There are four main distortion contributions in a RC oscillator with linear amplitude control [6]:

- Distortion from the amplifiers; this contribution typically increases with frequency due to decreasing loop gain and the approaching of large-signal bandwidth limitations. Particularly with integrated circuit amplifiers significant low-frequency distortion from thermal effects may be observed though [8][9]. Also distortion induced from the amplifier supply currents may be an issue [9][10].

- Distortion from residual ripple of the level dector which modulates the output amplitude. Low pass filtering of the ripple is not possible to an arbitrary degree as the settling time of the oscillator level will be affected—at some point amplitude stability might even be entirely lost. Depending on the level detector architecture the ripple may show an increase at low and/or high frequencies.

- Distortion from nonlinearity of the multiplier. Depending on the multiplier implementation its distortion characteristics may be substantially frequency independent or rise either at low and/or high frequencies. Additionally the distortion contribution may be a strong function of multiplier output voltage level (i.e. the integrator output voltage), which in turn is typically frequency dependent.

- Nonlinearity in the passive components used for the RC network. This is the very fundamental limitation in distortion performance of RC oscillators, which can only be addressed by parts choice and possibly the reduction of operating level. Typical distortion sources in passive components are their voltage coefficient, thermal self-modulation (or power coefficient) and nonohmic series resistance from end contacts [9][11]. Also switches used for frequency and level setting may introduce nonohmic resistance which effectively appears in series with the passive components.

The realisation of the distortion levels intended in this design is only possible if all four of the above listed contributions are reduced to very low levels.

2.3 RC Oscillator Topologies

There are several RC oscillator topologies which differ in their suitability for a low distortion implementation. In particular notable is their varying ability to suppress distortion from level detector ripple and multiplier nonlinearity by inherent low pass filtering. This has been thoroughly analysed by Hofer in [12] where he discloses the state-variable filter as the most suitable topology with this respect. In addition to this the state-variable topology uses all operational amplifiers in inverting mode; this prevents distortion from common-mode input swing [13][14][15] as the inputs are invariably operated at zero input voltage. The state-variable topology was hence chosen for this design.

2.4 Hardware Concept

For ease of design and performance verification of the various oscillator subcircuits and also to allow for later developments it was decided to employ a motherboard-daughterboard concept. The motherboard holds the components of the main oscillator loop (i.e. the state-variable topology), associated local power supply and the logic circuits for frequency switching. The operational amplifiers, the level detector and the multiplier are implemented on a daughterboard each. It has also been allowed for that the motherboard may accommodate an output stage daughterboard, although the design of this is not part of this thesis.

Chapter 3

Main Oscillator Loop

In the following text we will first of all discuss basic considerations (such as frequency setting) for the state-variable oscillator topology. Later a new measurement technique for the evaluation of distortion in passive components is introduced. Also considered is the implementation of the switches in the main oscillator path and the detailed implementation of the overall state-variable ring.

3.1 Basic State-Variable Oscillator Considerations

Figure 3.1 depicts a basic state-variable oscillator with linear amplitude control. U1–U3 and associated feedback networks form the main oscillator loop. The level detector compares the oscillator amplitude with the voltage reference V1 and feeds an error voltage to the integrator amplifier U4. The integrator stage provides the control voltage for the multiplier U5 which is characterised by its gain constant k. R6 introduces a zero in the integrator response which is necessary for amplitude stability [16]. For the level detector topology used for this oscillator (see chapter 5) it can be shown that the gain of the integrator for frequencies above the zero must be $\frac{-1}{\pi \cdot \mathrm{V1}}$ [17] for optimum settling time.

To keep both noise and distortion contribution of the main signal amplifiers U1–U3 low it is good design practice to operate them at approximately equal output voltage. This constrains $\mathrm{R1} = \mathrm{R4}$ and $\mathrm{R2} \cdot \mathrm{C1} = \mathrm{R3} \cdot \mathrm{C2}$. The oscillation frequency f_0 is then given as follows:

$$f_0 = \frac{1}{2\pi \cdot \mathrm{R2} \cdot \mathrm{C1}} \tag{3.1}$$

Frequency setting must hence be accomplished by simultaneous adjustment of R2/R3 and C1/C2. To minimise thermal resistor noise it is necessary to adjust the capacitors for the range switching (e.g. in decadic steps)

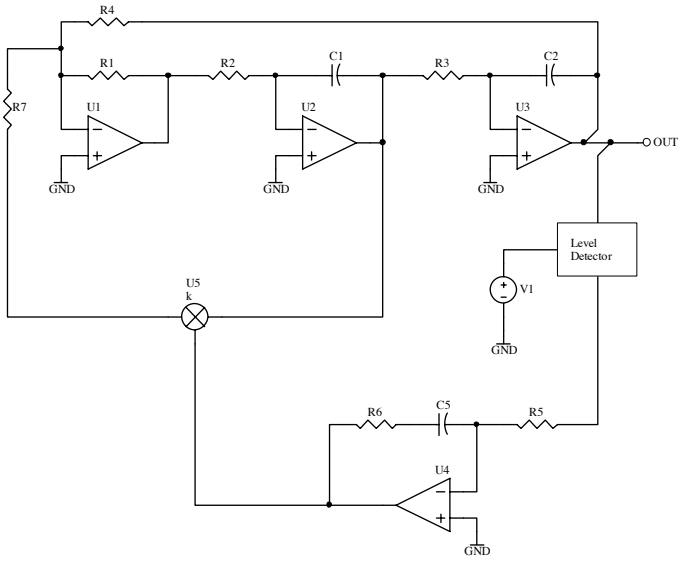


Figure 3.1: Conceptual state-variable oscillator.

and the resistors for frequency setting within one range (e.g. with a binary weighted resistor network). Fine-tuning can be done by adjusting either R1 or R4; as the required range is low this does not result in significant noise or distortion contribution from U1. The oscillation frequency is then given by [18]:

$$f_0 = \frac{\sqrt{\frac{\mathrm{R1}}{\mathrm{R4}}}}{2\pi \cdot \mathrm{R2} \cdot \mathrm{C1}} \tag{3.2}$$

To reach the frequency resolution and accuracy specifications as given in chapter 2 it was decided to use a 10 bit binary weighted resistor network in the integrator stages. Furthermore capacitor tolerances are trimmed out by selecting R1 for each range. Resistor tolerances are insignificant as 0.1 % parts are used.

An important properity of an RC oscillator with linear amplitude control is the multiplier authority, i.e. the range over which the multiplier can control the Q of the oscillator circuit. It is given by the product $\frac{k}{\alpha}V_{C_{max}}$ where k denotes the multiplier gain constant, α the decoupling factor of the multiplier (i.e. $\frac{\mathrm{R7}}{\mathrm{R1}}$) and $V_{C_{max}}$ the maximum control voltage. To reduce distortion and noise contribution from the multiplier it is convenient to keep the multiplier authority low. However this cannot be taken too far as for proper amplitude stability after settling the multiplier must be kept within its linear range, i.e. the control voltage must not exceed certain limits. The control voltage needed to adjust the Q of the state-variable ring to

infinity (which is the value required to held the amplitude constant) varies considerably with frequency and depends mainly on capacitor losses and finite loop gain of the amplifiers in the integrator stages [19].

3.2 Passive Components

The resistors and capacitors used in the feedback network of the three amplifiers of the state-variable oscillator loop must be carefully chosen to minimise their distortion contribution. [11][20][21][22][23][24][25][26][27] have investigated distortion in passive components but the measurement resultion has been limited to less than $-130\,\mathrm{dBc}$, making the results insufficient for this design. To evaluate passive components at distortion levels of less than $-140\,\mathrm{dBc}$ a new measurement procedure was derived which will be presented below.

Previous measurement procedures have employed a direct measurement where the device under test is connected in series with a voltage divider resistor. This combination is then driven by an oscillator and the distortion of the voltage across the device under test measured. The resolution of such a measurement is limited by the oscillator and distortion analyzer contribtion; furthermore the resistor in series with the device under test introduces another uncertainity. In particular the contribution of the oscillator and the analyzer is not easily reduced to negligible levels; hence some form of cancellation is needed. This is achieved in the new measurement method by two consecutive measurements. The first measurement is equivalent to the arrangement as described above. For the second measurement the device under test is replaced with a series-parallel combination of four components, each of the same type as the device under test. By subtraction of the two measurements the contribution of the oscillator, analyzer and the voltage divider resistor is cancelled out. As the nominal impedance of the series-parallel connected array is equal to that of a single component the operating conditions for analyzer and voltage divider resistor is kept constant, hence their distortion contribution may be expected to be equivalent.

The distortion in most passive components (that excludes such with explicit polarity such as electrolytic capacitors) can be quite accurately modelled by a constant voltage coefficient for the operating conditions observed in this oscillator design; in other words the impedance Z of the device under test is given as:

$$Z = (1 + \kappa\,|U|) \cdot Z_0 \tag{3.3}$$

Where κ denotes the voltage coefficient, U the voltage across the device under test and Z_0 the nominal impedance of the device under test for $U = 0$.

It can be shown by simulation or the use of Taylor series that such behaviour results in predominantly 3rd harmonic distortion if the component is exposed to a pure AC voltage (i.e. with zero DC bias). Also it can be shown that under such conditions the absolute level of distortion reduces four times if the AC level is reduced two times.

For the second measurement of the new measurement procedure the AC voltage across the components is halfed due to the series connection of two components; distortion will hence be one fourth that of a single component. From this it is seen that the difference of the two measurements will show $1 - \frac{1}{4}$ of the distortion of the single component which corresponds to about $-2.5\,\mathrm{dB}$.

To realise the theoretical cancellation of oscillator, analyzer and voltage divider resistor residual contribution several considerations are necessary. First of all the measurements cannot be carried out by means of a THD+N measurement; the noise contribution cannot be subtracted out the same way as the distortion contribution as it is not correlated between the two measurements. Spectrum analysis techniques (e.g. FFT) must be used to separate noise and distortion. Second the two measurements must be phase-aligned for correct cancellation. This has been realised by digitising both analyzer input and notch filter output waveforms and subsequent digital signal processing in Matlab. Furthermore it must be assured that the distortion contribution of oscillator, analyzer and voltage divider resistor is time invariant, i.e. consistent for both measurements. This is verified by a third measurement using the series-parallel connected array which is carried out before the measurement of the single component. By subtraction of the two measurements with the series-parallel connected array the consistency of the distortion contribution is sensed. If the distortion contribution is consistent no harmonic distortion will be observed.

Using this new measurement technique it was found that (at 1 kHz and for a level of +20 dBu across the device under test) measurement of distortion levels at $-140\,\mathrm{dBc}$ is possible with a consistency of $\pm 1\,\mathrm{dB}$; $-150\,\mathrm{dB}$ is possible with somewhat reduced consistency. As the actual operating level of the passives used in the oscillator loop is $+14\,\mathrm{dBu}$ (corresponding to 12 dB less 3rd harmonic distortion contribution) it can hence be assured that a component contributes insignificant distortion to the overall oscillator.

Several capacitor types were evaluated using the new measurement technique (see section A.1 for the actual measurement results). From the measured capacitors polypropylene and polystyrene film capacitors showed consistently low distortion levels at $-150\,\mathrm{dBc}$; ceramic C0G/NP0 capacitors

showed a consistent distortion floor of −130 dBc or less.[1] The use of ceramic C0G/NP0 capacitors however is advantageous because they offer very low temperature coefficient and no significant sensitivity to humidity. It was hence decided to use series-conntected capacitors to reduce the operating level to +8 dBu; hence a distortion reduction of 24 dB compared to the measurement level of +20 dBu may be expected, corresponding to a distortion contribution of at most −154 dBc.

Of the measured resistors metal foil and wirewound parts (see section A.2) showed distortion levels of −150 dBc; for economical reasons their use must be avoided however. Metal film parts gave distortion levels of less than −140 dBc at +20 dBu; with the expected 12 dB reduction this would provide adequate performance for the oscillator design.[2] However so far we have only considered distortion from voltage coefficient. Resistors also show distortion from thermal self-modulation (or power coefficient); due to the nonzero temperature coefficient the resistance value will be modulated with signal voltage as the instantaneous power dissipation varies. Because of the thermal capacitance of the resistor the resistance shows lower modulation at high frequencies; at the measurement frequency of 1 kHz thermal self-modulation can be assumed to be entirely negligible. At very low frequencies (below the thermal time constant) however the modulation may be assumed to happen instantaneously and the instantaneous resistance value R is given as follows:

$$R = (1 + \rho R_\theta \frac{U^2}{R_0}) \cdot R_0 \tag{3.4}$$

Where ρ denotes the temperature coefficient, R_θ the thermal resistance, U the instantaneous voltage across the resistor and R_0 the nominal resistance at $U = 0$.

Data on the thermal mass of standard resistors is not easily found; [30] gives a value of 110 K/W for a resistor rated at 0.25 W. If we assume a temperature coefficient of 100 ppm/K it is easily shown by simulation that a 2 kΩ resistor operated at +14 dBu will exhibit gross distortion of about −90 dBc. Information on thermal capacitance appears to be entirely unavailable for metal film parts; [31] indicates that thermal self-modulation of precision wirewound resistors shows a time constant in the order of 500 s.

[1] Some parts also showed 2nd harmonic distortion at low level; it is not yet clear if this is uncancelled oscillator/analyzer residual or actual capacitor distortion.

[2] The measurements have been carried out on 1 kΩ resistors. Resistors with significantly higher values may be expected to show somewhat higher voltage coefficient [27][28][29]. However in this particular oscillator design high value resistors are only used in the less significant bits of the binary weighted networks, and their value is well below 1 MΩ. Hence their distortion contribution remains insignificant.

This result however is hardly applicable to the physically much smaller metal film resistors. Some preliminary measurements were carried out on a 0.5 W carbon composite resistor indicating a time constant of 40 s. Including this time constant in the model gave a distortion residual of −135 dBc at 3 Hz. However it is difficult to assure that metal film parts will show very similar thermal behaviour and that the first-order thermal model applied is sufficient for accurate modeling of distortion; detailed insight must be left for future research.

Unfortunately direct measurement of distortion from thermal self-modulation was not possible because at low frequencies the residual of the available oscillator source (Audio Precision SYS-2722 [7]) is both high and also quite unsteady which prevents accurate cancellation. To ensure negligible thermal distortion for this oscillator design it was decided to use resistors with a temperature coefficient of 15 ppm/K. Furthermore each resistance value in the main oscillator loop was implemented by a pair of series-connected resistors of approximately equal value to reduce the power dissipation.

Consideration must also be given to the low pass action of the integrator stages; by this harmonic distortion from the resistors in the feedback network of the integrators is attenuated. For the resistors of the second integrator (i.e. the amplifier which forms the low pass output of the state-variable oscillator) the actual figure is shown to be 8.52 dB at the 3rd harmonic by simulation. Resistor distortion in the first integrator (band pass output) or the inverter (high pass output) is attenuated by 18.06 dB and hence less significant. As shown above voltage coefficient distortion of a single resistor has been measured at less than −140 dBc for an AC voltage of +20 dBu. As the actual operating level is 6 dB lower and two series-connected resistors are used resulting distortion is 24 dB lower; after consideration of the integrator attenuation an overall contribution of −172.5 dBc can be estimated. At lower frequencies thermal self-modulation occurs but the effect is assumed to be negligible at the frequencies of interest.

3.3 Switches

For range and frequency switching a considerable amount of switches is needed. The on-resistance of the switches necessarily appears in series with the passive components, hence it must show a sufficiently low value and a sufficiently low voltage coefficient for negligible distortion contribution. Furthermore the off-impedance must be high and again have a low voltage coefficient to avoid distorted feedthrough. FET switches are convenient as they offer low power consumption, low cost, high reliability and small size. However both their on-resistance and off-capacitance shows consider-

able voltage coefficient [32][33]; some improvement is possible by linearisation [18][32] and the use of series-shunt arrangements [27]. However for the demanding specifications of the oscillator design presented in this thesis it was considered necessary to further reduce the distortion contribution of the switches. Hence relays were chosen as switching element; their on-resistance and off-impedance are near-ideal in the frequency range of interest.

3.4 Implementation

The detailed drawings of the main oscillator loop circuit are shown in figure 1.1–1.10 of the schematic diagram document. Figure 1.2 depicts the high pass amplifier of the state-variable oscillator. K0202–K0206 switch the resistors R0213*–R0222* pairwise in parallel with the nominal feedback resistor network consisting of R0204 and R0205. The resistors are selected for each range for frequency trimming. R0209 injects the multiplier output into the summing node of U0201; in the highest frequency range (30–300 kHz) R0210 is switched in parallel to increase the multiplier authority. Also summed into the high pass amplifier are signals from the startup/mute and Q trimming circuit which will be discussed later.

Figure 1.3 shows the first integrator stage. R0301–R0320 and K0301–K0310 form the binary weighted resistor network; range switching is done by K0311–K0315. The unused feedback capacitors are connected to ground by R0321. R0322* is included to dampen the Q-enhancement of the overall oscillator loop which occurs towards the highest frequencies because of finite amplifier loop gain. The second integrator stage (see figure 1.5) is equivalent to the first and a repeated discussion is omitted. The amplifier which inverts the signal of the band pass output is depicted in figure 1.4 of the schematic diagram document. The output of this amplifier is fed to the multiplier and also used to mute the oscillator. Also shown on this schematic diagram are the resistors (R0407*–R0416*) and relays (K0401-K0405) which are used to pre-trim the Q of each frequency range to infinity. This allows best headroom in the integrator stage as the nominal control voltage will be zero.

Startup and muting of the oscillator is provided by the circuit as shown in figure 1.6. For startup Q0602 is turned on which connects the band pass output to the summing node of the inverter through resistor R0601. This greatly enhances the Q of the state-variable filter which results in fast amplitude growing. Q0601 acts as shunt switch to minimise feedthrough (which might carry harmonic distortion because of voltage-dependent junction capacitance of Q0602) during normal oscillator operation; the control signals to switch the JFETs are provided from the level detector daughterboard which senses a low amplitude condition. Muting of the oscillator is done by a similar arrangement which is however fed from the inverted band pass

signal. The according switches are formed by Q0604 and Q0605. Q0606 acts as level shifter for the level detector board to indicate that the oscillator is operating in the highest frequency range. Also shown on this schematic are light-emitting diodes (D0605 and D0606) to indicate muting and amplitude settling of the oscillator.

Control of the binary weighted resistor networks in the integrator stages is provided by the logic circuit as shown in figure 1.7. U0701–U0703 encode the rotary switch position into a binary format which is sent to two nonvolatile memory blocks U0704 and U0705. The output of the memory is level-shifted by the transistors shown in figure 1.8 to drive the relays.

The discrete operational amplifiers are powered from $\pm 15\,\mathrm{V}$ supplies. These are provided by discrete series voltage regulators which are shown in figure 1.9. These regulators are complementary designed (only the positive regulator will be discussed in detail) and achieve exceptionally low noise, low output impedance, high ripple rejection and excellent load regulation by several means. First of all the voltage reference U0901 is bootstrapped to the output through R0902 which makes its finite impedance negligible; startup for this arrangement is given by D0902 and R0903. Also the considerable voltage noise from the voltage reference is filtered by R0903 and C0902. The input differential pair (Q0901/Q0902) is cascoded by Q0903 and Q0904 which eliminates Early effect and results in better ripple rejection and output impedance. The input differential pair is followed by a current mirror (Q0905 and Q0906); the output current of the current mirror in turn drives two emitter followers (Q0908 and Q0909) and finally the common-emitter stage Q0910 which acts as main pass transistor. This topology results in very high open loop gain and low output impedance; C0903 acts as compensation capacitor and simultaneously ensures low output impedance at high frequencies. Q0907 provides output current limiting. The series regulators for the $\pm 12\,\mathrm{V}$ rails (relay supply) and the $5\,\mathrm{V}$ rail (logic supply) are shown in figure 1.10; standard voltage regulators are used for these less critical voltages.

The overlay print of the printed circuit board is depicted in figure 1.11 of the schematic diagram document.

Chapter 4

Operational Amplifier

In this chapter we will discuss the operational amplifier used in the main oscillator loop. After presentation of the performance requirements—particularly with respect to distortion—we will consider the actual implementation. A new amplifier topology is presented which allows realisation of an operational amplifier with very low distortion contribution along with good noise and DC precision performance.

4.1 Performance Requirements

The main requirement for the operational amplifiers used in the direct signal path is that they must contribute negligible distortion. According to the specifications defined in chapter 2 the level of the individual harmonics of the oscillator output shall not exceed $-140\,\mathrm{dBc}$ for the frequency range of $20\,\mathrm{Hz}$ to $20\,\mathrm{kHz}$ and $-100\,\mathrm{dBc}$ from $3\,\mathrm{Hz}$ to $300\,\mathrm{kHz}$. Hence it is desirable that the amplifier contribution is at least $20\,\mathrm{dB}$ below these figures. At the distortion levels intended it is also very important that the amplifier does not generate a magnetic field which carries harmonic distortion of the output signal. Otherwise mutul inductance between the feedback network and the operational amplifier will couple this distortion into the oscillator output [9][10]. In particular this means that the power supply currents of the amplifier must not contain significant levels of harmonic distortion.

While the main goal of the oscillator design presented in this thesis is low harmonic distortion it is also desirable to keep residual noise low. To minimise noise the feedback networks of all amplifier stages have been kept low. The total source impedance seen by the amplifier ports ranges from about $300\,\Omega$ to $3\,\mathrm{k}\Omega$ at frequencies up to that of the oscillation; for higher frequencies the source impedance falls towards zero for the integrator stages because of the feedback capacitor. To keep the noise contribution of the amplifiers low they should hence have low noise figure for source impedances

from 300 Ω to 3 kΩ. This corresponds to a voltage noise density of less than $3\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ and a current noise density of less than $2\,\mathrm{pA}/\sqrt{\mathrm{Hz}}$.

Although the operational amplifier needs to be mainly optimised for excellent AC performance DC precision needs some consideration as well. The level detector used in the leveling loop senses the peak voltage of the sinusoidal output signal (see chapter 5). Any DC voltage present at the output of the second integrator stage will lead to an equivalent AC level error as the peak detector cannot discriminate AC signal against DC content. While an oscillator amplitude error from a static operational amplifier offset voltage is easily trimmed out corresponding drift will result in AC level shift with temperature. Also bias currents flowing through the resistor network of the integrator stages will cause frequency-dependent level shifts because the resistor network is switched for frequency control.

The supply rails of the amplifier will carry some ripple and noise due to finite power supply performance. To avoid that ripple and noise superpose the oscillator output signal the operational amplifier should have high power-supply rejection for frequencies at least up to 1 MHz.

Last but not least it is important that the open-loop gain of the amplifier be high. While high open-loop gain typically correlates positively with low distortion and high power-supply rejection high open-loop gain is also necessary to make the oscillator well-behaved at high frequencies. Finite open-loop gain causes additional phase shift in the integrator stages (i.e. the phase shift at the desired oscillation frequency is above $\frac{1}{2}\pi$); at high frequencies this additional phase shift may exceed the losses from the integrator capacitors which cause negative phase shift. Under such conditions the oscillation will build up even with the leveling loop disabled, and amplitude control will require high signal levels from the multiplier. This is undesirable because it requires a low multiplier decoupling factor α which emphasises multiplier distortion contribution. As a lower limit the open-loop gain at 300 kHz should be 50 dB.

4.2 Amplifier Topology

At the time of writing there is no integrated circuit operational amplifier available which would offer sufficiently low distortion levels according to the requirements given above. Significant distortion improvements are possible by the use of topologies which use multiple series-connected amplifiers (see e.g. [34]); however these topologies still suffer from substantial distortion of the power supply currents as IC amplifier invariantly use class B output stages which draw half-wave rectified power supply currents. It was hence decided to design a discrete operational amplifier which uses a class A output stage. Class A output stages draw very little harmonic content from the

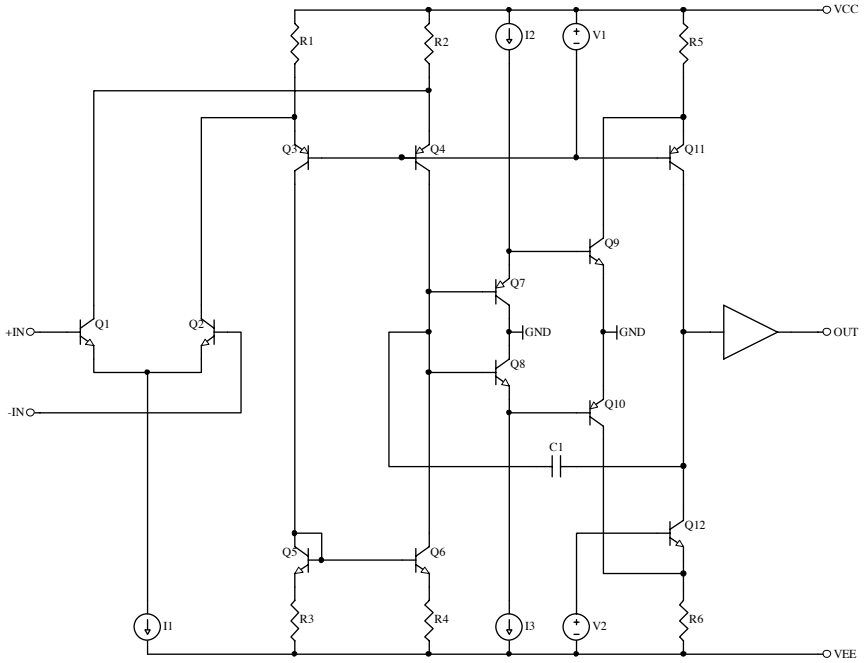


Figure 4.1: Simplified schematic diagram of the new operational amplifier circuit.

power supply and additionally offer freedom from crossover distortion [10] which will greatly improve the basic distortion performance of the amplifier.

Several known amplifier topologies were investigated by simulation and actual measurements; while all investigated topologies provided very low distortion at least up to 20 kHz if appropriatly implemented there were substantial deficiencies either regarding power-supply rejection, complexity, overload behaviour or stability. To achieve all desired performance aspects a new amplifier topology was derived which is first published here. In the following we will briefly discuss the new amplifier topology.

A simplified schematic of the new operational amplifier is shown in figure 4.1. The topology has two gain stages; the first stage consists of a standard differential transistor pair (Q1 and Q2) which acts as a transconductance stage. The differential output current of the input stage is fed to a folded cascode consisting of Q3 and Q4. This cascode acts as level-shifter to the current mirror (Q5, Q6, R5 and R6) which finally performs the differential-to-single-ended conversion of the first stage.

The second stage comprises a ground-referenced complementary common-emitter stage (Q9 and Q10). The two output currents of this stage are summed by the complementary folded cascode transistors Q11 and Q12. Two emitter followers (Q7 and Q8) are added to increase the gain of this

stage. Miller compensation is provided by C1 to roll-off the open-loop gain towards high frequencies. Compared with prior art amplifiers this new circuit arrangement for the second stage has several advantages; first of all the input summing node of the second stage (at the bases of Q7 and Q8) is held at virtual earth potential because of the grounded emitters of Q9 and Q10. For conventional amplifier topologies this node connects to one (or sometimes effectively to both) supply rails. As the Miller compensation capacitor references the output of the amplifier to the potential of the second stage input summing node this results in decreasing power supply rejection towards high frequencies [10][35]. The virtual earth input potential of the new amplifier stage avoids this and therefore provides much better power supply rejection.

Furthermore the complementary nature of this stage provides at least rough cancellation of even order harmonics. Distortion is further reduced because the common-base transistors Q11 and Q12 greatly reduce the influence of Early effect and voltage-dependent collector-base junction capacitances in Q9 and Q10. Slew-rate limitations of the second stage are almost entirely absent because of the push-pull nature of the circuit arrangement—the collector currents of Q11 and Q12 have no upper first-order limit which provides excellent drive capability for the compensation network and the output stage. Temperature stability of the bias conditions is ensured because the V_{be} drift of Q7/Q9 and Q8/Q10 approximately cancel. The output of the second stage is buffered from the amplifier load by a conventional unity-gain output stage.

From now on we will consider the full schematic diagram of the new operational amplifier as depicted in chapter 2 of the schematic diagram document. For the realisation of the amplifier a four-layer printed circuit board is used; this allows the generous use of ground planes which reduces parasitic inductance and capacitive crosstalk. The overlay print of the printed circuit board is also shown in the schematic diagram document.[1] In the following sections we will discuss several implementation details and present actual measurements of the circuit.

4.3 Biasing and DC Precision

Biasing of the amplifier is provided by light-emitting diodes D8 and D9. The forward current is set comparatively high at 5 mA; this reduces the dynamic impedance of the diodes and minimises their voltage noise. The

[1] The overlay print shows several components which are not found in the schematic diagram. These parts were included for circuit optimisation but are not used in the final implementation.

forward voltage is approximately 1.58 V and very consistent amongst different specimen [36]. The temperature coefficient of the forward voltage is approximately equal to that of a base-emitter junction of a bipolar transistor [37]. Hence the collector currents of Q3, Q13 and Q14 are largely independent of temperature.

The voltage offset of the amplifier is trimmed by R11; the values shown for R7–R11 give a trim range of sligthly more than ±6 mV which is sufficient to trim a V_{be} difference encountered in Q1 and Q2 without any matching of these transistors. For a bipolar input stage trimming the voltage offset to zero conveniently adjusts the temperature drift of this figure to zero as well [38]. However second-stage contributions may introduce errors. To reduce these in this operational amplifier several means have been employed. First of all the common-base transistor Q6 adjusts the collector voltage of Q4 to a value which is near-equal to the collector voltage of Q5. This minimises offsets from thermal and Early effect in Q4 and Q5. Furthermore Q6 partially cancels the base current errors of Q7 and Q8. The large value of R12 and R13 renders V_{be} differences between Q7 and Q8 negligible. As precision 0.1 % parts are employed for these two resistors the current mirror ratio is close to unity which further reduces several second-order drift terms. To reduce sensitivity to thermal gradients Q1 and Q2 are located in close proximity and thermally coupled by means of a heat shrink. Although no explicit thermal coupling is used the transistor pairs Q4/Q5 and Q7/Q8 are located in close proximity to aid equithermal operation.

The bias current of Q2 is cancelled by the selected resistor R6. D3–D5 provide a reference voltage with approximately the same temperature coefficient as the h_{FE} of a bipolar transistor [39]. As the tail current load of the input stage (formed by Q3, R3 and D9) is temperature compensated the residual input bias current (i.e. the sum of the Q2 base current and the cancellation current flowing through R6) remains to a good extent independent of temperature. R5 and C1 filter noise from the diode string D3–D5 as well as ripple from the supply rails. This bias current cancellation scheme has the great advantage that it does not add—unlike most circuits used in integrated circuit operational amplifiers—significant current noise; it has been verified that the added current noise is less than 10 %.

Nine specimen of this discrete operational amplifier have been built. As shown in figure 4.2 the magnitude of the inverting input bias current is kept below 100 nA; as the typical uncancelled input bias current is 4 μA the used input bias cancellation offers an inprovement of at least 40 times. The maximum source resistance seen by the inverting input is about 3 kΩ. Hence the maximum offset from input bias current is less than 300 μV which causes a negligible oscillator amplitude error. As the amplifiers are only used with

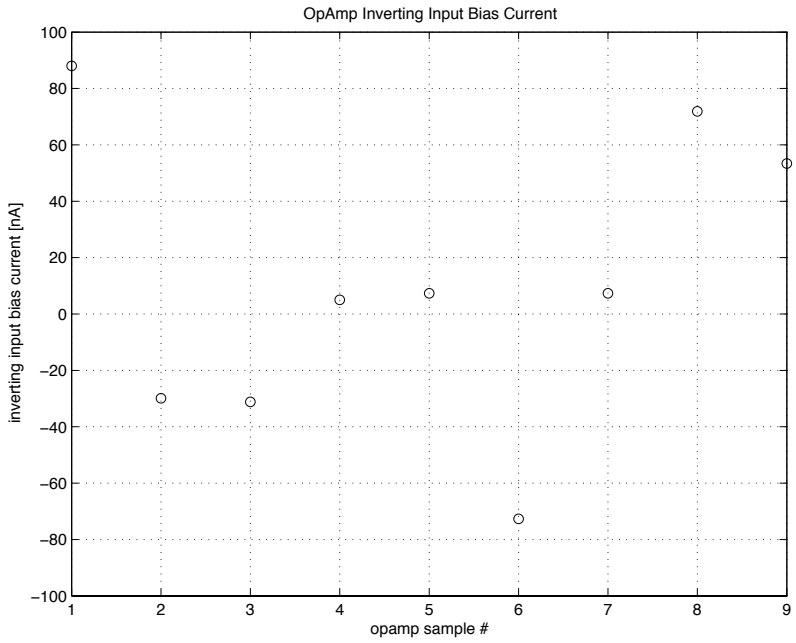


Figure 4.2: Inverting input bias current for the nine built operational amplifier specimen.

grounded noninverting input (i.e. as inverting amplifiers) there is no need to cancel the base current of Q1.

4.4 Output Stage

Q15 and Q16 form the complementary emitter follower output stage. The emitter resistors (R26 and R27) and R23 are selected for a quiescent current of 16 mA. This allows a class A peak output current of 32 mA which is sufficiently high for all amplifier configurations used in the oscillator. There is no explicit current limiting circuit used to minimise complexity. R28, R29, C11 and C12 form two low pass filters which localise the AC currents drawn by the output stage. Even though the output stage is operating in class A the collector currents carry significant amounts of harmonic distortion which might induce into the feedback network or any other nearby circuit element. As the filters greatly minimise the loop area of these currents the magnitude of the magnetic field is reduced accordingly.

The current gain and hence input resistance of the simple output stage is relatively low; furthermore the input resistance of the buffer shows some dependence on output voltage, which results in a dependence of amplifier open-loop gain on output voltage. At low frequencies this appears to be the

dominant distortion mechanism of the operational amplifier. More complex buffer stages (such as the complementary folded darlington configuration which is widely used in integrated circuit operational amplifiers [40]) could substantially reduce this error; however their lower bandwidth would necessitate higher compensation and hence worse high-frequency distortion performance.

4.5 Compensation and Slew-Rate

For lowest distortion and highest possible open-loop gain the operational amplifier uses a complex compensation scheme. First of all the transconductance of the input stage is shaped by R1, R2, L1 and L2. At frequencies above 1.32 MHz the impedance of L1 and L2 becomes insignificant and R1/R2 provide emitter degeneration for the input transistors Q1 and Q2. The resulting transconductance of the input stage is approximately 2.48 mS. For frequencies below 46.3 kHz L1 and L2 effectively short the emitters of Q1 and Q2 which results in a transconductance of 73.1 mS. The high transconductance at low frequencies is desirable for low DC offset, low noise and low distortion contribution from the second stage. The low transconductance at high frequencies allows the use of a small Miller compensation capacitor which improves the high-frequency linearity of the amplifier.

The Miller compensation is implemented as C-R-C-R-C network (R19, R20 and C4–C6). The first resistor (R19) is connected to ground to provide the open-loop gain with a second-order response [10]; this results in very high mid-band open-loop gain. The second resistor (R20) connects to the output of the amplifier and forms a transitional Miller compensation loop [41]. By means of this arrangement the Miller loop includes the output stage at low frequencies; towards higher frequencies the Miller loop is localised around the second stage for stability reasons. At low frequencies the current to drive the compensation network is hence provided by the output stage; this improves the linearity of the second stage as it reduces the AC magnitude of the collector current in Q9 and Q10. Further distortion improvement is achieved because the output stage expires more feedback for error correction, although due to the class A implementation the output stage contributes very little distortion anyway.

C2 and C3 are feed-forward capacitors which bypass the emitter followers Q9 and Q10 at high frequencies. This increases the phase margin of the Miller compensation loop and is necessary to prevent parasitic oscillation in the second stage. Similarly C7 improves the stability and slew behaviour of the second stage; the detailed mechanisms which cause this improvement must be left for future research though.

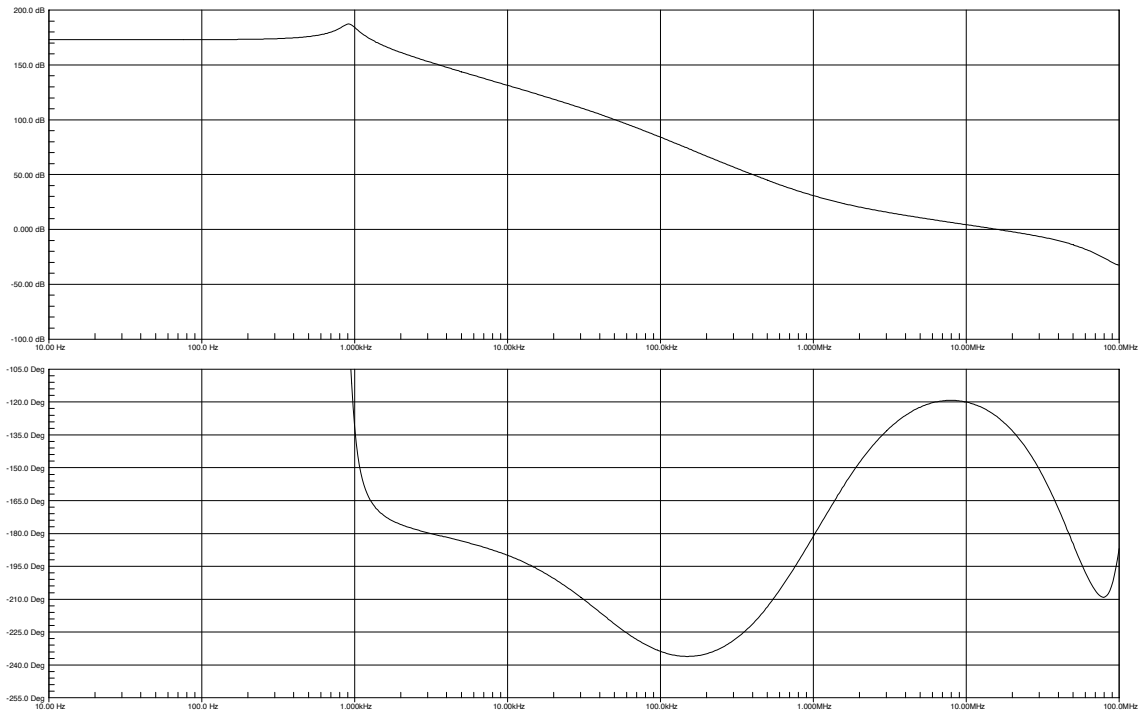


Figure 4.3: Open-loop gain and phase response of the new discrete operational amplifier.

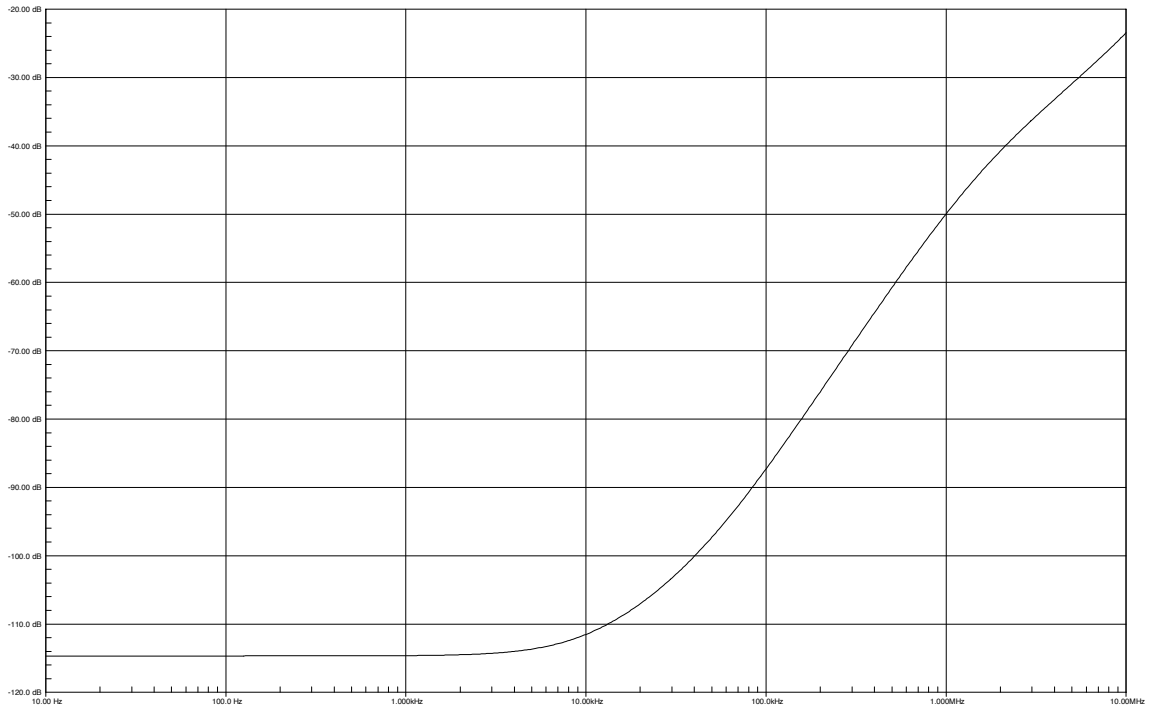


Figure 4.4: Positive power supply rejection.

The compensation scheme described above results in very high open-loop gain at signal frequencies while maintaining a unity-gain frequency of approximately 20 MHz. Figure 4.3 shows simulation results of the open-loop gain and phase response. It is seen that at 300 kHz the open-loop gain is about 57 dB which corresponds to a gain-bandwidth product of 212 MHz. At lower frequencies the gain-bandwidth product steadily increases well into the GHz range. Due to the higher-order compensation scheme the phase response exceeds π in a wide frequency range (about 3 kHz to 1 MHz). For stability the amplifier must hence be operated at a unity loop gain frequency above 1 MHz; this however is anyway the case for a typical state-variable oscillator implementation. Measurement of the open-loop gain and phase would be difficult to accomplish at the high gains involved. Hence only simulation results are shown here.

Figure 4.4 and 4.5 illustrate the supply rejection which is also closely related to the compensation scheme. Again only simulation results are shown; at low frequencies the supply rejection depends somewhat on resistor and transistor tolerances. It has been verified by a Monte-Carlo simulation that the low-frequency floor of the supply rejection is above 100 dB even for worst-case tolerances.

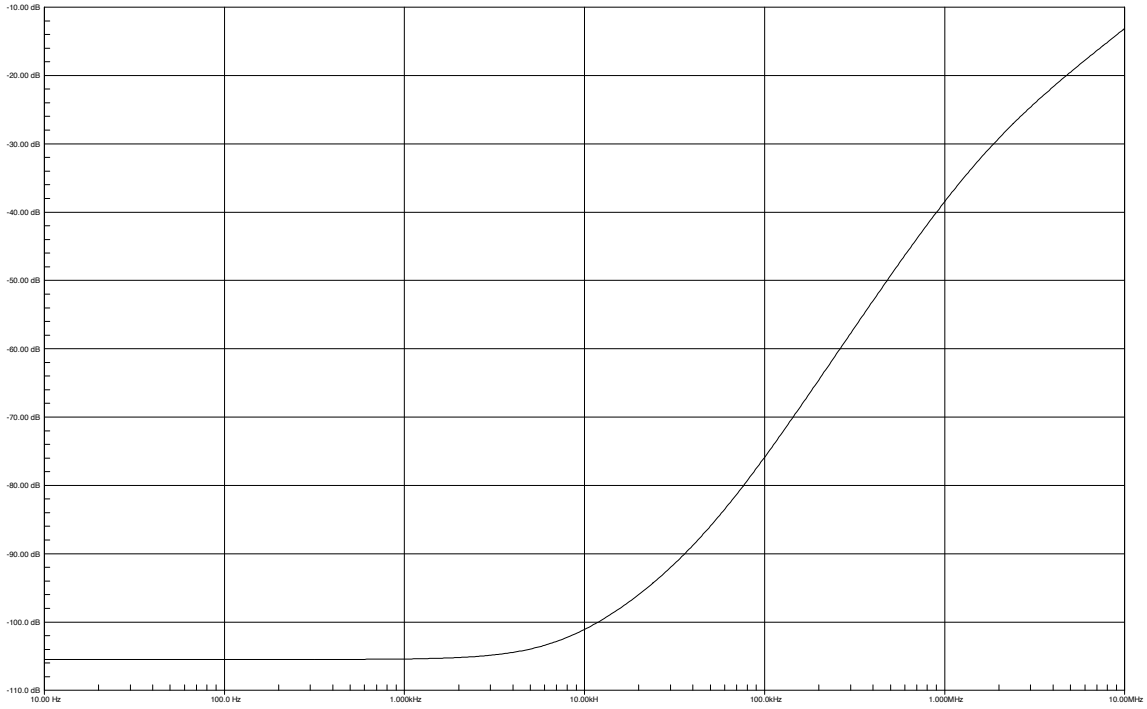


Figure 4.5: Negative power supply rejection.

The slew-rate of the amplifier is difficult to measure. This is because the higher-order compensation scheme necessitates the use of a rather high value of feedback capacitance for stability. This limits the small-signal bandwidth to a value lower than the theoretical large-signal bandwidth. However a slew-rate of $100\,\mathrm{V}/\mu\mathrm{s}$ has been verified which is well in excess of the actual requirements—at the nominal operating level of $+14\,\mathrm{dBu}$ the large-signal bandwidth extends beyond $4\,\mathrm{MHz}$. This underscores the excellent high-frequency linearity (which will be demonstrated by actual measurements in the following section) of the amplifier and is also advantageous to avoid latch-up conditions due to slew-rate limiting; if during transient conditions—which typically occur because of a range or frequency switch—an amplifier enters a slew-limited condition it will contribute excess phase to the overall state-variable ring. This might cause high-frequency oscillation which will further build up slew-rate limiting and hence result in latch-up [42]. However thanks to the excellent slew-rate performance of the new amplifiers this has not been observed in the oscillator design presented in this thesis.

4.6 Distortion Contribution

Direct measurement of the distortion contribution of the operational amplifier presented in this chapter is not possible as its distortion level is several orders of magnitude below that of available distortion analyzers. However operation of the amplifier at increased noise gain proportionally increases the distortion observed at the amplifier output due to reduced loop gain [13][15]. At 60 dB noise gain it is just possible to discriminate the distortion from the operational amplifier and the distortion analyzer (Audio Precision SYS-2722) for frequencies up to 30 kHz. For frequencies above 30 kHz the bandwidth of the operational amplifier limits the accuracy of the measurement and a noise gain of 40 dB needs to be chosen; however as the distortion contribution of the operational amplifier rises faster than that of the distortion analyzer meaningful measurements are possible nonetheless.

Figure 4.6 depicts the measurement results for the 2^{nd} and 3^{rd} harmonic. The level of the harmonics are referred to the output of an inverting integrator configuration with a time constant equivalent to the fundamental frequency; this corresponds to a noise gain of 0.97 dB for the 2^{nd} harmonic and 0.46 dB for the 3^{rd} harmonic and incorporates the actual configuration which is used for these amplifiers for the band pass and low pass output of the state-variable filter topology. The noise gain of the high pass output amplifier and the inverter following the band pass output is about 6 dB; however the distortion contribution of the high pass amplifier is low pass filtered by the two following integrator stages and the output of the inverter following the band pass output is additionally greatly attenuated through the multiplier path. Both amplifiers are hence negligible regarding their distortion contribution. The measurements were done at the nominal operating level of the oscillator (+14 dBu), with a 200 Ω output load and a source resistance at the noninverting amplifier input of 1 kΩ. The 200 Ω output load (corresponding to a peak output current of 27.45 mA) represents a worst-case condition as the output current of the actual opamp configurations is at least 5 % lower; it has been verified that lower output current results in lower distortion.

The 1 kΩ source resistance is used to mimic the source impedance present in the actual amplifier configuration; this is important because particularly at high frequencies the operational amplifier inputs draw distorted AC currents.[2] These currents flow through the source impedance where they superimpose their distortion on the main signal [10]. The maximum impedance

[2]This is mainly because global feedback constraints the output of the operational amplifier to be linear. Because of inherent nonlinearities in the amplifier transfer function this enforces nonlinearities in the collector current of the input pair, which in turn result in the mentioned distorted input currents.

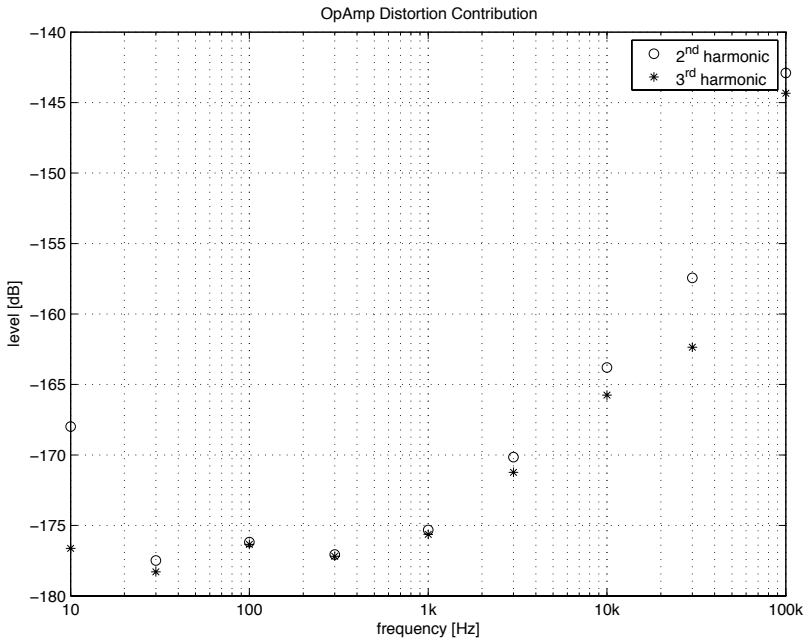


Figure 4.6: 2^{nd} and 3^{rd} harmonic distortion contribution of the discrete operational amplifier.

seen by the amplifier input of the integrator stages is 2.37 kΩ for the 2^{nd} harmonic and 1.68 kΩ for the 3^{rd} harmonic; the 1 kΩ source impedance is hence somewhat optimistic, but it has been verified that higher source impedances up to 10 kΩ do not cause additional distortion which would contribute significantly to the performance of the overall oscillator design. This also gives some ensurance that amplifier specimen which show a particularly low h_{FE} value for Q2 do not have significant input current distortion.

From these measurements it is seen that the 2^{nd} and 3^{rd} harmonic distortion contribution of the operational amplifier presented is well below the specifications for the overall oscillator performance. Harmonics above the 3^{rd} are negligible and hence no measurements are shown. The increase in 2^{nd} harmonic distortion at 10 Hz can probably be attributed to a contribution from the used distortion analyzer rather than to actual operational amplifier distortion.

To verify that the amplifier does not draw significant distorted supply currents (which could induce into the feedback network) the magnitude of the distortion of the supply currents was measured with a 200 Ω load and an output level of +14 dBu. The results for the positive supply are shown in figure 4.7; it is seen that—particularly at high frequencies where induction effects are most significant—the supply current carries extremely low levels

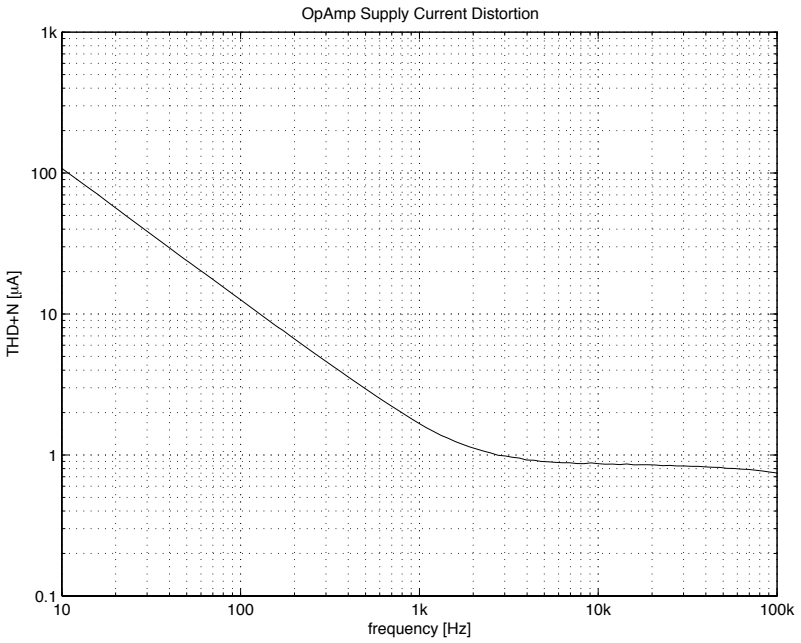


Figure 4.7: Magnitude of the THD+N content of the operational amplifier supply current.

of harmonic distortion. Results for the negative supply are very similar and hence omitted.

4.7 Voltage and Current Noise Density

The voltage and current noise density of the new operational amplifier was measured and plotted against frequency (see figure 4.8 and 4.9). At 1 kHz the noise figures of the amplifier are about $1.4\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ and $1\,\mathrm{pA}/\sqrt{\mathrm{Hz}}$; the resulting optimum source impedance of $1.4\,\mathrm{k}\Omega$ is a very close match to the actual operating conditions of the amplifiers. At the optimum source impedance the noise figure is just 0.7 dB which is an excellent result considering that the amplifier achieves outstanding AC performance as well.

Because the transconductance shaping of the input stage it is expected that the voltage noise density of the new operational amplifier increases at frequencies above the audio frequency range. Preliminary measurements indicate that the increase is about 10 dB; this corresponds well with the value of R1 and R2 which are expected to be the dominant noise contributors in that frequency range. Detailed measurements must be left for future research though.

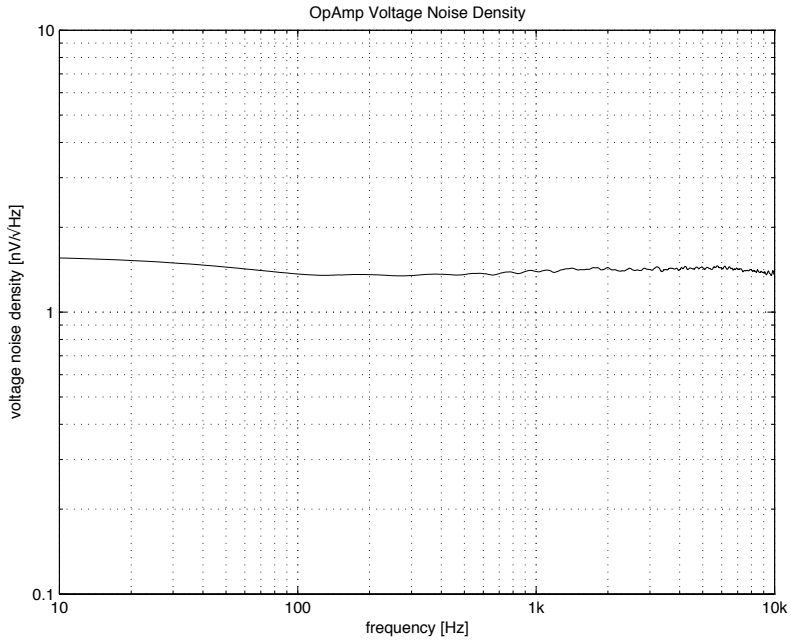


Figure 4.8: Voltage noise density of the discrete operational amplifier.

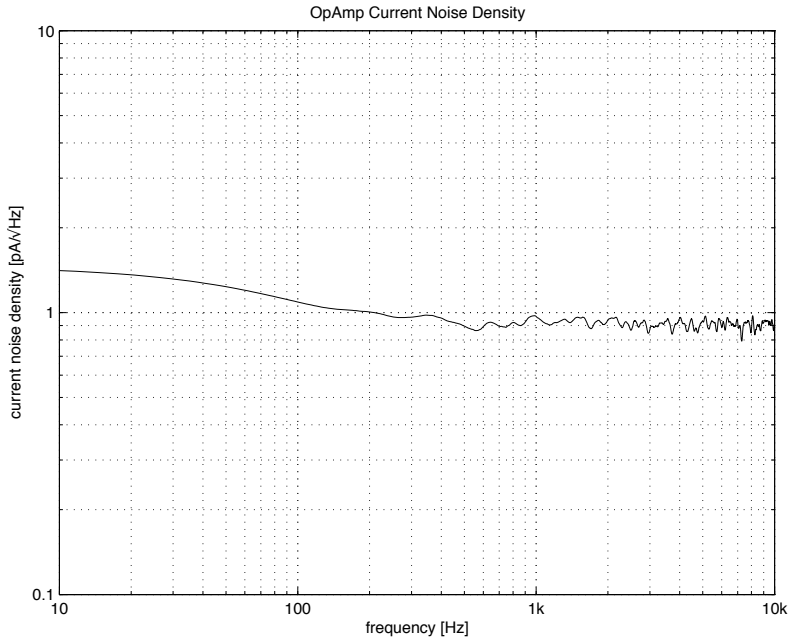


Figure 4.9: Current noise density of the discrete operation amplifier.

Chapter 5

Level Detector and Error Integrator

This chapter mainly considers the level detector which has significant influence on the overall oscillator performance. In particular we will discuss the performance requirements, limitations in prior art implementations and the design and performance verification of a new level detector. Also presented in this chapter are the error integrator, startup circuitry and amplitude settling indication.

5.1 Performance Requirements

The performance requirements of the level detector are very demanding; for most oscillators its deviations from ideal dominate the overall distortion performance. In short it must offer:

- Low output ripple
- Low output noise
- High amplitude flatness and accuracy in the intended frequency range (3 Hz–300 kHz)
- Fast response to amplitude changes

Below we will elaborate on these requirements in more detail.

Any output ripple of the level detector leads to amplitude modulation of the oscillator output; for a ripple frequency f_r and an oscillator frequency f_0 sideband signals at $|f_0 - f_r|$ and $f_0 + f_r$ will result [43]. If the ripple frequency is correlated to the oscillator frequency (i.e. $f_r = n \cdot f_0$ for $n \in \mathbb{N}$) it is easily seen that harmonic distortion is generated. This distortion is low pass filtered by the integrator stages of the state-variable topology; by

simulation it is shown that 2^{nd} harmonic distortion is reduced by 9.54 dB; the corresponding figure for the 3^{rd} harmonic is 18.06 dB. Nonetheless it is clear that level detector ripple must be sufficiently low to achieve the desired distortion performance.

Besides ripple which is correlated to the oscillator frequency the level detector output will also show some amount of random noise. This noise content will again cause amplitude modulation of the oscillator output. Typically the level detector noise will show significant $1/f$ noise content which is not attenuated by the low pass action of the integrator stages. As good amplitude stability of the oscillator output is desired the level detector output noise must be reasonably low.

For good amplitude flatness the level detector DC output voltage should be independent of oscillator frequency; in particular bandwidth-limitations tend to reduce the output voltage at high frequencies. The loop gain of the leveling loop will correct this by increasing the oscillator amplitude. Also any drift, hysteresis or other forms of amplitude detection errors will influence the oscillator level accuracy and should be minimised.

The level detector should offer fast response to oscillator amplitude changes. Any delay introduced will add phase shift to the transfer function of the leveling loop; if the phase shift becomes sufficiently high it will increase amplitude settling time or even result in amplitude instability.

The requirements of the error integrator are easier to fulfil. First of all the time constant of the error integrator should inversely track the oscillator frequency for fast settling of the control voltage (which is feed to the multiplier) [17][18]; above 10 kHz tracking may be suspended as settling times become fast enough anyway. Second the error integrator must not contribute significant ripple to the control voltage signal.[1]

5.2 Level Detector Topology

There are numerous level detector topologies which have been used in prior art oscillators. In the following we will consider the most common architectures. A full-wave rectifier has found frequent use particularly in earlier and simple oscillator designs [5][6][13][22][34][44][45][46]. The output of a full-wave rectifier theoretically contains—besides the DC content—2^{nd} harmonic and higher even-order harmonics only. Hence the level detector ripple solely causes 3^{rd} (and higher odd-order) harmonic distortion at the oscillator output. However in practice asymmetries and offsets in the rectifier

[1] At first it seems misguided to expect ripple contribution from the error integrator as integrators are typically implemented as linear circuit. However as will be seen the final implementation of both the level detector and error integrator uses switching techniques which invariably cause some output ripple.

will introduce some fundamental frequency and 3^{rd} harmonic content in the level detector output. This causes 2^{nd} harmonic distortion at the oscillator output which is less rejected by the low pass action of the integrator stages than higher order harmonics. In practice the ripple at the level detector output will be far too high for the distortion levels intended in this thesis and hence the full-wave rectifier is not considered further here.

A substantial improvement is possible by the use of a four-phase rectifier [16]; the additional phases at $\frac{1}{2}\pi$ and $\frac{3}{2}\pi$ are easily derived from the band pass output of a state-variable oscillator topology. Theoretically the ripple of a four-phase rectifier contains 4^{th} harmonic (plus higher harmonics at multiples of four) only. This introduces 3^{rd} (and higher odd-order) harmonic distortion at the oscillator output, however the level is much lower than for a full-wave rectifier. Again in practice non-idealities in the rectifier will introduce lower harmonics and fundamental frequency content in the output of the rectifier. More significant however is the dependence on RC time constant match of the two integrator stages. A mismatch causes different output levels at the band pass and low pass outputs of the state-variable ring; this introduces odd-order harmonics in the level detector output and also leads to a—possibly frequency-dependent—oscillator level error. This level detector scheme is hence unsuitable for the performance levels intended for the oscillator design presented here.

We now consider the Pythagorean trigonometric identity [47] given as:

$$1 \quad = \quad \sin^2(\omega t) + \cos^2(\omega t) \tag{5.1}$$

By this it is seen that the sum of the squared band pass and low pass output of a state-variable oscillator topology gives a theoretically ripple-free and instantaneous level detector [48]. RC time constant mismatch in the integrator stages will introduce 2^{nd} harmonic content in the level detector output and an oscillator level error [33]. Furthermore feedthrough, nonlinearities and noise of the multipliers will introduce various other errors in the level detector output. While this detector scheme offers substantially higher performance than the previously introduced full-wave and four-phase rectifiers the practical limitations with respect to output ripple and oscillator amplitude error are difficult to overcome and hence this approach was not considered further after one prototype has been evaluated.

The level detector topology finally chosen for the oscillator design presented in this thesis basically uses a sample-and-hold amplifier which samples the peak amplitude of the oscillator output signal [49][50]. With an ideal sample-and-hold amplifier this level detector scheme results in zero output ripple; also because only the low pass output of the state-variable

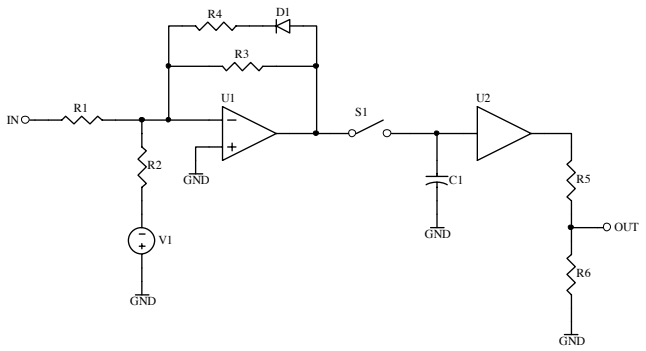


Figure 5.1: Basic sample-and-hold level detector with preceding gain stage.

ring is used to derive the amplitude information no sensitivity to integrator time constant mismatch exists. Naturally any practical sample-and-hold amplifier will show some output ripple and noise due to various circuit limitations (which will be discussed in detail later). However this approach offers the possibility to subtract the reference voltage *ahead* of the actual level detector; this shifts the nominal (positive) peak voltage to zero and it becomes easy to amplify this signal before the sample-and-hold amplifier. By attenuation of the sample-and-hold amplifier output a nominal gain of unity is restored which simultaneously reduces ripple and noise in proportion. This possibility is unique to this level detector architecture; all previously discussed approaches require subtraction of the reference voltage after the actual amplitude sensing, hence no gain can be introduced ahead of the detector.

Figure 5.1 further illustrates the principle. R1 and R2 provide the subtraction of the reference voltage V1 from the oscillator sine wave (present at the input port). U1 amplifies the difference signal with a gain given by $-\frac{\mathrm{R3}}{\mathrm{R1}}$; D1 and R4 limit the gain at large positive output voltages to $-\frac{\mathrm{R3}\|\mathrm{R4}}{\mathrm{R1}}$ to prevent saturation of U1. S1, C1 and U2 form the sample-and-hold amplifier whose output is attenuated by the voltage divider formed by R5 and R6; these resistors are chosen such that $\frac{\mathrm{R3}}{\mathrm{R1}} = 1 + \frac{\mathrm{R5}}{\mathrm{R6}}$ to restore a nominal gain of unity. This attenuates the effective ripple and noise of the sample-and-hold stage by the ratio of $\frac{\mathrm{R3}}{\mathrm{R1}}$ while simultaneously reducing its headroom. In principle arbitrary high values of attenuation may be implemented. However considerations with respect to amplitude settling time constrain an upper limit; ideally the output of the sample-and-hold amplifier is able to force the integrator output voltage (i.e. the control voltage which feeds the multiplier) from the maximum to the minimum value (and vice versa) within one cycle. This requires a minimum value for the headroom in the sample-and-hold amplifier. In practice some saturation of the

sample-and-hold amplifier is acceptable, but for a typical implementation the gain ahead of the sample-and-hold stage is limited to less than 40 dB for reasonable settling behaviour.

The basic implementation as shown in figure 5.1 shows output ripple because of finite sampling time of the sample-and-hold amplifier. For fast and accurate response to amplitude changes the sampling time must not fall below some minimum which is given by the on-resistance of the switch and the value of the sampling capacitor; the value of the sampling capacitor cannot be made arbitrary low because of hold droop (which becomes a significant ripple contributor at low frequencies) and the on-resistance is limited by available semiconductor technology[2]. During the on-time of the switch the amplitude envelope of the input signal will be passed to the output where it causes ripple—particularly at high frequencies where the on-time is more significant relative to the period of the oscillator signal. For the distortion levels intended for the oscillator design presented in this thesis it is necessary to reduce this ripple contribution by topological means. Several prior art oscillators have used a two-stage design [18][33][51][52] which is also employed for this oscillator. The operation is illustrated by figure 5.2. The first stage is made to track the oscillator signal during half of its period (more precisely from phase $\frac{3}{2}\pi$ to $\frac{1}{2}\pi$) and to hold the peak amplitude during the other half of the period (that is from phase $\frac{1}{2}\pi$ to $\frac{3}{2}\pi$). The second stage samples the output of the first stage during a fixed period after the first stage has switched to hold mode.

By this two-stage approach it is possible to optimise the track-and-hold stage for fast acquisition time and the sample-and-hold stage for low hold droop; this enables implemention of a level detector with low ripple, excellent amplitude flatness and fast response. However prior art oscillators have invariantly used simple implementations for both the track-and-hold and sample-and-hold amplifier. These consist each of a single switch and a single hold capacitor (as conceptually shown in figure 5.1). There are various limitations in these designs which contribute to output ripple:

- During the sampling time of the sample-and-hold stage feedtrough in the track-and-hold stage appears as ripple at the level detector output. This ripple contribution increases with frequency as the (fixed) sampling time of the sample-and-hold amplifier becomes a more significant portion of the period of the oscillator frequency.

[2]Transistors with low on-resistance typically show higher junction capacitance; this increases control voltage feedthrough and input feedthrough during the hold state. Both effects increase output ripple.

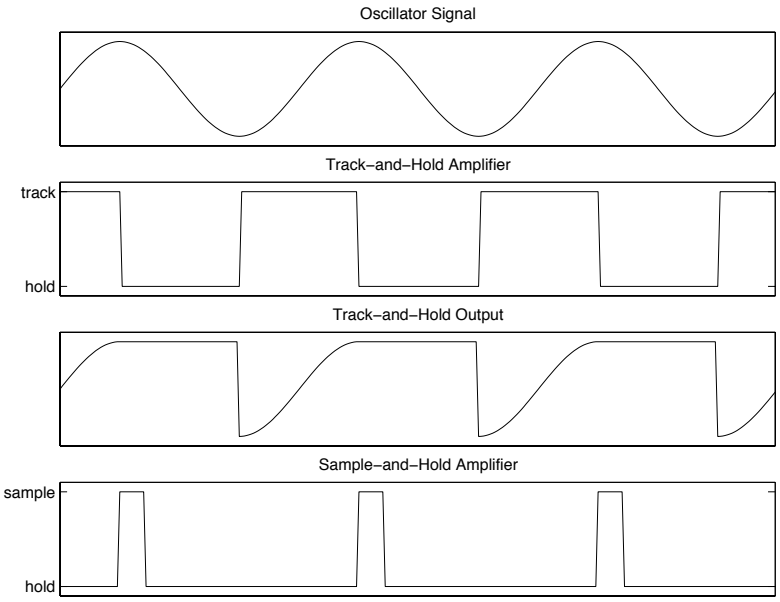


Figure 5.2: Operating principle of the track-and-hold/sample-and-hold level detector.

- Control voltage feedtrough in the sample-and-hold stage causes a pedestal step in the output voltage during the sampling time. Again this ripple contribution increases with frequency.
- Hold droop in the sample-and-hold amplifier causes ripple which increases towards low frequencies where the hold time increases.

Additional minor contributions result from hold droop in the track-and-hold stage and feedtrough in the sample-and-hold amplifier.

For the performance levels of this oscillator design as specified in chapter 2 the output ripple of these prior art implementations is unacceptably high. To address the various issues listed above a new design was derived. A simplified schematic diagram is depicted in figure 5.3. As is seen both the track-and-hold amplifier (U1) and the sample-and-hold amplifier (U2) use the same arrangement of switches (S1–S3 and S4–S6) and hold capacitors (C1/C2 and C3/C4); in the following we will only consider the track-and-hold stage for simplicity.

The series-conntected switches S1 and S2 are used to improve hold mode feedthrough; R1 bootstraps S2 which makes its feedthrough capacitance very small. C2 and S3 are added to reduce hold droop [53]; to the extent that the value of C1 and C2, the inverting and noninverting input bias current of U1 as well as any other leakage current contributors (such as printed circuit board leakage) are matched the hold droop appears as common-mode signal

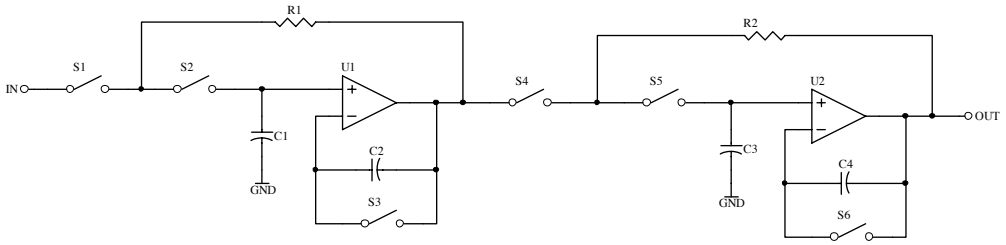


Figure 5.3: Simplified track-and-hold/sample-and-hold amplifier with improved feedthrough and hold droop performance.

to U1. Unless the linear common-mode range is exeeded the hold droop error is hence reduced by the common-mode rejection of the used operational amplifier. This arrangement also cancels control voltage feedthrough of S2 and S3.

By this new track-and-hold/sample-and-hold amplifier very low output ripple is achieved over the full oscillator frequency range. Amplitude flatness is somewhat compromised because of the series-connected switches which double the on-resistance; however this was considered a minor disadvantage as compensation may be achieved by a frequency-shaping network ahead of the track-and-hold amplifier. In the following section we will present the actual implementation of the level detector.

5.3 Implementation

We will first consider the implementation of the voltage reference circuitry which is used to generate the oscillator level reference—see figure 3.2 in the schematic diagram document. A reference voltage of +5 V is provided by the precision bandgap reference U0201. The output voltage of this integrated circuit is inverted, amplified, low pass filtered and buffered by operational amplifier U0202 plus associated feedback network (R0201–R0203 and C0202). Q0201 is switched on if the oscillator is muted. Subtraction of the reference voltage from the oscillator signal is done by U0301 (see figure 3.3 in the schematic diagram document); trimming of the oscillator level is achieved by R0303. D0301 and D0302 limit the gain of the stage formed by U0301 at large positive and negative output voltages in order to avoid saturation of U0301. Further waveform shaping is provided by D0303 and D0304; together with the gain of two provided by U0304 this limits the voltage to the following track-and-hold/sample-and-hold amplifiers to +10.7 V and −5.7 V. This protects the switches in the track-and-hold/sample-and-hold stages from breakdown. The overall gain of the two stages formed by

U0301 and U0304 is 20; as discussed above this gain reduces ripple from the track-and-hold/sample-and-hold amplifiers.

Figure 3.4 shows the comparator circuit used to derive the timing information for the switches of the track-and-hold amplifier. U0401 is fed from the band pass output of the state-variable oscillator ring and provides waveform shaping to reduce the effect of offset in the following comparator circuit. C0401 and R0402 are selected for high-frequency flatness of this stage. Q0401–Q0405 form the discrete high-speed comparator. C0402 dynamically increases the tail current of the differential input pair (Q0401 and Q0402) to enable a switching time of about 10 ns for a negative transition. This switching time is critical for good amplitude flatness at high frequencies; any delay introduced will shift the sampling point away from the peak of the sine wave which results in reduced amplitude reading. C0403 and Q0405 speed-up positive transitions.

The track-and-hold amplifier is depicted in figure 3.5 in the schematic diagram document. Q0501*–Q0503* are the switching transistors which need to be selected and matched for pinchoff voltage. Matching Q0502* and Q0503* is necessary to synchronise their switch-off characteristics. Selecting Q0501* for higher pinchoff voltage minimises control voltage feedthrough as Q0502* will turn off before Q0501*, preventing the feedthrough charge from reaching the hold capacitor C0501. C0501 and C0502 are the hold capacitors which need to be precision types for good rejection of control voltage feedthrough and hold droop. U0501 needs to offer low input bias and offset current along with high speed and reasonably low voltage offset and drift; a combination wich is only provided by few FET amplifiers.

The timing for the sample-and-hold stage is derived from two one-shot circuits as shown in figure 3.6. The first one-shot provides a 32 μs pulse after a negative transition of the comparator output (i.e. after the track-and-hold stage has switched to hold mode); this pulse is used to switch the sample-and-hold amplifier to sampling mode (by turning off Q0602). Simultaneously Q0601 is turned on to hold the comparator output in the low state; this is necessary as otherwise the track-and-hold amplifier would switch to tracking mode during the sampling period of the sample-and-hold amplifier for frequencies above about 15 kHz. The second one-shot is used to force the sample-and-hold stage to at least 15 μs hold mode duration. This is essential for correct level sensing because the track-and-hold stage might need more than one cycle for accurate amplitude tracking at high frequencies (above 100 kHz).

The sample-and-hold amplifier (see figure 3.7 in the schematic diagram document) uses very similar circuitry as the previously discussed track-and-hold amplifier. However it is modified to show reduced hold droop and control voltage feedthrough by several means:

- The sampling capacitors C0701 and C0702 are considerably larger.
- The switching transistors Q0701*–Q0703* have lower junction capacitances.
- The inputs of U0701 are guarded to reduce printed circuit board leakage.
- The residual hold step is trimmed by R0706.

The increased sampling capacitor value and the different transistor types (with higher on resistance) reduce the bandwidth of the sample-and-hold amplifier compared to the track-and-hold amplifier. This is however—as shown above—of no disadvantage as the sampling time is fixed to 32 μs even at high frequencies.

The error integrator implementation is shown in figure 3.8. U0802 provides a single 100 μs pulse per oscillator period during which transistor switch Q0803 is turned on. That way the integrator time constant is made to inversely track the oscillator frequency. For oscillator frequencies above 10 kHz Q0803 is continuously switched on. U0801 provides polarity inversion to correct the inversion of the following integrator stage.

The error integrator output voltage and the output of the sample-and-hold stage are summed by U0901 (consider figure 3.9 of the schematic diagram document). This implements the correct integrator zero (or leveling loop response at high frequencies) for fast settling. In the highest frequency range the output of the sample-and-hold amplifier is reduced by switching of Q0901. This adjusts the integrator zero to accomodate that at high frequencies the oscillator amplitude is not sensed in every period.

To indicate that the amplitude has settled a window comparator (U1001 in figure 3.10) is used. It senses the error voltage present at the sample-and-hold amplifier output; if the error voltage is below $\pm$99 mV settling is indicated. As the timing of the various stages in the level detector and error integrator requires a sufficiently large oscillator amplitude to be present for correct operation an independent circuit to guarantee startup must be provided. U1002, U1003 and U1004 implement a level detector based on the Pythagorean trigonometric identity as explained in section 5.2. The output of U1005A goes high if the oscillator amplitude is very low; R1013 applies hysteresis to the comparator circuit to avoid multiple transitions during settling. The second section of U1005 invertes the output of U1005A; both signals are used to switch transistors in the main oscillator loop which activate speedup-circuitry. If the oscillator is muted the output of U1005A is forced to the low state.

Figure 3.11 in the schematic diagram document shows the local voltage regulators of the level detector board. The circuit realises low output noise

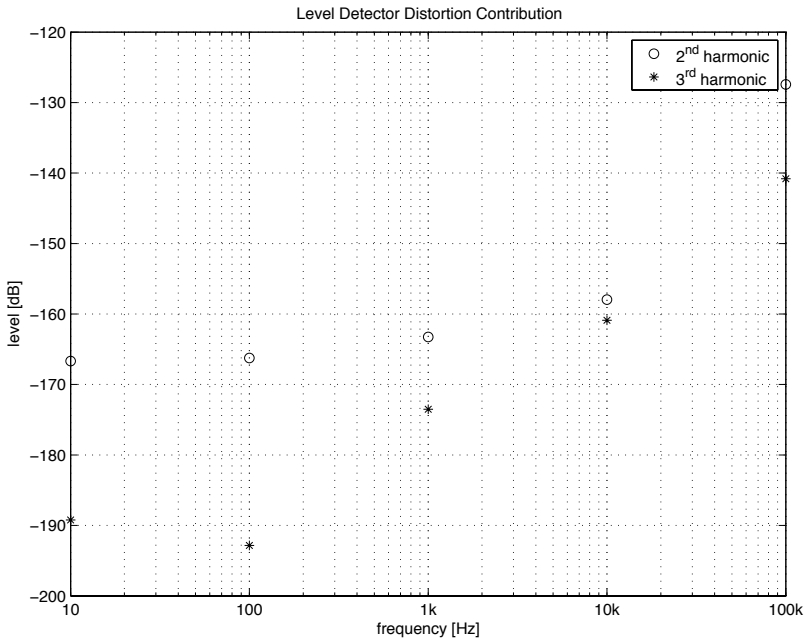


Figure 5.4: Distortion contribution from level detector ripple.

and low output impedance. Shunt regulators are used to localise any supply currents which may carry harmonic distortion of the oscillator signal. This reduces the loop area of the harmonic distortion currents to minimise their induction into the main oscillator loop. In critical places local RC filters have been added (e.g. R0415 and C0406) to further reduce loop area.

The overlay print of the level detector daughterboard is shown in figure 3.12;[3] visible are several screening cans which have been added at critical nodes. The screening reduces hum pickup (which would result in amplitude noise) and crosstalk to the main oscillator board. The later is particularly important as the various timing circuits of the level detector generate fast pulses which are synchronous to the oscillator frequency; significant crosstalk would hence result in harmonic distortion.

5.4 Distortion Contribution

To evaluate the distortion contribution of the level detector it is necessary to measure the output ripple. As shown above fundamental frequency and 3^{rd} harmonic content of the ripple causes 2^{nd} harmonic distortion in the oscillator output; likewise 2^{nd} and 4^{th} harmonic ripple content results in 3^{rd} har-

[3] R0403 is shown in the overlay print but not in the according schematic diagram because the use of this resistor was not found necessary.

monic oscillator distortion. By summing up either fundamental frequency and 3^{rd} harmonic ripple content or 2^{nd} and 4^{th} harmonic ripple content and consideration of the multiplier gain constant k, multiplier decoupling factor α and the low pass filtering action of the integrator stages it is possible to calculate the distortion contribution at the 2^{nd} and 3^{rd} harmonic.

Figure 5.4 shows the measurement results for several oscillator frequencies. It is seen that the distortion contribution of level detector ripple is well below the specifications of the oscillator as given in chapter 2. Verification of this measurement procedure was done by injecting a fraction of the oscillator signal into the control voltage signal (provision has been made for this by addition of P0901); resulting ripple is sufficiently large to cause distortion which is directly measurable at the oscillator output.

5.5 Noise Contribution

The peak noise of the control voltage signal was measured at about 1.6 mV. By multiplication with the multiplier gain constant k and decoupling factor α it is found that the resulting oscillator amplitude noise is less than 7 μdB which is a very good figure. Most of the control voltage noise is actually caused by hum pick up as the oscillator was operated without the screening cans or other form of screening installed; this is confirmed by the FFT plot of figure 5.5 where it is seen that the sidebands peak at ± 50 Hz of the oscillator frequency. It is estimated that amplitude noise is reduced by an order of magnitude once proper screening and casing of the oscillator has been applied.

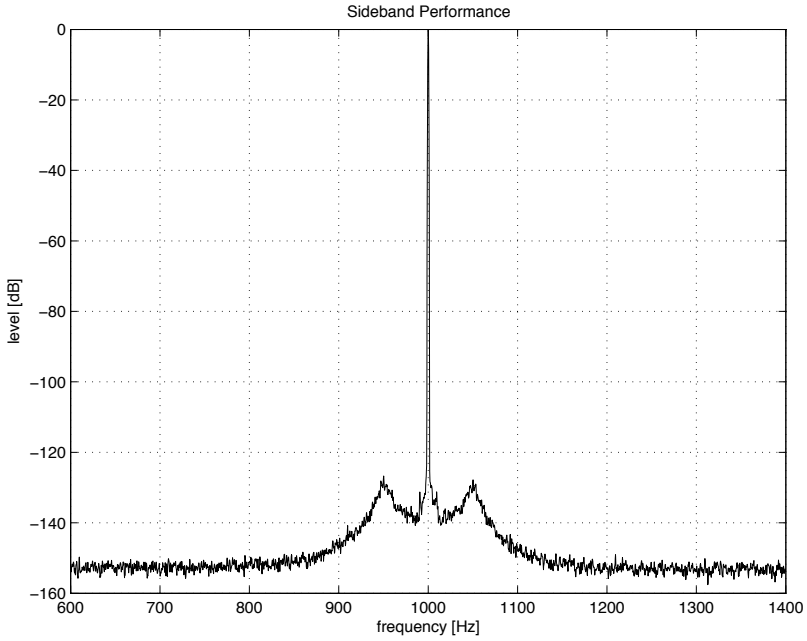


Figure 5.5: Sideband noise of the new oscillator design.

Chapter 6

Multiplier

In this chapter we will first present the performance requirements of the multiplier. Subsequently known implementations are analysed and a new solution with improved behaviour is presented. Finally detailed measurements of the multiplier distortion and noise contribution are shown.

6.1 Performance Requirements

As a basic requirement the multiplier should support four-quadrant operation as this simplifies the design of the overall oscillator loop, particularly over a wide frequency range. Furthermore its gain constant k should be dependable and roughly constant over the full control voltage range of $\pm 12\,\mathrm{V}$ as it is a first-order term of the transfer function of the leveling loop; substantial deviation from a nominal value will influence amplitude settling characteristics and can result in amplitude instability. Basic amplitude accuracy will not be affected however as the high DC loop gain of the leveling loop reduces any error in the multiplier.

Obviously the multiplier circuit should contribute harmonic distortion to the oscillator output well below that given in the specifications (see chapter 2). If we contemplate again figure 3.1 it is seen that the output of the multiplier (denoted as U5) is low pass filtered by the two integrator stages formed around U2 and U3 if the oscillator output is taken from the low pass output of the state-variable ring (i.e. the output of the second integrator stage). By simulation it is easily shown that the 2^{nd} harmonic contribution of the multiplier is reduced by 9.54 dB; the corresponding figure for the 3^{rd} harmonic is 18.06 dB. Also in a typical implementation the multiplier will be decoupled by a factor α, which further attenuates the harmonics present at the multiplier output. However the multiplier authority (i.e. $\frac{k}{\alpha}V_{C_{max}}$) is limited to a minimum value as shown in chapter 3, and for typical multiplier circuits an increase in k will also result in a proportional increase in the

absolute level of output distortion for a given control voltage. Hence no further distortion reduction by decoupling can be achieved once the minimum multiplier authority is reached.

To reduce distortion the internal operating level of the multiplier should be minimised. However this cannot be taken too far as otherwise the multiplier output will show significant levels of noise. Noise sufficiently above the oscillator frequency is low pass filtered by the two integrator stages just as harmonic distortion. However noise below the oscillator frequency is not attenuated by the integrator stages. Decoupling of the multiplier will attenuate noise—however as shown above for the harmonic distortion contribution the minimum multiplier authority needed limits the achievable attenuation. Hence particularly for high oscillator frequencies (where the low pass action of the integrators is least effective to reduce noise) multiplier noise should be minimised.

6.2 Multiplier Topology

Most multipliers used in prior art oscillators are based on voltage-controlled resistors using JFETs [5][13][18][33][45][48][54][55][56]. While these circuits are easily implemented at low cost and complexity they have a number of disadvantages. First of all the AC voltage across the voltage-controlled resistor must be kept very low (well below 100 mV) for sufficiently low distortion, making noise contribution an issue. Typically distortion cancellation [32] is implemented, however cancellation accuracy is limited by transistor parameter spread. Trimming is possible but thermal drift will remain. Furthermore the considerable parameter spread which is observed in JFETs will make the gain constant k unpredictable unless the transistor is selected. Even then some temperature dependence will remain.

In some oscillator designs light-dependent resistors have been used (see e.g. [5][6]). While these resistors may offer somewhat lower distortion at medium frequencies (around 1 kHz) than the previously discussed JFET implementations they typically show increased distortion at low and high frequencies (below 100 Hz and above 10 kHz) according to measurements of the author. This is presumably because of thermal self-modulation (at low frequencies) and voltage-dependent capacitance (at high frequencies). In addition to this the control law is substantially nonlinear; for reasonably constant k this necessitates the use of a compensation circuit (e.g. as shown in [57]). Light-dependent resistors also show rather high time constants (5–100 ms) which are very different for rising and falling resistance. These time constants will act as an additional low pass filter in the transfer function of the leveling loop. This may affect settling time and amplitude stability.

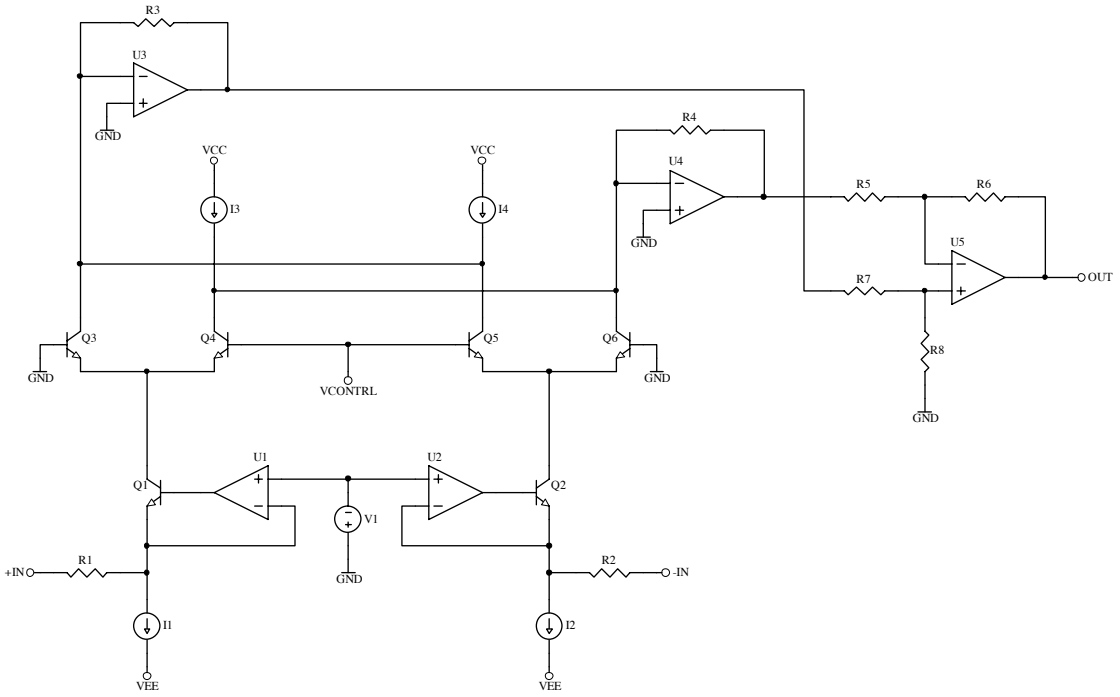


Figure 6.1: Simplified schematic diagram of the new multiplier circuit.

Other possibilities which have been implemented in prior art oscillators include voltage controlled attenuators (VCAs) [22] and multipliers based on translinear gain cells [44][51][52], both of which are available as integrated circuits. VCAs offer low distortion and low noise but are—in a basic implementation—limited to two-quadrant operation; furthermore their gain law is not linear but dB-linear which is highly inconvenient as resulting gain constant k is anything but constant. Commercially available multipliers based on translinear gain cells offer four-quadrant operation but suffer from rather high distortion and noise levels; this is to a good extent a result of their optimisation with respect to accuracy, drift, bandwidth and settling time.

For the implementation of this low distortion oscillator a new multiplier topology was developed. It is also based on a translinear gain cell but optimised for low distortion and noise. A simplified diagram of the new topology is shown in figure 6.1. The basis of the new multiplier circuit is the translinear gain cell formed by Q3–Q6; the output currents of this cell are cross-coupled to provide a differential output current which is subsequently converted to a single-ended output voltage by U3–U5. The differential input voltage is converted to a differential current by U1, U2, Q1, Q2, R1 and R2.

This new multiplier topology has several advantages over prior art multipliers. Due to local feedback the linearity of the voltage-to-current converters (which carry the oscillator signal) is very good. The linearity of the translinear gain cell is enhanced because the collectors of the transistors are all operated at equal and constant collector voltage; this eliminates distortion from Early effect. As the emitter-collector voltage is kept low (approximately 0.6 V) thermal dissipation of the transistors is very low which greatly reduces low-frequency distortion due to thermal self-modulation.

In the following section we will consider the detailed implementation of the new multiplier circuit; consideration of the full schematic diagram and overlay print as available in chapter 4 of the schematic diagram document is suggested. A detailed mathematical analysis of the translinear gain cell operation will not be presented here; the interested reader may instead consider the references [58][59][60][61].

6.3 Implementation

The linearity of the voltage-to-current converters is a major consideration as their distortion contribution can easily dominate the multiplier performance particularly at high frequencies. The basic transconductance nonlinearity of Q0202 and Q0205 is reduced by the loop gain of the operational amplifiers (U0201 and U0202) to negligible levels. The nonlinear losses from base current and collector-base junction capacitance are added to the emitter current by Q0201 and Q0203 [62]. This allows sensing of these currents by feedback which reduces their distortion contribution. Without this arrangement the voltage-to-current converters would cause significant additional distortion particularly at high frequencies. C0201 and C0202 localise the feedback loop of the operational amplifiers at high frequencies for stability reasons.

The biasing of the voltage-to-current converters and the translinear gain cell is very critical. Low noise is achieved by low quiescent current as this reduces the basic transconductance of the transistors of the translinear gain cell; low distortion however demands high quiescent current to keep the AC collector current small compared to the DC collector current. For this design a total translinear gain cell current of about 1.3 mA was empirically chosen for both good noise and distortion performance. Actual biasing is provided by the current source transistors Q0203 and Q0204. D0201 serves as low noise base voltage reference; as the temperature coefficient of the forward voltage of this light-emitting diode approximately tracks that of the V_{be} of a bipolar transistor [37] the collector currents of Q0203 and Q0204 and hence the quiescent current of the translinear gain cell remain temperature independent. The input voltage of the operational amplifiers (U0201 and U0202)

is provided by the bandgap reference U0203. The considerable voltage noise from this reference is low pass filtered by R0211 and C0203.

The translinear gain cell itself consists of a matched transistor array (Q0301A–Q0301E). Matching, log conformance and low $r_{bb'}$ is important for these transistors to achieve low distortion [61][63]. The control voltage is reduced to a useful range (approximately ±65 mV) by the voltage divider formed by R0301 and R0302; with this control voltage range the gain constant k remains approximately independent of control voltage. It is symmetrically reduced by about 20 % at the highest control voltages, however this is a sufficiently low deviation from the nominal value of 0.01 to not influence amplitude settling or amplitude stability. C0301 reduces high-frequency content of the control voltage signal. The current sources provided by Q0302 and Q0303 cancel the quiescent current of the translinear gain cell and allow operation of the following current-to-voltage converters at zero DC voltage. R0305 allows trimming of the differential DC offset at the outputs of the current-to-voltage converters.

U0401–U0403 implement the current-to-voltage converters and the differential-to-single-ended conversion. C0405 and C0406 provide AC-coupling as there is typically a small DC offset present at the output due to drift in the bias circuit. The anti-series arrangement is employed for low distortion contribution of the electrolytic capacitors [64].

The local voltage regulators are implemented as shunt type. As discussed in chapter 5 this localises any AC content of the supply current. This is advantageous because it greatly reduces the loop area of harmonic distortion present in the supply current. U0501 and U0502 provide the voltage reference and loop gain. Q0502 and Q0504 are used to increase the current capability of the shunt element. C0501 and C0503 reduce the noise gain of the shunt regulators to unity for frequencies above 16 Hz. This substantially reduces the output impedance and noise of the regulators.

6.4 Distortion Contribution

To determine the distortion contribution of the multiplier circuit the absolute level of the harmonic distortion present at the multiplier output was measured for a range of control voltages. By consideration of the multiplier decoupling α, the low pass filtering of the integrator stages and the nominal operating level of the state-variable ring an estimate for the distortion contribution at the oscillator output may be derived. Figure 6.2–6.6 show the measurement results for five decadically spaced frequencies from 10 Hz to 100 kHz. It is seen that for all control voltages and frequencies the multiplier distortion contribution is well below the specifications of the overall oscillator performance. However the distortion contribution of the multi-

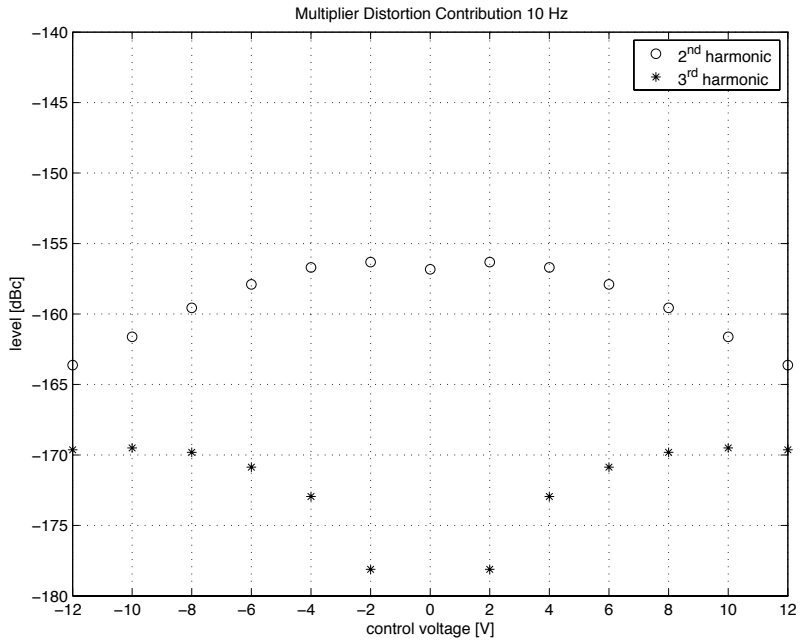


Figure 6.2: 2^{nd} and 3^{rd} harmonic distortion contribution of the multiplier at 10 Hz.

plier is clearly more significant than that of the passive components and the operational amplifiers.

6.5 Noise Contribution

The effective noise contribution of the multiplier is not straightforward to determine. As noted above the integrators low pass filter the multiplier noise as function of oscillator frequency; furthermore noise close to the oscillator frequency is amplified because of the peaking response of the state-variable ring. This part of the multiplier noise contribution will be attenuated by the notch filter of the analyzer, but the frequency response of this notch filter is not known in general.

Figure 6.7 shows measurements of the multiplier output noise relative to the oscillator amplitude of +14 dBu. Consideration has been given to the decoupling factor α but not to the frequency response of the state-variable ring. However as is seen the noise contribution of the multiplier is very low and in fact well below the noise residuals of any currently available distortion analyzer[1]. Hence it is assumed that the noise contribution of the multiplier

[1]The best commercially available distortion analyzers approach a noise floor of −120 dBc in a 22 kHz measurement bandwidth [7].

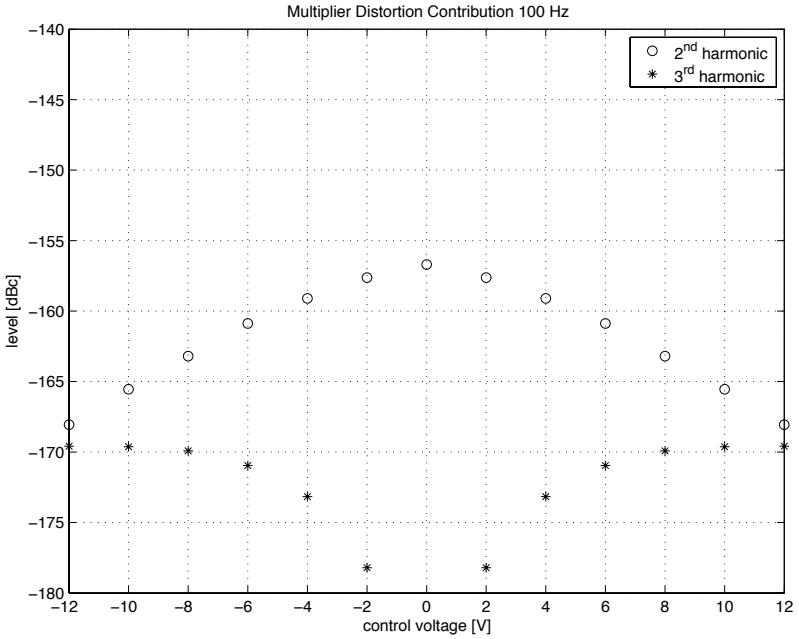


Figure 6.3: 2^{nd} and 3^{rd} harmonic distortion contribution of the multiplier at 100 Hz.

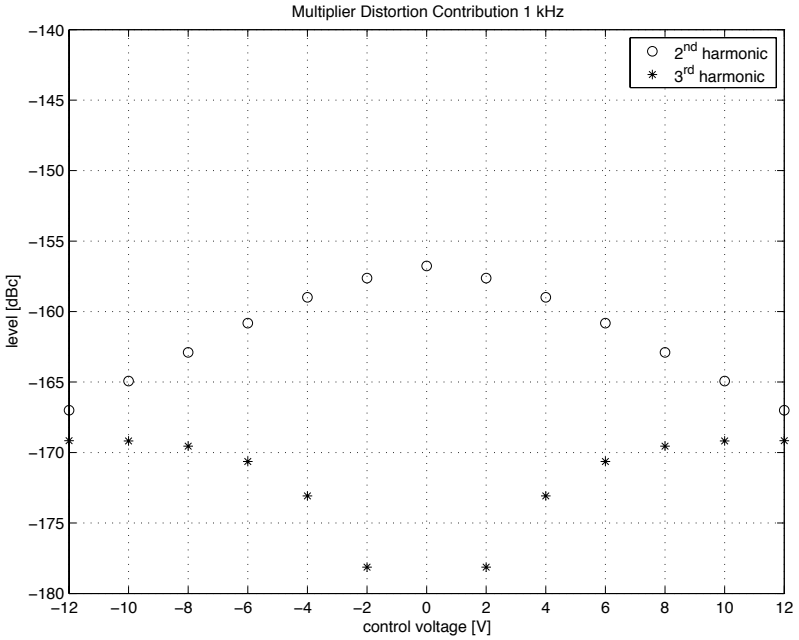


Figure 6.4: 2^{nd} and 3^{rd} harmonic distortion contribution of the multiplier at 1 kHz.

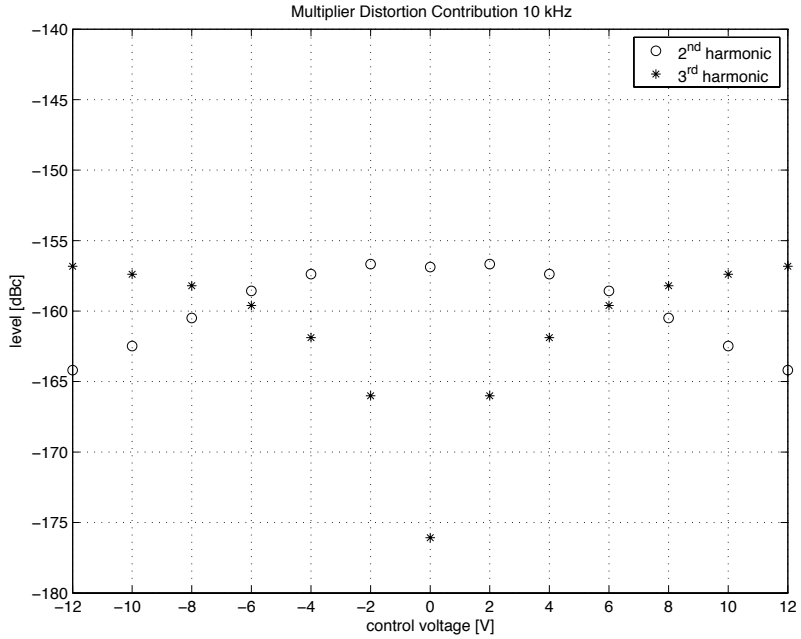


Figure 6.5: 2nd and 3rd harmonic distortion contribution of the multiplier at 10 kHz.

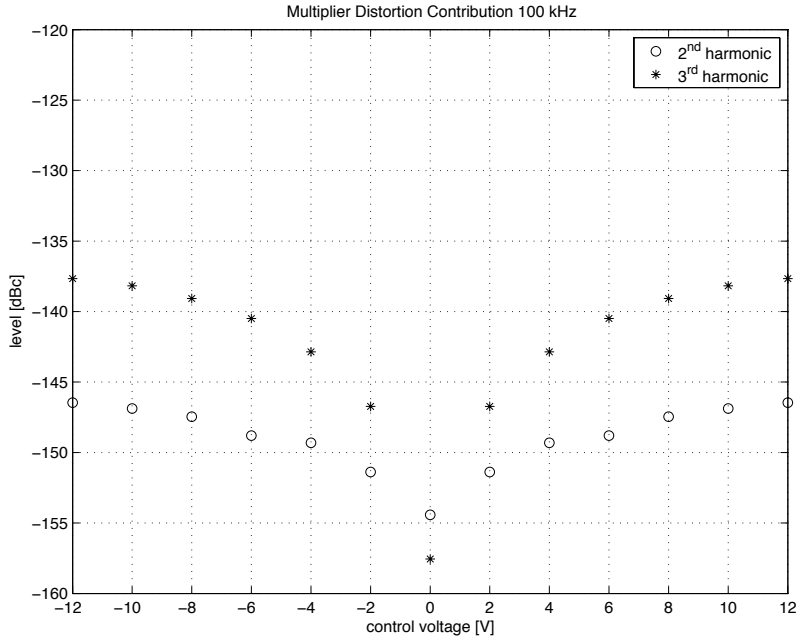


Figure 6.6: 2nd and 3rd harmonic distortion contribution of the multiplier at 100 kHz.

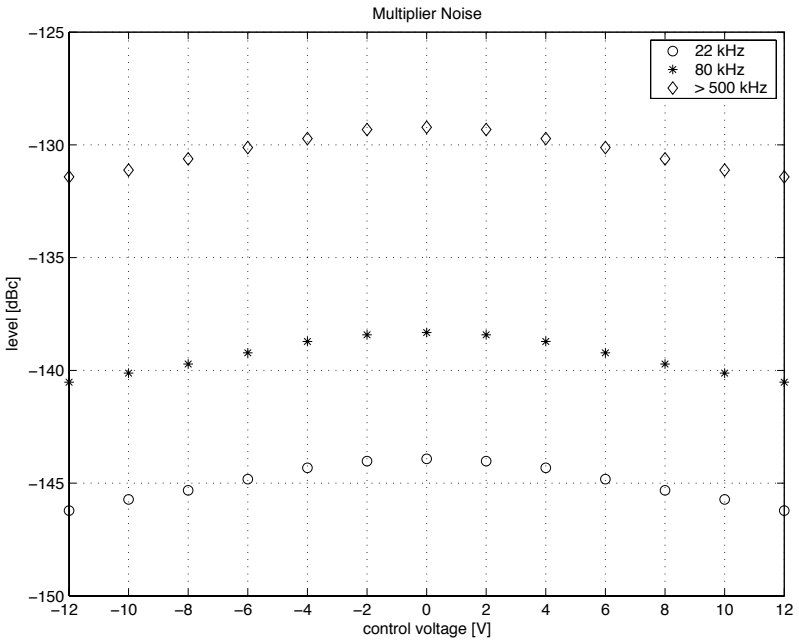


Figure 6.7: Multiplier noise contribution relative to the oscillator amplitude of +14 dBu and for three different measurement bandwidth'.

is of no relevance for any practical distortion measurement and no attempt to analyse the noise contribution in more detail has been made.

Chapter 7

Performance Verification

In the previous chapters the performance of various subcircuits was analysed. Here we will consider the overall oscillator performance, particularly with respect to harmonic distortion.

7.1 Distortion

In chapter 3–6 we have analysed the distortion contribution of the passive components, the operational amplifiers, the level detector ripple and the multiplier. Summarised the contributions for frequencies up to 10 kHz below:

	2nd harmonic	**3rd harmonic**
Capacitors		−154 dBc
Resistors		−173 dBc
Operational Amplifier	−163 dBc	−165 dBc
Level Detector	−158 dBc	−160 dBc
Multiplier	−156 dBc	−156 dBc

If these contributions are added up the resulting figures are −149 dBc for the 2nd harmonic and −145.4 dBc for the 3rd harmonic distortion. This represents a worst-case estimate and it can be expected that some contributions will actually cancel. Hence we can conclude that the sum of these main distortion sources surpasses the specification of −140 dBc; higher order harmonics have not been evaluated in detail but it has been verified that their level is well below that of the 3rd harmonic. Distortion at 100 kHz is not considered here but it has been verified that the sum of the distortion contributions is well below the specification of −100 dBc.

The distortion performance analysis as shown above ignores other potential distortion mechanisms; in particular these are:

- Induced distortion from magnetic fields carrying harmonic distortion content.

- Capacitive crosstalk from nodes with high harmonic distortion content.

- Voltage-dependent impedance contributions from the printed circuit board which appear in parallel with the feedback network of the state-variable filter; in particular capacitance and leakage resistance.

Great effort has been undertaken to reduce these effects as far as possible; the induction of magnetic fields carrying harmonic distortion content has been reduced by minimising the loop area at the source (in particular the operational amplifiers, the level detecor and also the multiplier circuit), the placement of the various circuits on the printed circuit board (in particular sufficient distance between level detector and main oscillator loop has been allowed) and magnetic screening of critical areas of the level detector. The only significant source of capacitive crosstalk is presumably the level detector daughterboard where the timing circuits generate various pulses synchronously with the oscillator frequency. Crosstalk has been minimised by electrostic screening of various critical nodes of the level detector and the use of sufficient distance to the main oscillator loop. The effect from voltage-dependent impedance of the print circuit board material has been minimised by keeping the impedance level of the feedback network low.

Nonetheless it is very difficult to ensure that none of these mechanisms causes harmonic distortion which becomes significant at the $-140\,\mathrm{dBc}$ level. Harmonic distortion analysis using the FT analyzer of the Audio Precision SYS-2722 audio analyzer [7] has been carried out at all three outputs of the state-variable oscillator ring. 2^{nd} and 3^{rd} harmonic distortion has invariably been measured at $-135\,\mathrm{dBc}$, with no higher harmonics visible. As it is highly unlikely that oscillator distortion is exactly the same at all three outputs it can be assumed that the measured distortion is actually a contribution from the analyzer. Verification with a lower distortion notch filter must be left for future research though.

Figure 7.1–7.3 shows THD+N measurement for three different measurement bandwidth' (22 kHz, 80 kHz and 500 kHz). It is seen that the actual measurements are well below the specifications of the used distortion analyzer (Audio Precision SYS-2722 [7]); again the measurements are consistent at all three outputs of the state-variable topology which indicates that the analyzer limits the measurement resolution. In any case the specifications as given in chapter 2 have been surpassed.

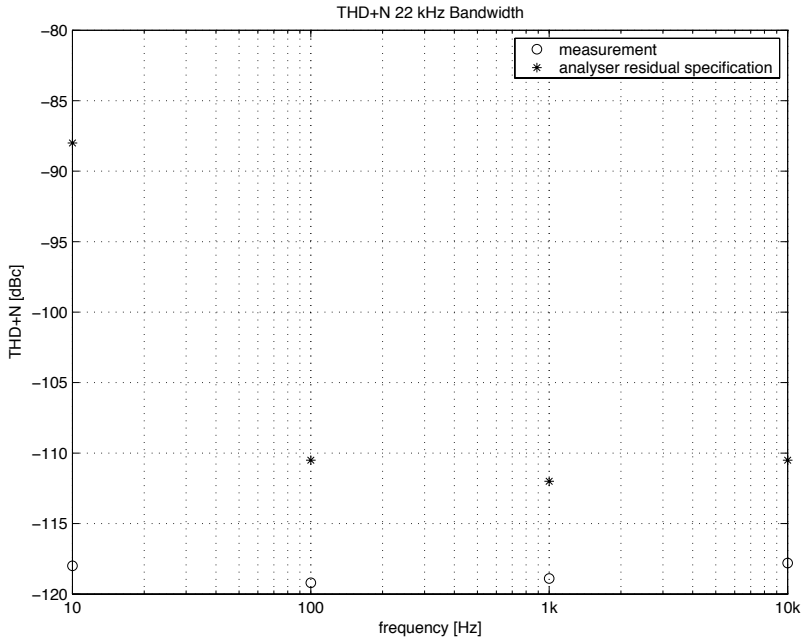


Figure 7.1: THD+N in a 22 kHz measurement bandwidth.

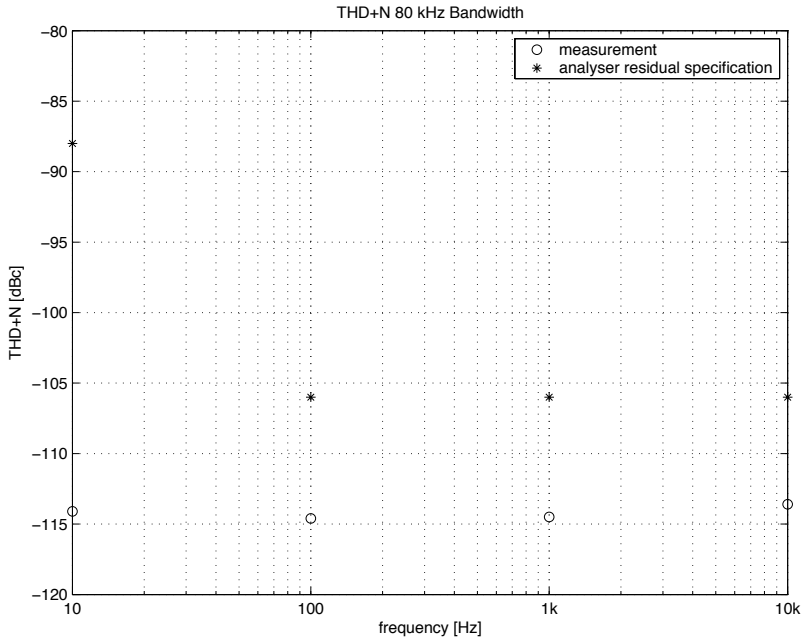


Figure 7.2: THD+N in a 80 kHz measurement bandwidth.

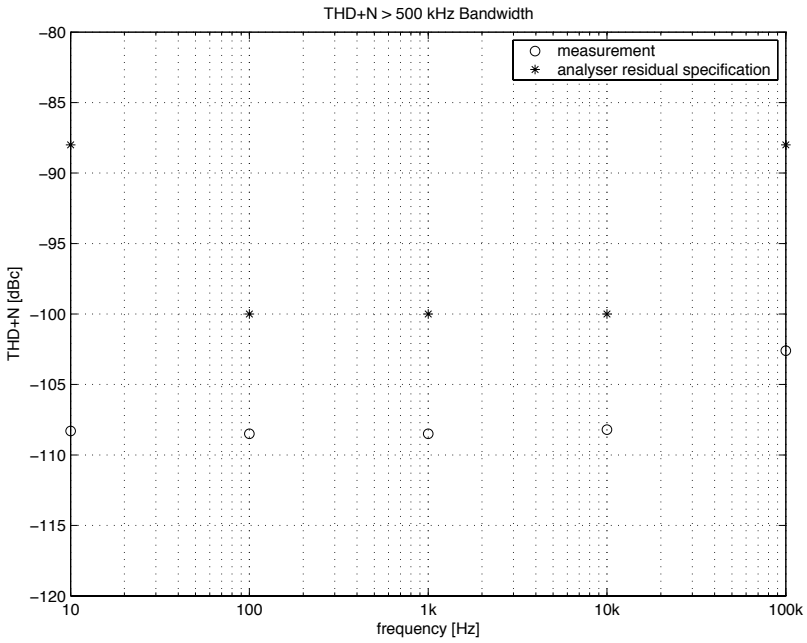


Figure 7.3: THD+N in a 500 kHz measurement bandwidth.

7.2 Amplitude Flatness

The amplitude flatness of the oscillator output from 10 Hz–100 kHz was measured using an Audio Precision SYS-2722 audio analyzer [7]; the results including measurement uncertainity are shown in figure 7.4. It is seen that the measured amplitude flatness is substantially better than the measurement uncertainity and well below the specifications as given in chapter 2.

7.3 Amplitude Settling Time

Only preliminary results for amplitude settling time can be shown here. Figure 7.5 displays the settling behaviour of oscillator amplitude and control voltage after a range change from 100 Hz to 1 kHz. The slope of the control voltage indicates that the specification of 1 s to 0.1 dB has been achieved. However it must be expected that for a range change from 1 kHz to 100 Hz settling time exceeds 1 s as settling time is typically proportional to the period of the new oscillation frequency. Preliminary research indicate that this could be improved by increasing the bandwidth of the track-and-hold stage of the level detector (see chapter 5). Verification of this must be left for future research.

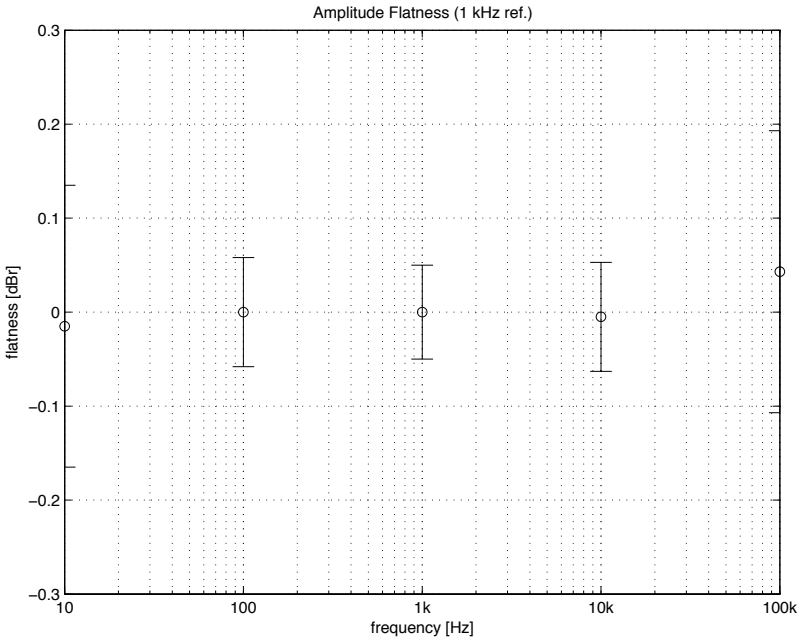


Figure 7.4: Amplitude flatness of the oscillator output relative to 1 kHz.

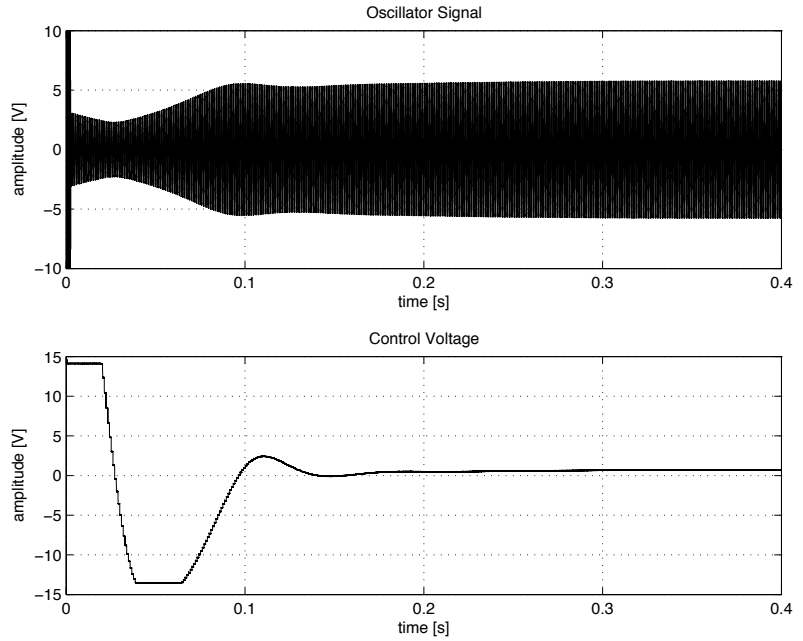


Figure 7.5: Settling time for a range change from 100 Hz to 1 kHz.

Chapter 8

Conclusion

The purpose of this thesis was the development of a sinusoidal oscillator with very low harmonic distortion ($-140\,\mathrm{dBc}$ in the audio frequency range) and an extended frequency range ($3\,\mathrm{Hz}$–$300\,\mathrm{kHz}$). As the intended distortion level of this oscillator design is beyond the resolution of available distortion analyzers exact verification of the overall performance was not possible. However four main distortion sources in RC oscillators with linear amplitude control can be recorded: distortion from passive components in the RC network of the oscillator, harmonic distortion of the amplifiers, finite level detector ripple and distortion in the multiplier. By isolated measurement of the distortion contribution of these four main distortion contributions a worst-case estimate for their total sum may be derived. In this thesis design criteria, new practical realisations and performance data for these four circuit elements were presented. By this design methodology it was ensured that any of the four main distortion contributions is made insignificant and that their total sum excels the design specification. In the following section we will discuss the results in detail and also present some topics for possible future research.

8.1 Passive Components

A new measurement technique to evaluate distortion in capacitors and resistors was presented. The new measurement procedure allows cancellation of oscillator and distortion analyzer residual contribution which have previously limited measurement resolution. This cancellation is achieved by two consecutive measurements where in the second measurement the device under test is replace by a series-parallel connected array of components of the same part type as the device under test. This array has the same nominal impedance as the device under test but much lower distortion as the voltage across the single components is halfed. By subtraction of this second

measurement from the first measurement the actual distortion of the device under test is revealed. A necessary condition for this new measurement technique is consistent (i.e. time invariant) distortion contribution from the oscillator source, the distortion analyzer as well as a resistor which is employed in the measurement. A technique for verification of this condition is introduced. By using this new measurement procedure it was found possible to verify distortion in passive components at 1 kHz with a resolution of −140 dBc to −150 dBc which represents an improvement of an order of magnitude compared to previous measurement techniques.

Also considered was distortion from thermal self-modulation in resistors which may become significant at very low frequencies. Direct measurement with sufficient resolution was not possible due to limitations in the oscillator source but negligible distortion contribution from this mechanism to the overall oscillator performance has been assured by several means; these include the choice of resistors with low temperature coefficient and the reduction of resistor power dissipation.

8.2 Operational Amplifier

In this thesis a new discrete amplifier was discussed which considerably surpasses previously known amplifiers with respect to distortion. Furthermore this new amplifier offers very low noise, excellent power supply rejection and good DC precision. To achieve this performance a new amplifier topoloy was designed; its main feature is a new second stage arrangement which results in the mentioned power supply rejection improvement and also enhances distortion performance. Several design techniques were presented to ensure good DC precision of the new amplifier topology. Also the reduction of harmonic distortion in the power supply current (which may induce into other circuit elements) of the operational amplifier was considered.

8.3 Level Detector

A new level detector design was presented in this thesis which offers considerably lower ripple than prior art level detectors. The new level detector uses a known architecture which senses the peak amplitude of the oscillator signal by sampling techniques. Limitations in the sampling stages however have restricted the performance—in particular the ripple content—of previous designs; the new level detector uses improved sampling stages which offer reduced feedthrough and hold droop. This is achieved without degrading the accuracy, amplitude flatness and response speed to amplitude changes of the previous level detector designs.

8.4 Multiplier

Prior art RC oscillators have suffered from significant multiplier distortion and noise contribution. The new multiplier circuit presented here offers significantly reduced contributions. It is based on a translinear gain cell which is operated at bias conditions which trade-off for both good noise and distortion performance. Special linearisation techniques for the preceding voltage-to-current converter stages are presented. The reduction in distortion and noise which is observed with the new multiplier design is achieved together with a dependable gain constant which is important for settling time and amplitude stability considerations.

8.5 Future Research

As discussed above exact distortion performance verification of this oscillator design was not possible due to residual contributions of available distortion analyzers. Future research could consider the design of a notch filter with sufficiently low distortion contribution; particularly suitable for such are passive notch filters due to the inherent absence of significant amplifier distortion contribution [65]. While such topologies are difficult to design for high frequency resolution distortion verification at a selected set of fixed frequencies may be sufficient.

The oscillator design as presented in this thesis does not yet include an output stage which enables level setting and provides a floating differential output with suitable load driving capability; to make the oscillator useful for laboratory work the addition of such an output stage is necessary. Design and verification of a suitable circuit will be subject of future research. Similarly the addition of a dedicated power supply and appropriate casing will be necessary.

In chapter 3 a new measurement technique to evaluate distortion in passive components was discussed. However it was found that the oscillator residual contribution of the used Audio Precision SYS-2722 audio analyzer [7] limited achievable resolution at low frequencies despite the employed distortion cancellation. This prevented direct measurement of distortion from thermal self-modultion which might be expected in resistors. The newly available oscillator offers substantially reduced distortion contribution and direct measurement of thermal self-modulation is now considered practical once the output stage has been implemented. Future research could hence consider detailed investigation of this resistor distortion mechanism.

Appendix A

Appendix

A.1 Distortion in Capacitors

Figure A.1–A.7 show several capacitor distortion measurements. The voltage across the device under test was set to +20 dBu; for 10 nF and 100 nF capacitors the measurement frequency was set to 1 kHz and for 1 nF capacitors to 10 kHz. Due to the measurement procedure as described in chapter 3 the plots show 3rd harmonic readings which are 2.5 dB lower than the actual capacitor distortion.

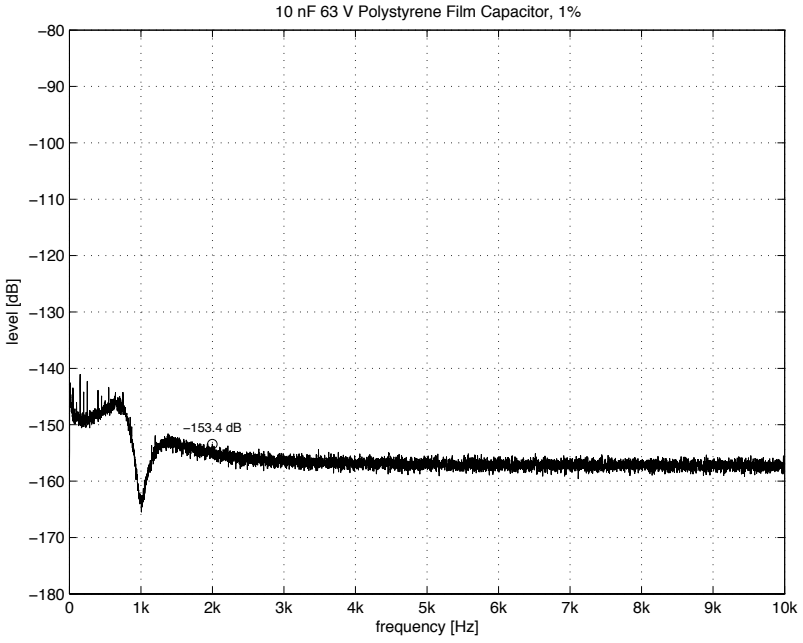


Figure A.1: Polystyrene film capacitor, LCR Components FSCEX, 10 nF, 63 V, 1 %.

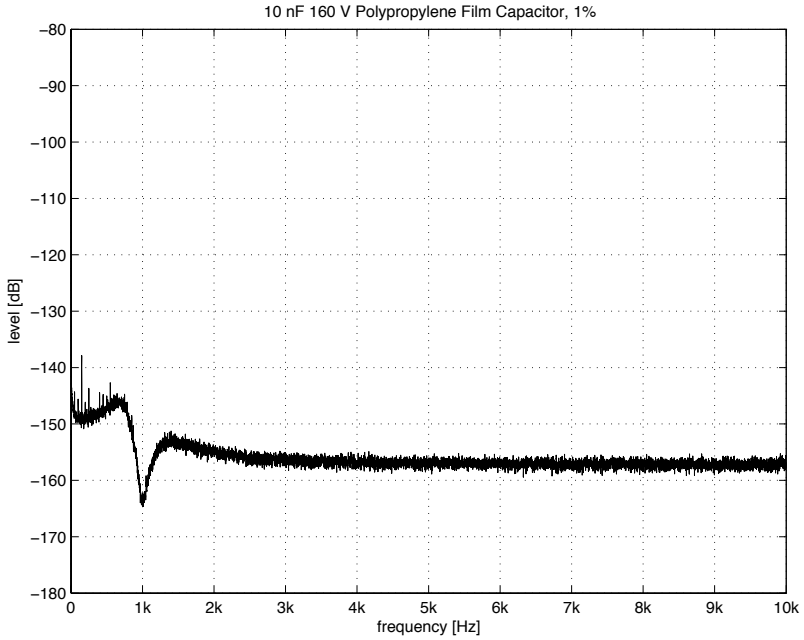


Figure A.2: Polypropylene film capacitor, Vishay Roederstein MKP 1837, 10 nF, 160 V, 1 %.

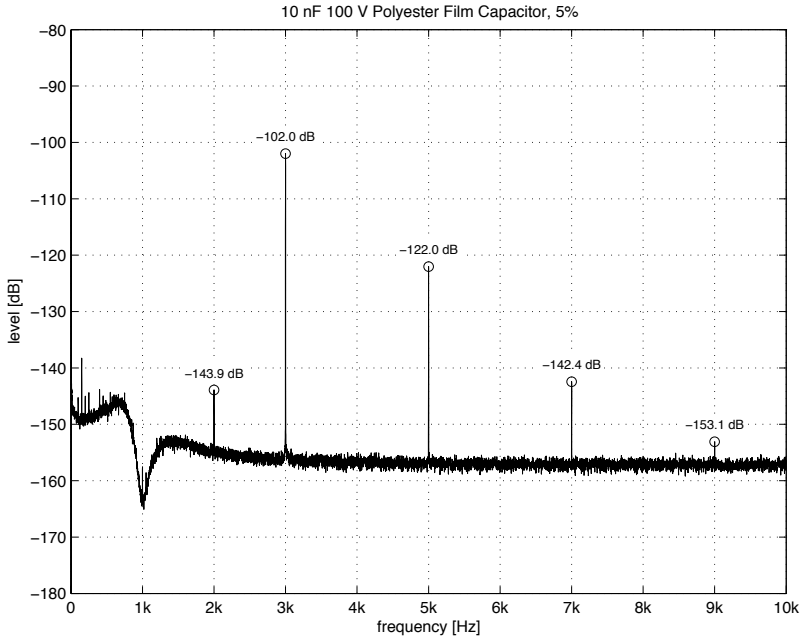


Figure A.3: Polyester film capacitor, Evox Rifa MMK5, 10 nF, 100 V, 5 %.

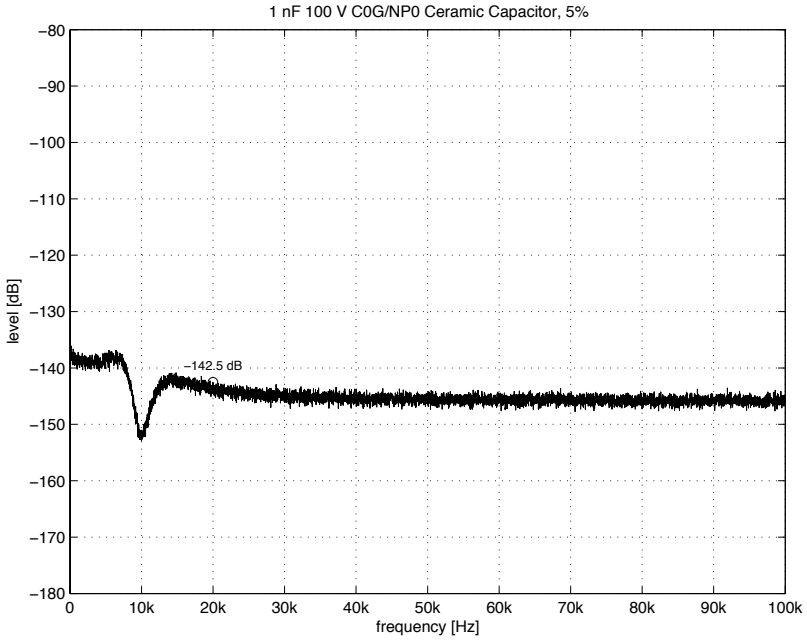


Figure A.4: Ceramic C0G/NP0 capacitor, Vishay Vitramon VJ, 1 nF, 100 V, 5 %. Measurement frequency increased to 10 kHz.

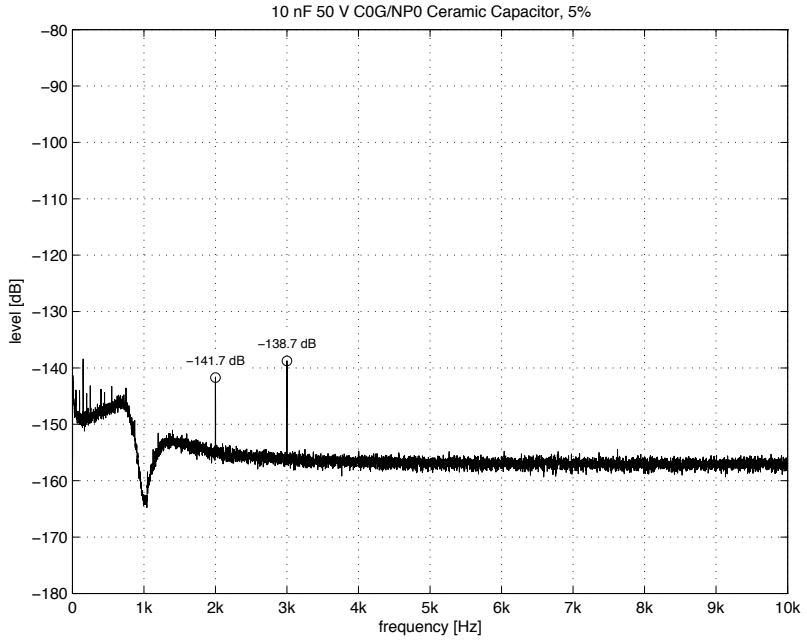


Figure A.5: Ceramic C0G/NP0 capacitor, Epcos B37986G, 10 nF, 50 V, 5 %.

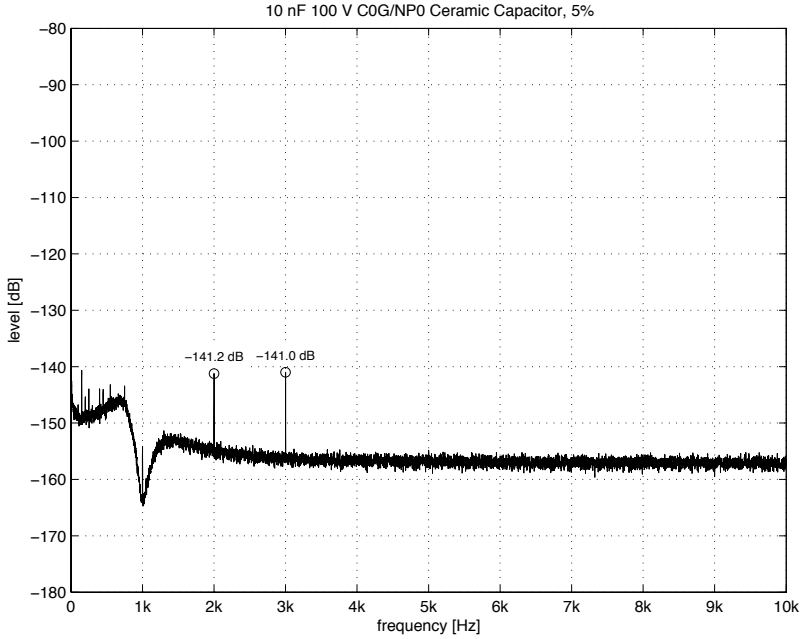


Figure A.6: Ceramic C0G/NP0 capacitor, Murata GCM31, 10 nF, 100 V, 5 %.

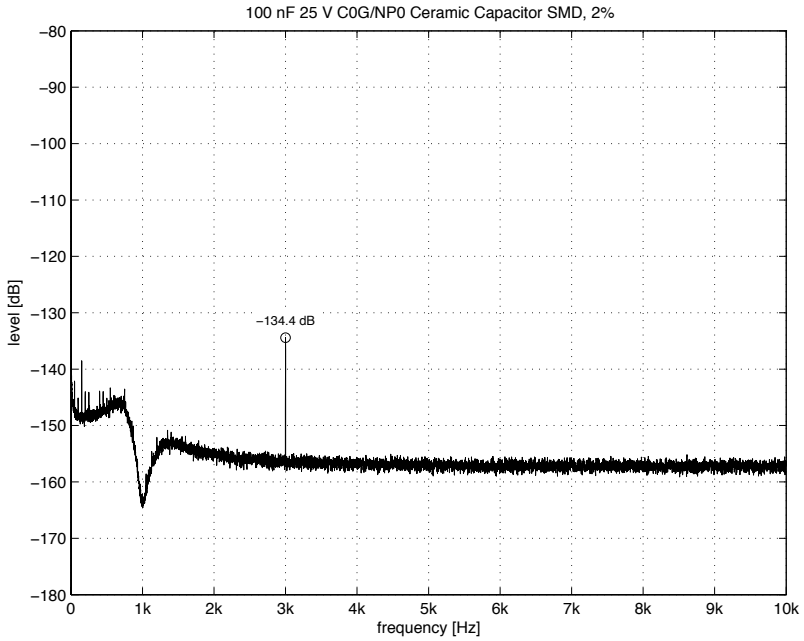


Figure A.7: Ceramic C0G/NP0 capacitor, Murata GRM31, 100 nF, 25 V, 2 %.

A.2 Distortion in Resistors

Figure A.8–A.13 show several resistor distortion measurements. The voltage across the device under test was set to +20 dBu and the measurement frequency to 1 kHz. Due to the measurement procedure as described in chapter 3 the plots show 3rd harmonic readings which are 2.5 dB lower than the actual resistor distortion.

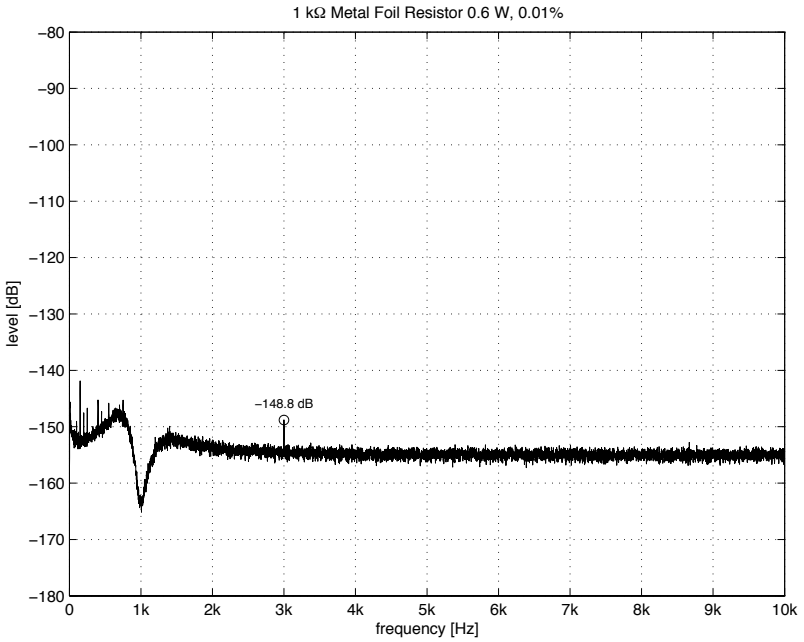


Figure A.8: Metal foil resistor, Vishay S102C, 1 kΩ, 0.6 W, 0.01 %.

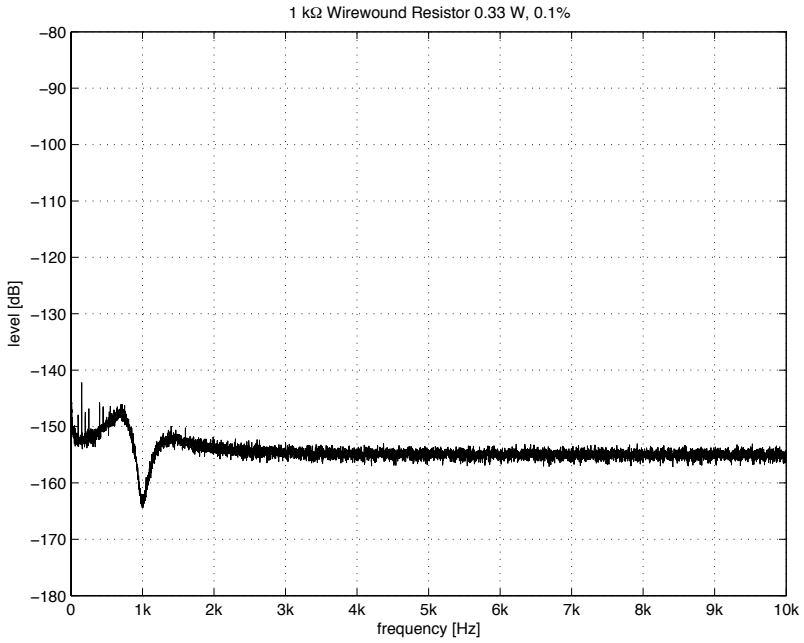


Figure A.9: Wirewound resistor, Rhopoint 8G16D, 1 kΩ, 0.33 W, 0.1 %.

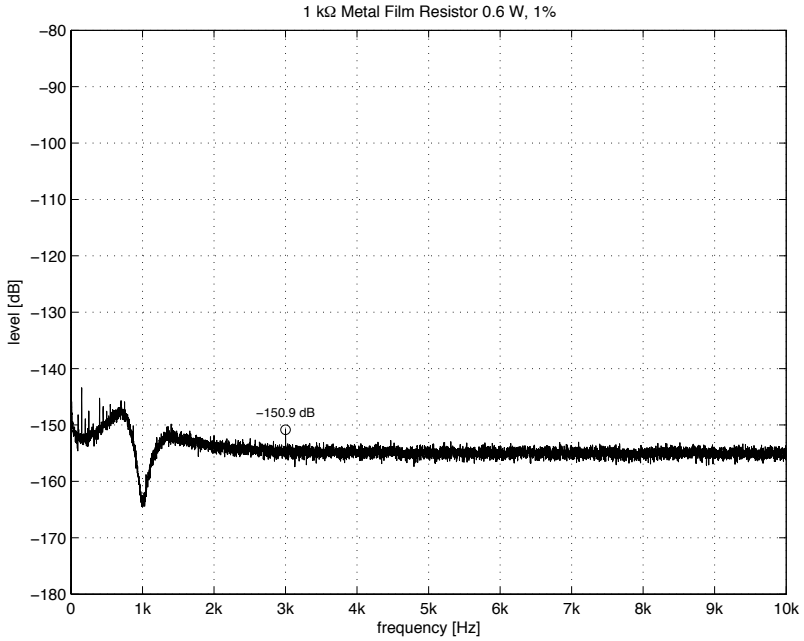


Figure A.10: Metal film resistor, Vishay Sfernice MRS25, 1 kΩ, 0.6 W, 1 %.

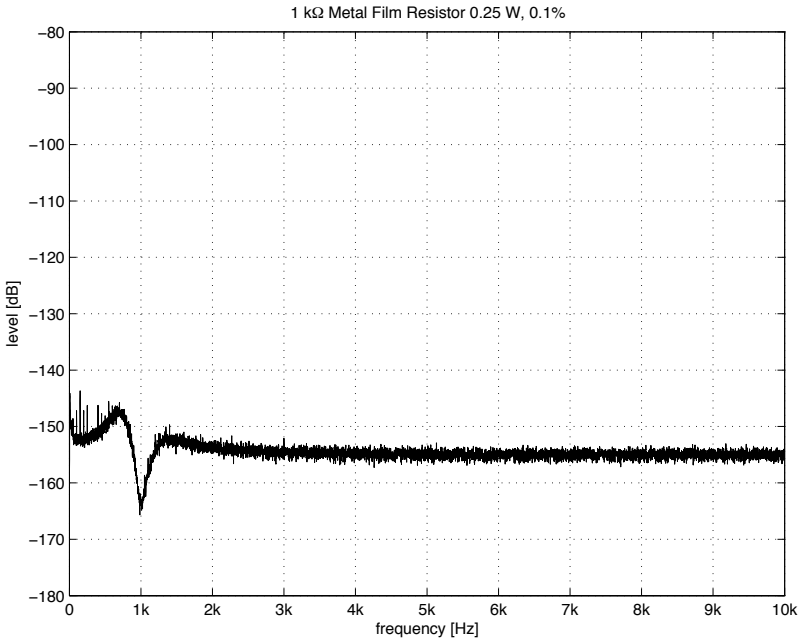


Figure A.11: Metal film resistor, Welwyn RC55Y, 1 kΩ, 0.25 W, 0.1 %.

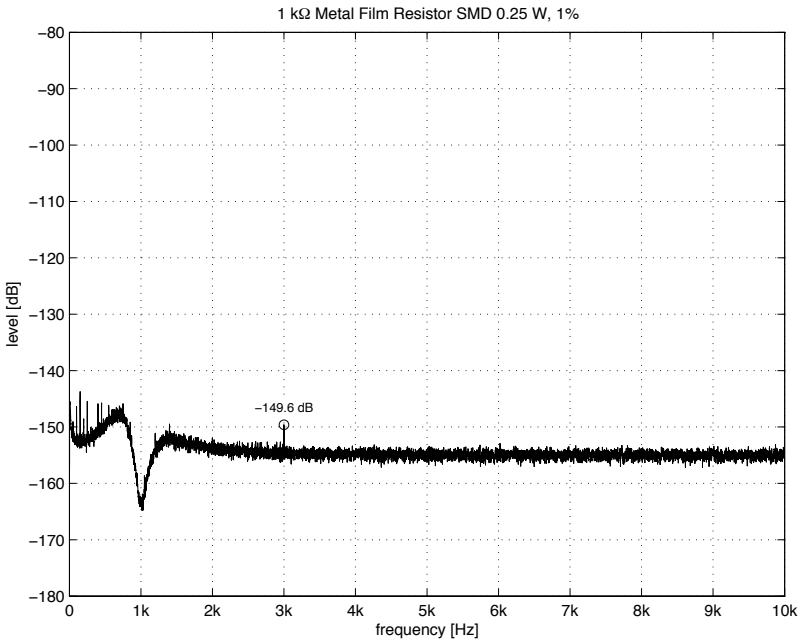


Figure A.12: Metal film resistor, Vishay MMA0204, 1 kΩ, 0.25 W, 1 %.

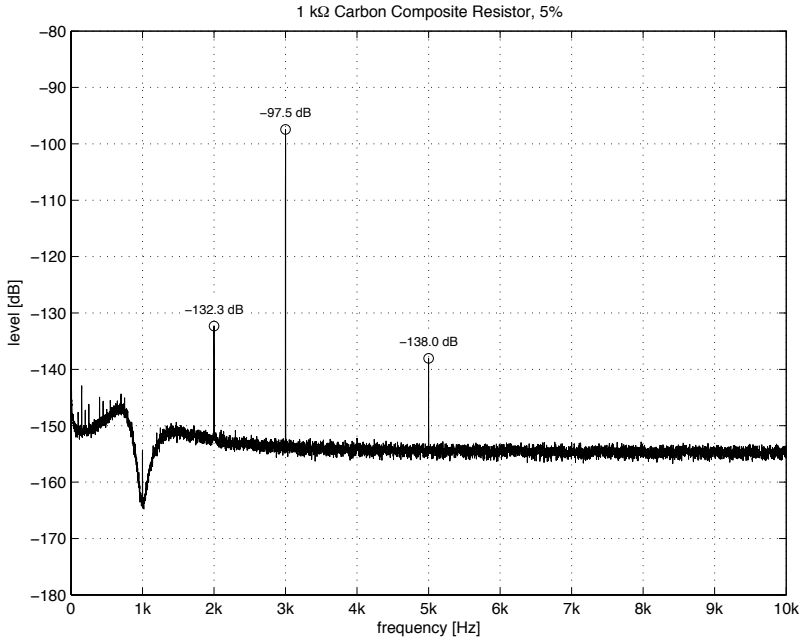


Figure A.13: Carbon composite resistor, unknown brand, 1 kΩ.

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