ReClockPi

Low noise low jitter double I2S/DSD re-clocker

By Ian Jin MAY.6, 2021 Ver. 0.9b

A. Introduction

ReClockPi is a low noise low jitter double re-clock logic board. It was designed to work with FifoPi or other digital music devices in sync mode to improve the I2S/DSD signal quality to a higher possible level.

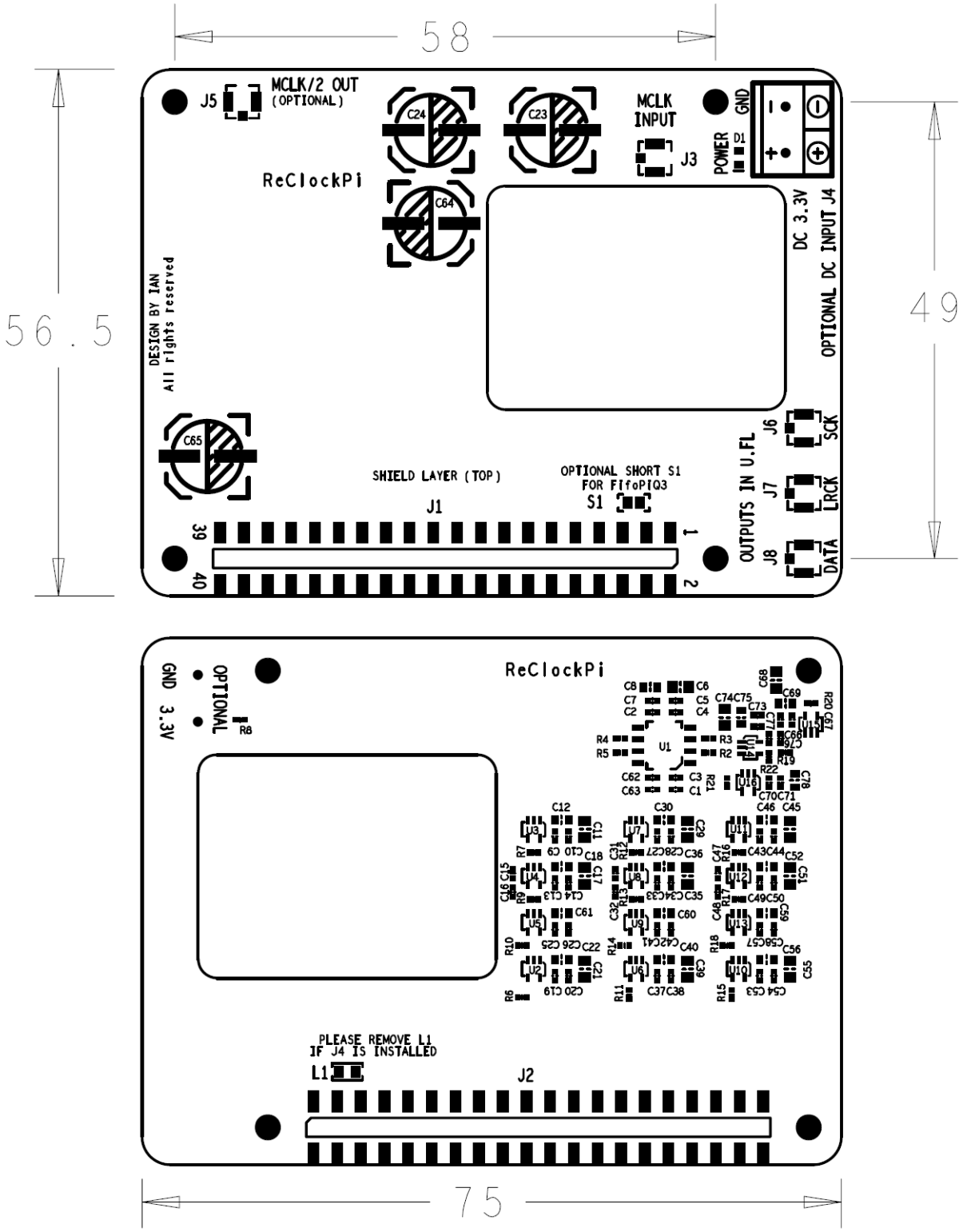
ReclockPi uses high speed discrete logic chips to solve the IR-drop issues of normal multi-bit flip-flop/counter based re-clocker, which could result in some high frequency synchronized re-clock ripples over both high and low logic levels. After upgrading a FifoPi with a ReClockPi, the I2S/DSD signal quality will be improved. The signal noise over the waveforms will be reduced and thus a lower jitter performance can be measured.

ReClockPi really makes a difference. It's so far the best solution to upgrade a FifoPi's performance even more. All digital audio applications that are sensitive to the I2S/DSD noise and jitter will be benefited from this ReClockPi.

B. Highlighted Features and Specifications

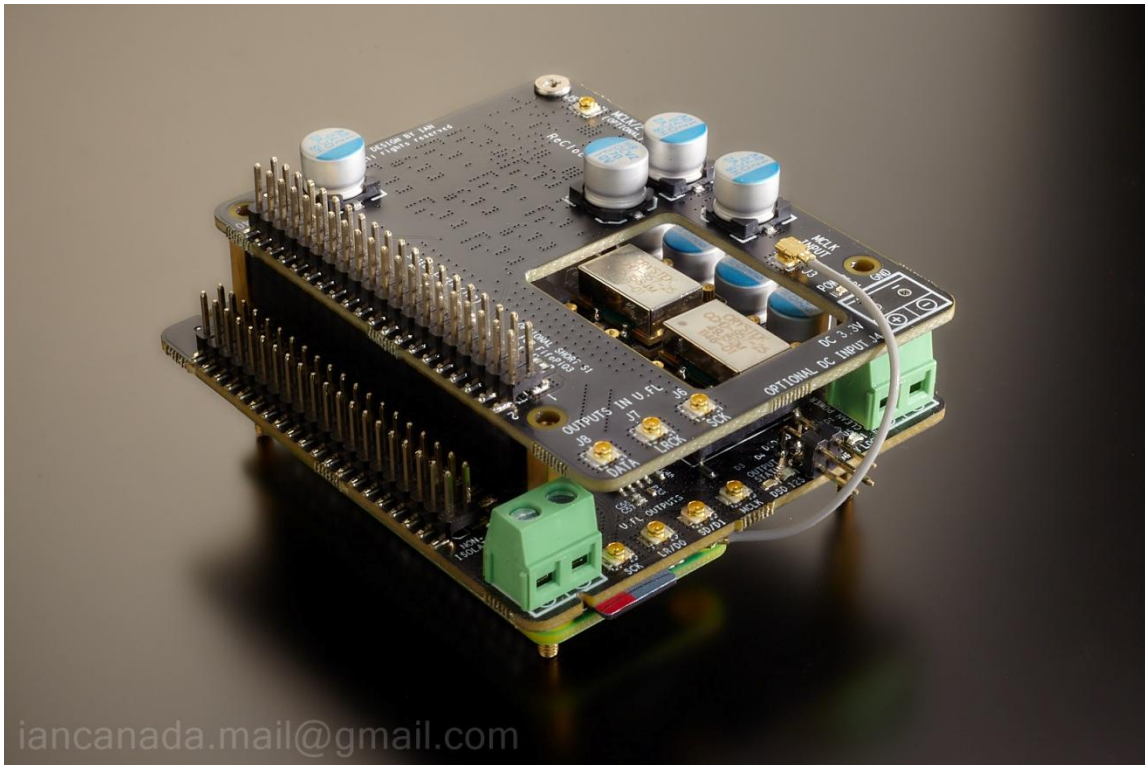
- Discrete double re-clock logic stage works as a digital music signal conditioner
- Low noise. The output signal noise over logic levels is much lower than the output signals from a multi-bit flip-flops/counters re-clocker.
- Low jitter. The I2S/DSD output time jitter = MCLK jitter + additive jitter of the discrete flip-flops.
- Independent shield layer on top of the four layers PCB to lower the EMI noise as same as a ShieldPi
- Upgrade a FifoPi right away by just plugging on top
- Optional half frequency MCLK output can be in lower phase noise
- Share power supply with a FifoPi clean side by default, can be upgraded to use an independent 3.3V external ultra capacitor or battery power supply.
- GPIO and U.FL dual I2S/DSD outputs
- Support PCM up to 768KHz and DSD up to DSD1024
- Reserve a window opening on PCB to work with taller XOs or XO adapters on a FifoPi

C. Layout and Dimensions (in mm)



D. Getting start

1. Install the ReClockPi into the isolated GPIO connector on top of a FifoPi.
2. Connect a MCLK u.fl cable to J3 from a FifoPi MCLK output (at bottom side is preferred).
3. Install the DAC or other audio HATs on top of ReClockPi.
4. It is still recommended use the MCLK from the FifoPi. But as alternative, there will be no any problem to use the MCLK/2 output from J5 on the ReClockPi.
5. Enjoy the music.



E. Connectors

J3: MCLK input in u.fl coaxial cable socket

Must be connected to a u.fl MCLK output of a FifoPi to operate.

I2S/DSD outputs in u.fl coaxial cable socket

J6: re-clocked SCK/BCK output
J7: re-clocked LRCK/DL output
J8: re-clocked DADA/DR outpu
It is recommended to use u.fl coaxial cables to connect to an external DAC or other audio devices
All output signals are in LVTTL (3.3V) logic levels

J5: MCLK/2 output in u.fl coaxial cable socket

This is a 1/2 frequency MCLK output. Theoretically the phase noise would be -6dBc/Hz better than the original MCLK from the FifoPi. However, even with the new designed high performance discrete re-clock logic circuit, it can still have some additive jitter less then 1ps RMS. So, the time jitter of this MCLK/2 could be a little bit higher than the MCLK form a FifoPi.

If that's the case, I would still recommend using the MCLK from the FifoPi. But if you need lower frequency MCLK for your DAC or other audio devices, or you just want to try something different, you will have no problem using the MCLK/2 from J5 as an alternative option.

MCLK/2 form J5 is in LVTTL (3.3V) logic levels.

40 pin GPIO connectors

pin numbers	**J2** 40 PIN GPIO connector to board below (Normally a FifoPi)	**J1** 40 PIN GPIO connector to HAT on top (DAC or other audio board)
1,17	3.3V from preceding board	Same 3.3V from preceding board
2,4	FifoPi clean side power supply	Same FifoPi clean side power supply
6,9,14,20, 25,30,34, 39	GND	GND
12	SCK input	Re-clocked SCK/BCK output
35	LRCK/DL input	Re-clocked LRCK/DL output
40	SD/DR input	Re-clocked SD/DR output
3	I2C DA	I2C DA
5	I2C CL	I2C CL
8	TXD0	TXD0
10	RXD0	RXD0
All other pins	same pins from preceding board	same pins from preceding board

Note: All input/output signals on the GPIO connectors are in LVTTL (3.3V) logic level except power and ground.

J4: Optional independent external 3.3V DC power input

By default, ReClockPi takes 3.3V power supply from the attached FifoPi. However, you can upgrade to an independent external 3.3V power supply by using this J4 DC input connector.

S1: Optional short jumper

Open by default.

When shorted, it will connect the ReClockPi 3.3V voltage rail together with the FifoPi clean side power supply. This option is only for working with a FifoPi Q3 or other FifoPi version with 3.3V clean side power supply.

Please also leave S1 open when use an external 3.3V power supply.

F. LED indicators

D1: Power indicator, indicating that the ReClockPi is powered

G. Application notes

1. How to use the optional jumper S1?

When working with a FifoPi Q3 or other version FifoPi that powered by a 3.3V power supply at the clean side, it is recommended to short the S1 by a solder iron to lower the power supply connection resistance.

Please don't do it if you use an external 3.3V power supply.

This step is just optional.

2. How to upgrade to an external independent 3.3V DC power supply by J4?

By default, ReClockPi takes 3.3V voltage from the FifoPi attached to. For the best possible performance, you can also upgrade the ReClockPi power supply to an external independent 3.3V DC power by J4.

To do so, you will need:

A. Remove L1 at bottom side of the ReClockPi PCB.

B. Solder a DC terminal block connector to the position of J4.
P/N:Phoenix Contact 1869664 (not supplied)

C. Connect an external 3.3V power supply (100mA or higher output current) to J4. Ultra low noise linear 3.3V power supply will be a basic option. 3.3V ultra capacitor power supply (like LinearPi+UcConditioner 3.3V) or LifePO4 battery power supply would be highly recommended.

PLEASE MAINTAINING CORRECT POLARITY!!!

3. Which MCLK should I use for my DAC or other audio devices?

It is still recommend using the MCLK from the FifoPi because it is the original parent clock. However, the MCLK/2 from J5 of the ReClockPi will be a good alternative and could be sounded differently. You can also try this MCLK/2 from J5 in case:

A. You need a lower frequency MCLK

B. Accounting to your personal preference.

4. Why a ReClociPi can improve sound quality?

A. ReClockPi can reduce the I2S/DSD signal noise
Most multi-bit flip-flop/counter based re-clocker circuits have IR-drop issue, which could result in some high frequency re-clock ripples (synchronized to MCLK) over both high and low logic levels. Though those ripples have no business with time jitter and close-in phase noise, but they are still some kind of noise which can be modulated to the DAC and other sensitive audio devices outputs in some degree. ReClockPi eliminates those IR-drop noise thus better sound quality will be expected.

B. ReClockPi can reduce I2S/DSD signal time jitter
ReClockPi uses high speed discrete logic chips to perform a precision double re-clock function. The I2S/DSD jitter can be reduced even more. Sound quality of DACs and other digital audio devices that are sensitive to the I2S/DSD jitter will be benefited from the ReClockPi.

C. ReClockPi can reduce EMI noise

ReClockPi uses the top layer of its four layers PSB as a shield layer. This feature is exactly as same as a ShielePi. The shield layer can provide an additional shield to the DAC and other audio devices to reduce overall EMI noise. That will be positive to the sound quality.

5. What is the most common issue if a ReClockPi doesn't work correctly?

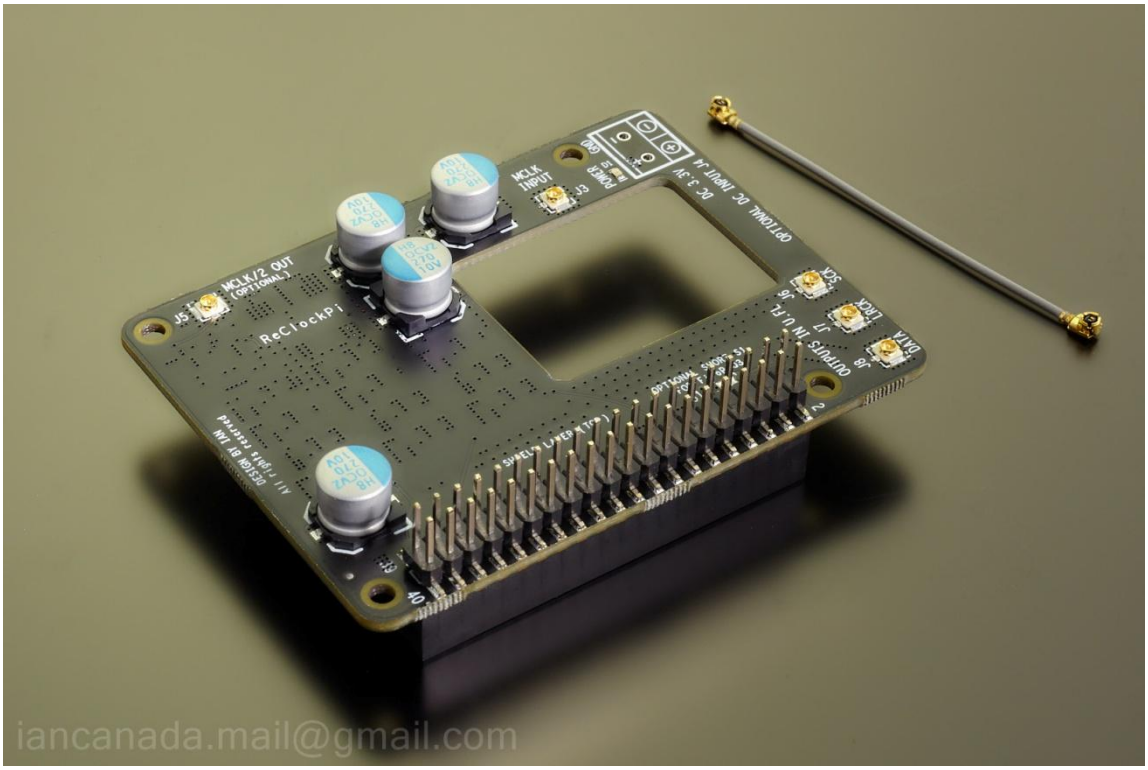
Please check/replace the u.fl MCLK cable first and make sure it fit properly into the u.fl connectors at both side. ReClockPi rely on the MCLK to function. It won't work correctly if the MCLK wasn't connected well.

6. What must be very careful when install a ReClockPi?

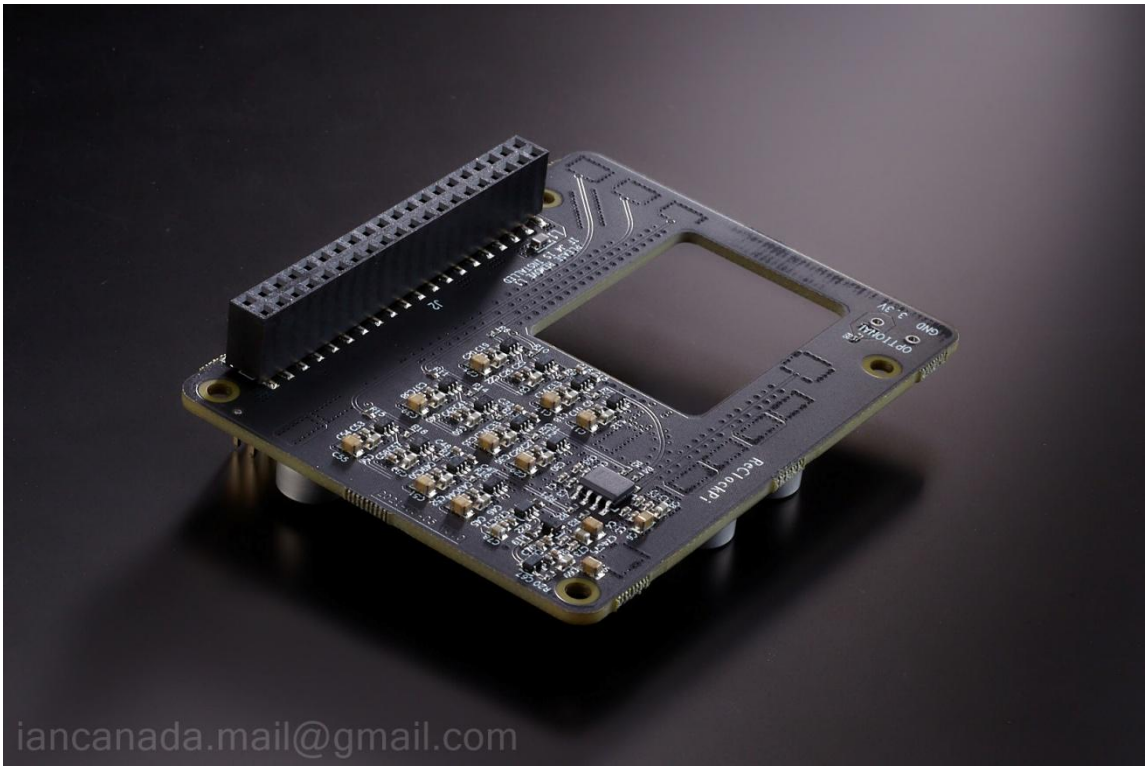
When the GPIO connector is plugged in at wrong position with shift, the power supply can be short to GND. PCB damaged could be expected if turn on the power supplies under this situation. It must be very careful to install the ReClockPi into GPIO socket correctly and make sure pin to pin are at right position.

H. Pictures ReClockPi

1. ReClockPi as shipped



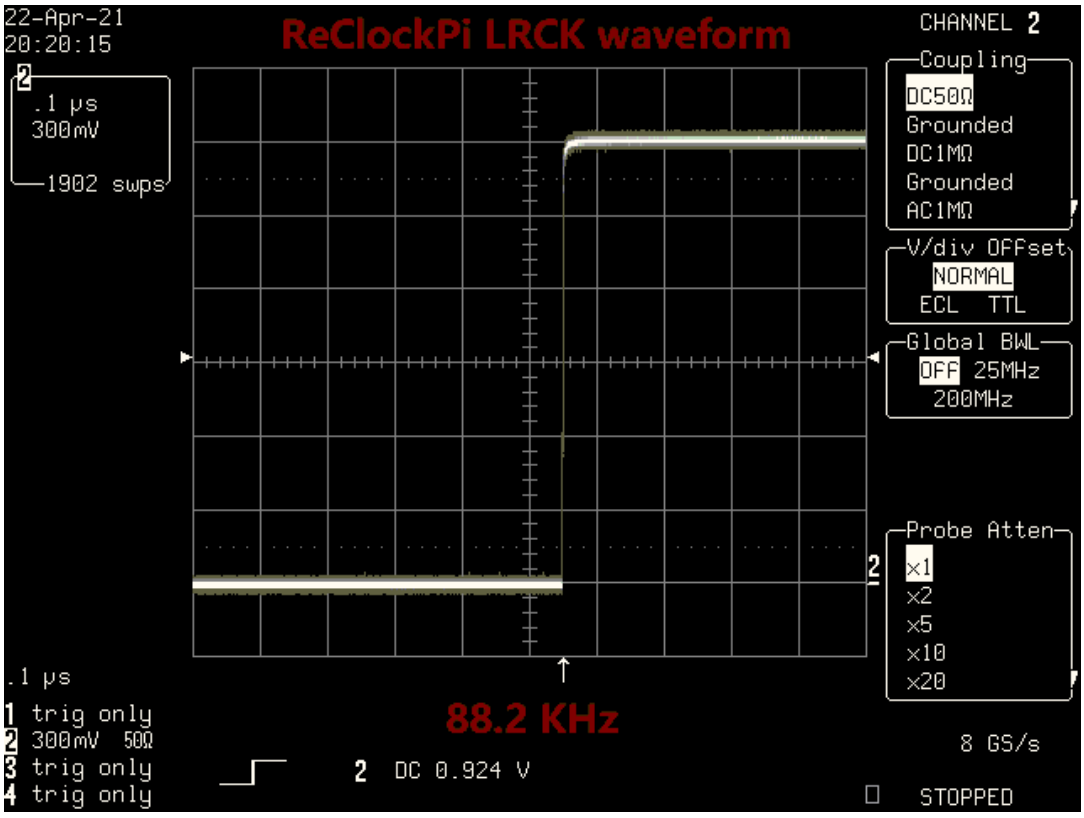
2. The PCB back side of a ReClockPi

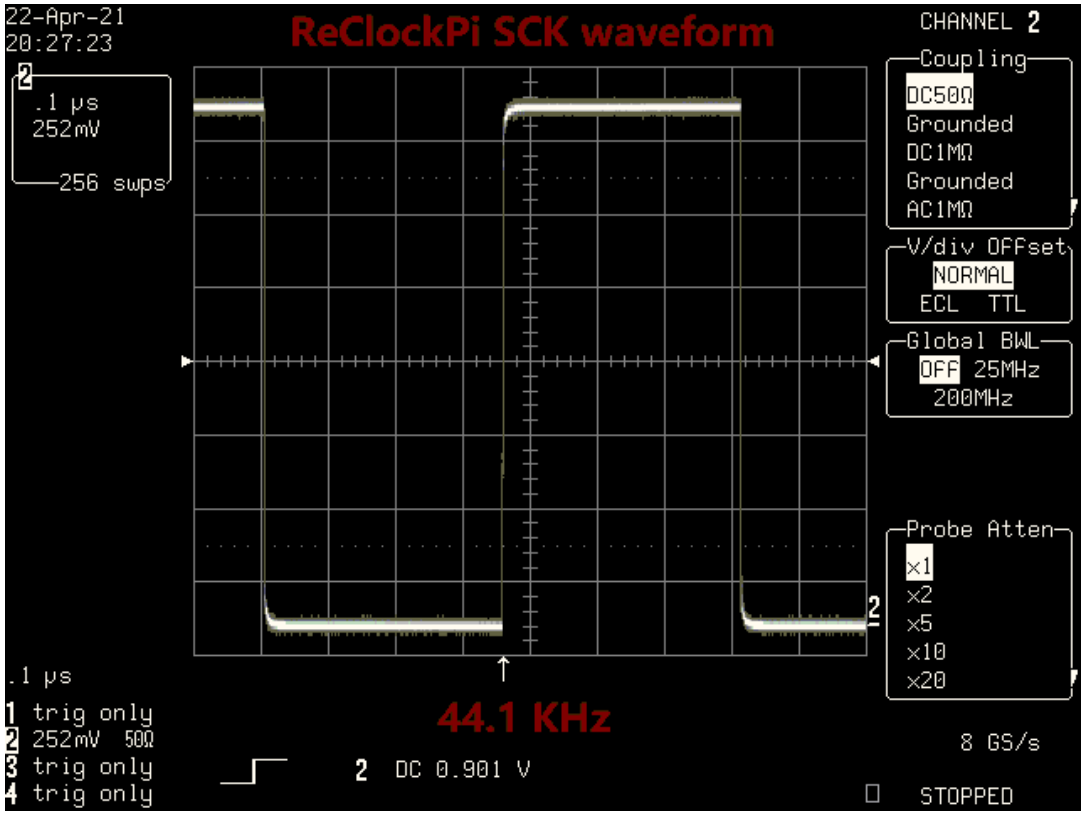


3. ReClockPi works with a FifoPi Q3 that has tall external XO adapters installed

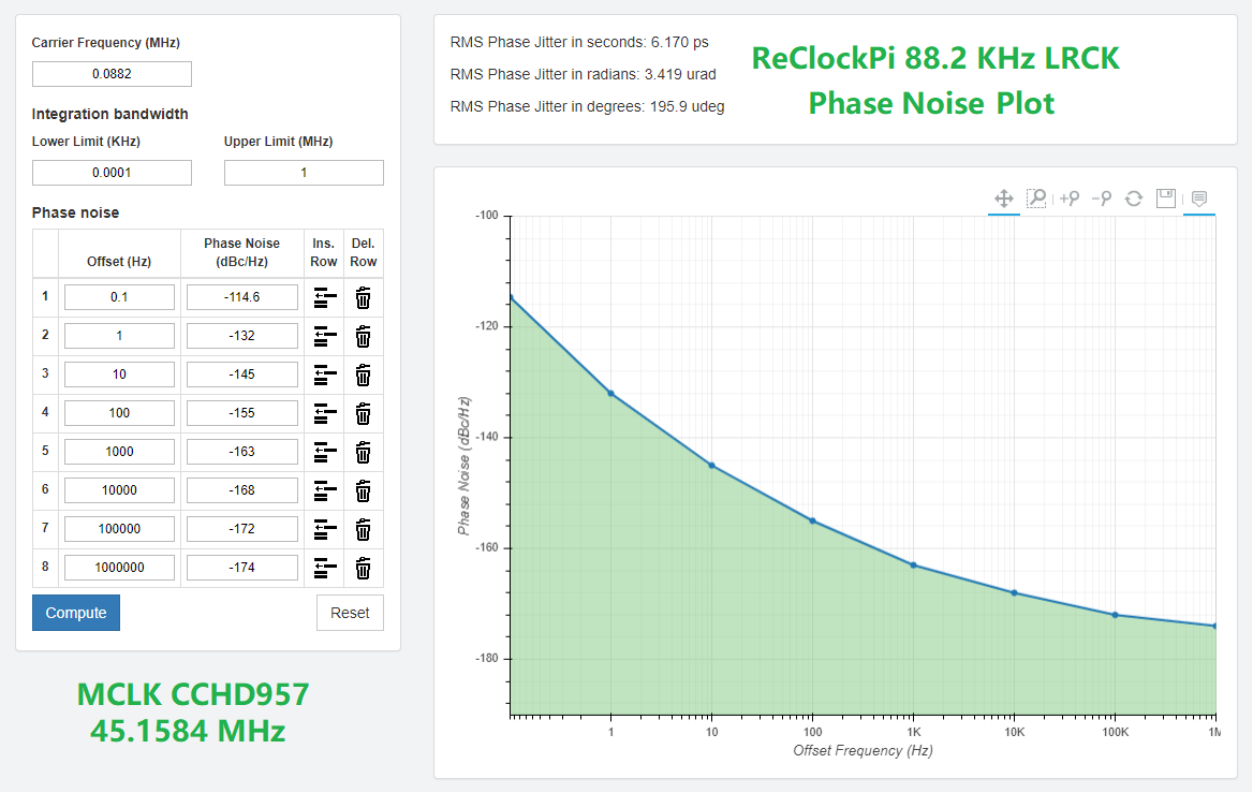
I. Measurement results

ReClockPi LRCK and SCK output waveforms

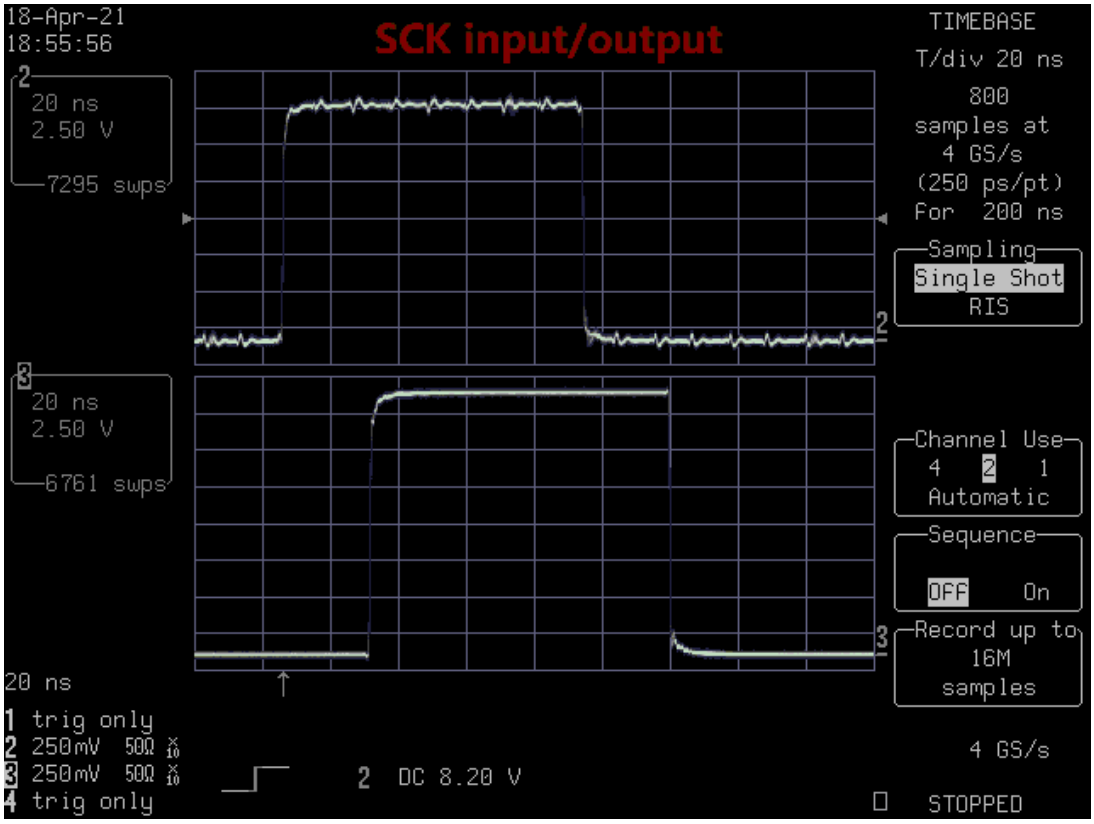


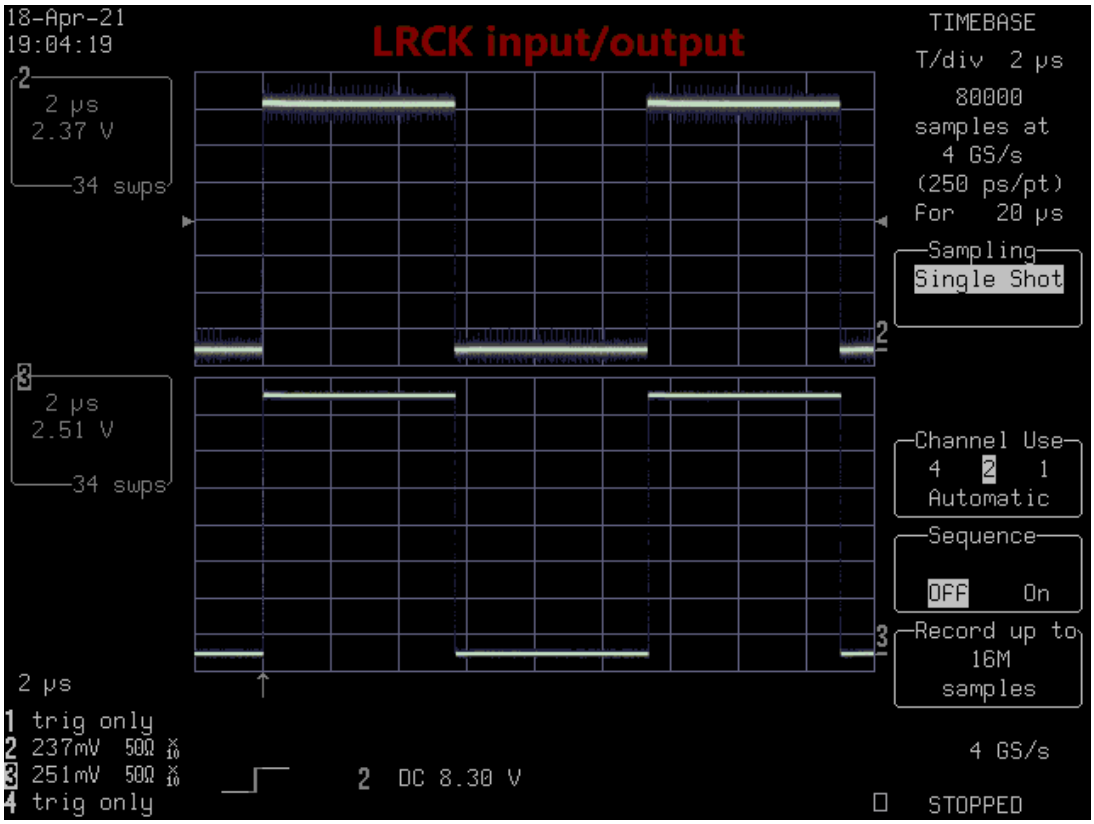


Estimated LRCL phase noise plot



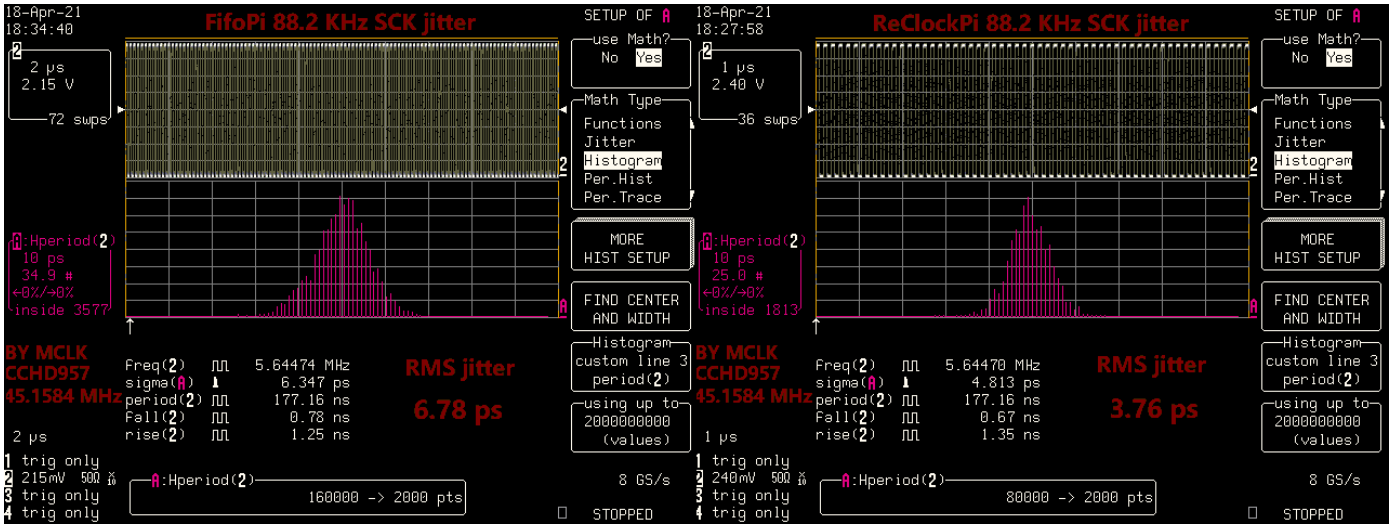
Estimated SCK phase noise plot



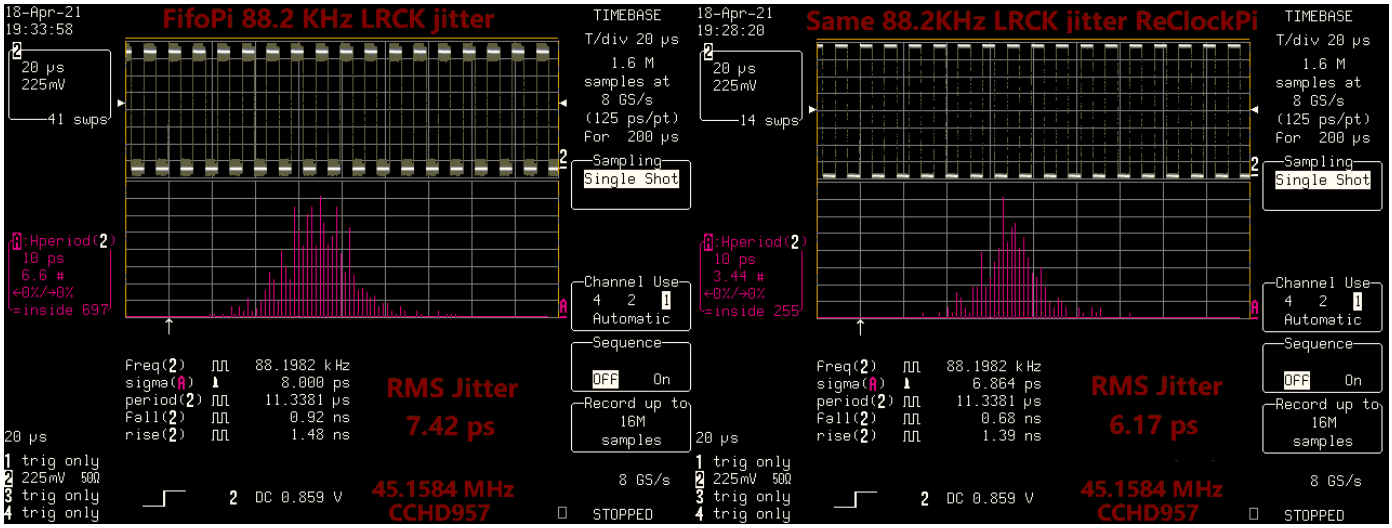


iancanada.mail@gmail.com

SCK input/output signal time jitter



LRCL input/output signal time jitter



J. History of revising

MAY. 6, 2021 V0.9b released