equal to $-\omega_t/2$. In the closed-loop gain G, however, an additional pole $-1/CR$, associated with the feedback network itself appears. Although this pole never causes ringing, it slows down the step response no matter how fast the operational amplifier may be. Therefore, in practice, we are satisfied with a partial compensation $C < C_x$, which corresponds to a state near the aperiodicity limit.

The condition of aperiodic settling,

$$\omega_t CR \geq 2\sqrt{(\omega_t C_x R - 1)}, \tag{7.32}$$

which follows from the solution of Eqs. (7.30) and (7.31), yields for $f_t = 10$ MHz, $C_x = 5$ pF, and $R = 10$ kΩ a minimum value of the compensating capacitor $C = 4.7$ pF.

The correct value of the compensating capacitor is best found experimentally (Figure 7–15). This enables secondary effects (operational amplifier excess phase shift, load capacitance, resistor shunt capacitances), which were neglected in the analysis, to be taken into account as well.

7.4 Rate Error

The *rate error* is familiar to those involved with servomechanisms: As a result of dynamic limitations, the output shaft follows the control voltage with some delay, with an error proportional to the rate.

A similar error accompanies the behavior of an operational circuit excited by a variable input signal. In the frequency domain (see Chapter 6), the sine wave is such a signal. In the time domain, it is the *ramp*—a signal linearly increasing with time.

Some practical cases where it makes sense to judge the operational-circuit accuracy in this way are, for example, the programmable potentiostat, the automatic titrator, the sawtooth resolver, or the resistor-trimming machine.

7.4.1 Noninverting Amplifier Rate Error

In a fashion similar to the step response, we relate our considerations to a particular operational circuit (Figure 7–16), the noninverting amplifier with a gain

$$G = \frac{G_I}{1 + s/\omega_c},$$

$$G_I = \frac{R_2}{R_1} + 1, \qquad \omega_c = \frac{\omega_t}{G_I},$$

according to Section 5.4.1. The input signal is a voltage linearly increasing with time at a rate w_s starting from $t = 0$.

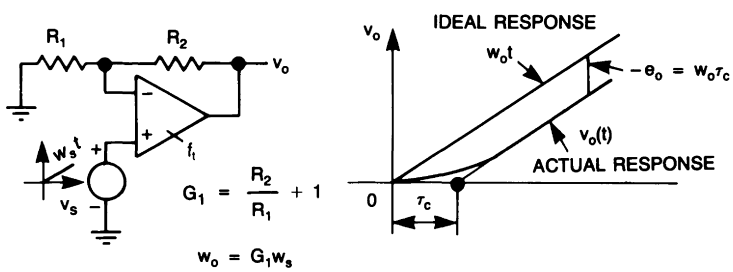

Figure 7–16. Rate error of a noninverting amplifier excited by a ramp.

If the amplifier has been at rest for a sufficient time, it can be considered to be in the steady state. Then, the Laplace transform of the output voltage is

$$v_o(s) = G\frac{w_s}{s^2} = \frac{G_I w_s}{s^2(1 + s/\omega_c)},$$

from which the time-domain equivalent is found to be

$$v_o(t) = G_I w_s\{t - \tau_c[1 - \exp(-t/\tau_c)]\}.$$

The output voltage comprises an ideal component

$$v_{oI} = G_I w_s t = w_o t, \tag{7.33}$$

on which an error component is superimposed. In the last expression we have denoted

$$w_o = G_I w_s, \tag{7.34}$$

as the rate of the output ramp.

After a short exponential transient with a time constant $\tau_c = 1/\omega_c$, the error voltage $e_o = v_o - v_{oI}$ settles to a steady value

$$e_o = -w_o\tau_c. \tag{7.35}$$

This easy looking task is, in fact, quite difficult. For illustration's sake, we take a precision operational amplifier (f_t = 1 MHz) connected as a noninverting amplifier with a gain G_I = 1000 and a time constant τ_c = 160 μs, which is excited by an input ramp at a rate of w_s = 1 V/s. The corresponding output rate w_o = 1 V/ms equals the maximum slope of a sine wave with an amplitude of 10 V and frequency of 16 Hz. Even with this moderate excitation, the output voltage lags the ideal value $w_o t$ by an error voltage of $-e_o$ = 160 mV, or by a rate error of 1.6% from the 10-V output voltage range!

The interrelation of the rate error in the time domain and the dynamic vector error in the frequency domain, mentioned in Section 6.1.1, is not just academic. The investigated noninverting amplifier with crossover frequency f_c = 1 MHz/1000 = 1 kHz would process the 16-Hz sine wave with exactly the same vector error of ϵ_V = 16 Hz/1 kHz = 1.6%.

This result can be generalized, at least for all first-order resistive operational circuits. The rate error voltage $-e_o$ of an operational circuit excited to an output ramp with a rate w_o, related to the rated output voltage V_o, is equal to the vector error ϵ_V of the same operational circuit excited to an output sine wave with amplitude V_o and frequency f_w, at which the maximum slope of the sine wave equals the slope of the ramp:

$$-\frac{e_o}{V_o} = \epsilon_V(f_w) = \frac{f_w}{f_c} \quad \text{for} \quad 2\pi f_w V_o = w_o. \tag{7.36}$$

A proof is trivial. The relationship [Eq. (7.36)] is simply another form of Eq. (7.35).

The relationship [Eq. (7.36)] forms a basis for the following concluding statement. The indicators of operational-circuit dynamic accuracy based on continuous signal excitation (vector error for a sine wave, rate error for a ramp) are, in general, much more unfavorable than those based on pulse signal excitation (settling time following a step between two constant levels).

To be specific, a voltage follower with a crossover frequency of f_c = 1 MHz excited by a 10-V step settles to an error of 0.01% in 1.5 μs (we have

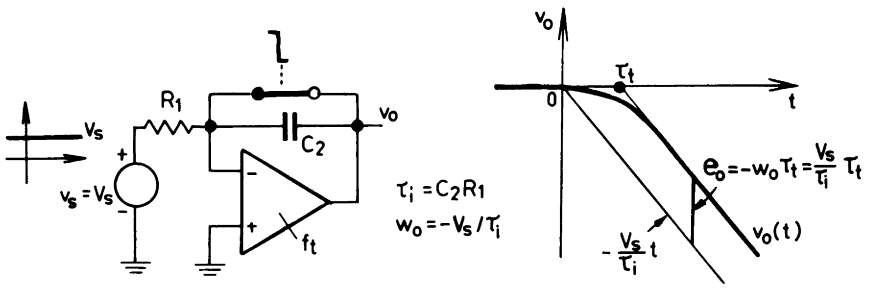

Figure 7–17. Rate error of an integrator. The output ramp is started by turning the switch off.

an exponential settling in mind) and can repeat such steps at least 500,000 times per second. The same voltage follower transmits a sine wave with a vector error of 0.01% only up to 100 Hz.

7.4.2 Integrator Rate Error

The integrator produces an output ramp by itself, by integrating a constant input voltage (Figure 7–17). According to Section 5.4.3,

$$e_o = V_s \frac{\tau_t}{\tau_i} = -w_o \tau_t. \tag{7.37}$$

The integrator rate error increases with increasing speed of integration; that is, with decreasing integrator time constant τ_i. A slow integrator (τ_i = 1 s, f_t = 1 MHz) integrates the input voltage V_s = 10 V with a negligible rate error of e_o = 1.6 μV. A fast integrator (τ_i = 10 μs, f_t = 10 MHz) integrates the same input voltage with a considerable rate error of e_o = 16 mV or 0.16% from 10 V.

7.5 Measurement of Settling Time

Measurement of settling time of a high-speed operational amplifier to an error of 0.01% is one of the most difficult dynamic measurements. Often, this becomes a test of the experimenter, a test of his/her ability to critically evaluate the measured data (4).

7.5.1 Settling of Voltage Inverter

For the *voltage inverter* (3, 4, 8, 9), a test circuit for measuring the voltage-inverter settling time presented in Figure 7–18 is an analogy to that used for measuring the vector error in Figure 6–24. At the artificial summing junction of the normal resistors R_N, a voltage $e(t)$ is observed, which equals one-half of the output error voltage resulting from exciting the inverter by a pulse 0 V/ + 10 V or 0 V/ − 10 V. During measurement, the static error caused by resistor tolerances and the offset are disregarded since these are easily measurable at dc.

The test arrangement is first adjusted at a low pulse-repetition rate of 100 Hz to 1 kHz and a pulse width of 1 ms to 100 μs by means of the 10-Ω potentiometer in such a way that the settled trace, observed on the screen of an oscilloscope set to full sensitivity, does not show any step. During this slow run, an eventual long tail is revealed that might otherwise be regarded as an error of the test setup and, as such, unjustifiably nulled out.