The standard recovery rectifiers used in the rectifier bridge must accommodate the highest average current expected which occurs at the ac low-line voltage. This has been calculated during the predesign estimates (black box considerations). The rated forward current should be more than 2 A and minimum blocking voltage should be twice the maximum high ac line crest voltage. This is more than 764 V. A 1N5406 would be a good choice.

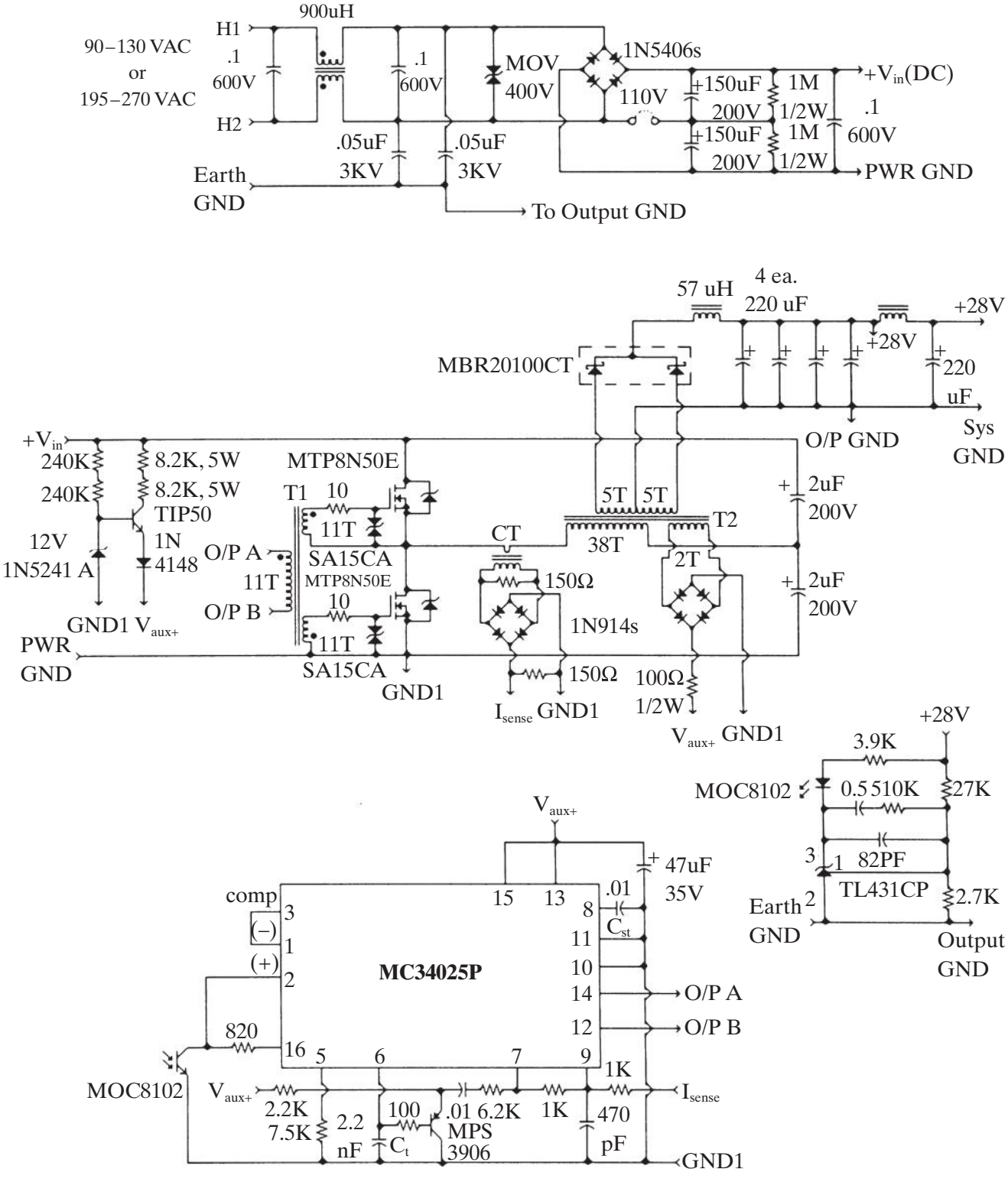

Figure 3–77 Schematic of a 100 kHz, 280 W, half-bridge converter.

Design of the controller circuitry

The overall control strategy will be current-mode control. The industry standard controller is the UC3525N or the MC34025P. The IC can be configured as either a current-mode or voltage-mode controller. I will use the current-mode control configuration.

The oscillator frequency is set by referring to a timing graph. In order to provide a 100 kHz operating frequency, the values for RT and CT are

RT = 7.5 K ohms
CT = 2200 pF

The design of the current sensing circuit

I have decided to use a current transformer to sense the primary current waveform, since resistive methods are impractical in the half-bridge topology. Several transformer manufacturers make current transformers for such a purpose wound on a toroidal core. Coilcraft makes current transformers with 50, 100, and 200 turns on their secondaries. The secondary voltage must be determined in order to have representative current waveforms of the level to work with the control IC. The voltage needed on the output of the current transformer is

$$V_{CT(sec)} \approx V_{sc} + 2V_{fwd} = 1.0\,V + 2(0.65) = 2.3\,V$$

Selecting a 100 : 1 ratio current transformer, the secondary current is given by

$$I_{sec} = (N_{pri}/N_{sec})I_{pri} = (3.1\,Amps)/100 = 31\,mA$$

The resistor needed to convert this current into the needed voltage is

$$R_{sc} = 2.3\,V/31\,mA = 75\,ohms$$

In order to improve the slope compensation circuitry that depends upon a resistor to ground all the time, I will split this resistor between the secondary winding of the current transformer and after the rectifiers. I will double the value of the two resistors (150 ohms each), so that when the diodes are conducting, the net value is the same.

It is necessary to add a small leading edge spike filter to the current sensing output. To keep the time delay to a reasonable value, I will use a 1 K ohm resistor and a 470 pF capacitor.

Slope compensation

Every current-mode control application that exceeds 50 percent duty cycle must have slope compensation on the current ramp waveform. Otherwise an instability will occur whenever the duty cycle exceeds 50 percent. This is typically done by summing into the current waveform some of the oscillator ramp waveform. This will increase the slope of the current waveform and therefore trip the current sense comparator earlier. A common problem is the inadvertent loading of the oscillator, so I will use a PNP emitter-follower to buffer the oscillator. The circuit configuration can be seen in Figure 3–74.

The design of the slope compensation circuit is almost fairly qualitative and may eventually need to be adjusted at the breadboard stage. To estimate how much additional ramp voltage is needed to keep the power supply stable, one performs the following equation. A_i is the gain or step-down influences of the transformers between the output and the current sense pin.