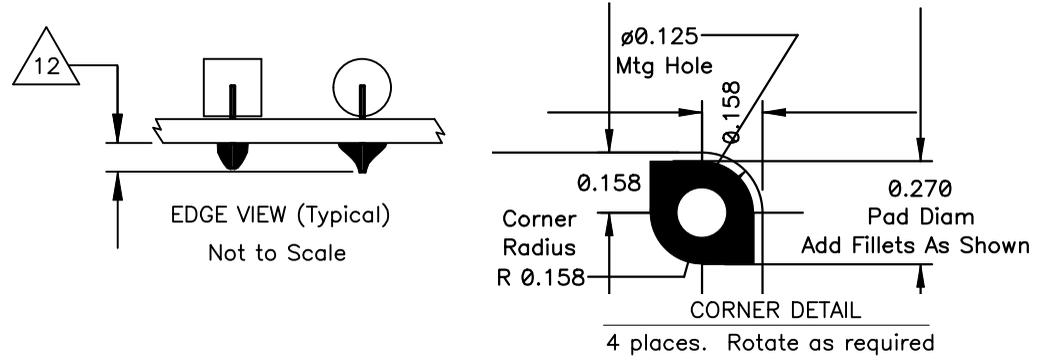
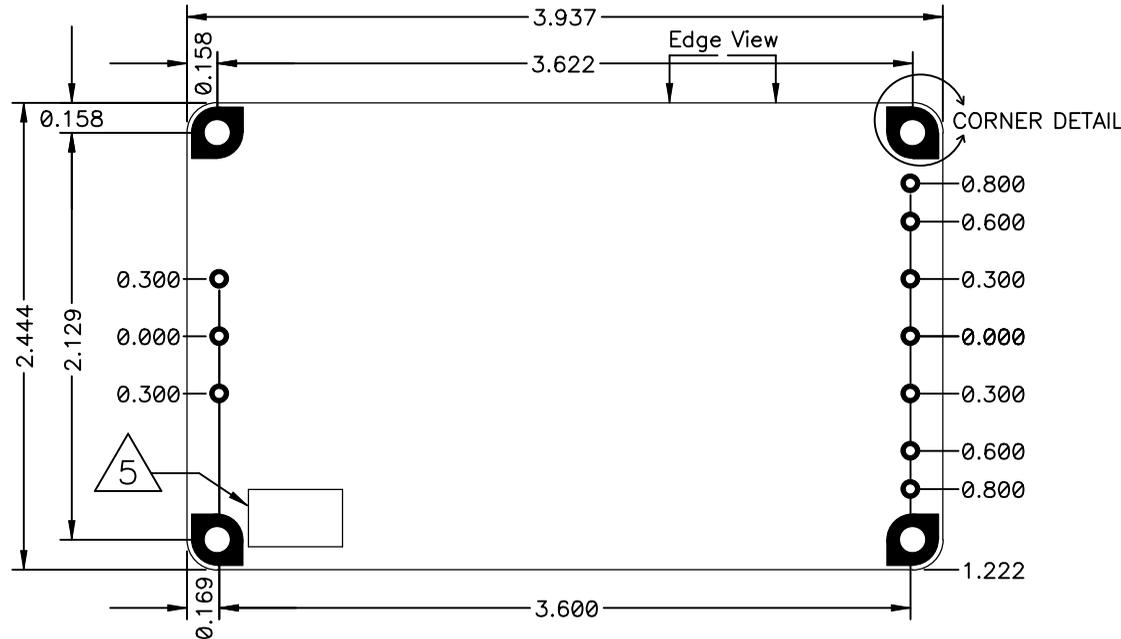
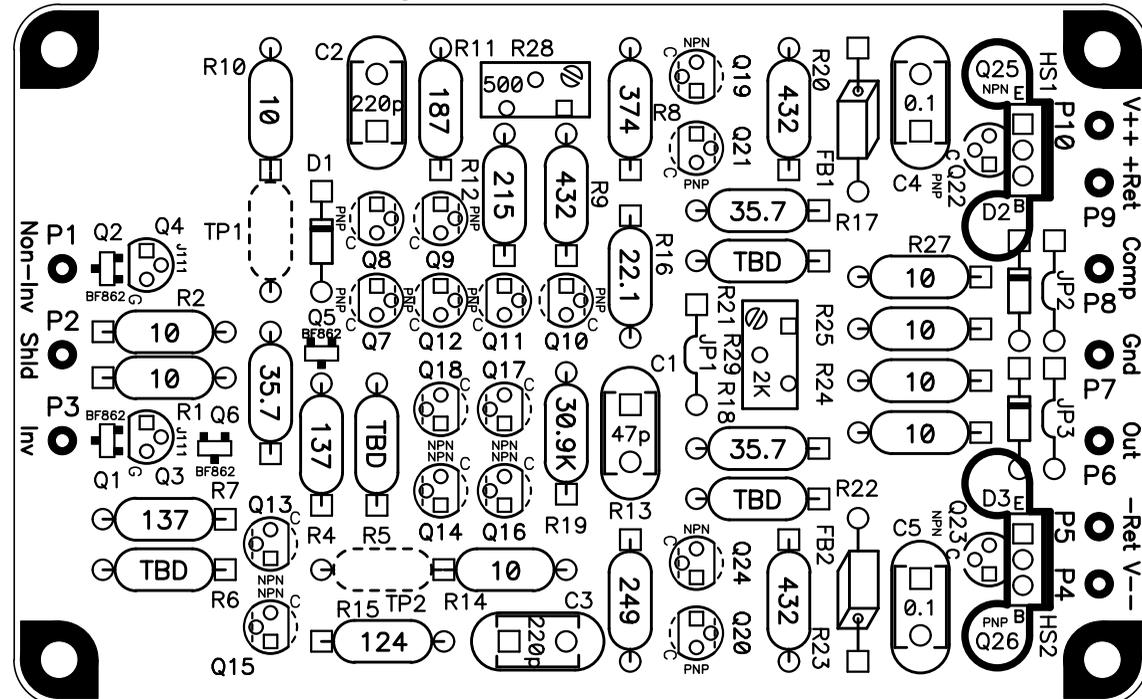


DIY AUDIO DISCRETE OPAMP
 SWOPA Disc Opamp THD1
 PWB DWG SWOPA2885PWB1 REV B



NOTES: UNLESS OTHERWISE SPECIFIED

- ALL MATERIALS ARE TO BE ROHS COMPLIANT. FABRICATE PER ANSI/IPC-A-600, IPC-QE-605, IPC-4101, IPC-4552 AND IPC-SM-840 SPECIFICATIONS.
- MATERIAL: BASE MATERIAL LAMINATED EPOXY GLASS (COLOR GREEN) .056 THK (.062 MAX) ROHS COMPLIANT FR-4 PER IPC-4101 SLASH SHEETS #26 OR #83 OR #98 WITH MINIMUM Tg 170 DEGREE C OR HIGHER, Td 340 DEGREE C OR HIGHER AND FLAME RATED UL 94V-0.
- SOLDERMASK BOTH SIDES OF BOARD OVER BARE COPPER WITH ROHS COMPLIANT MATERIAL PER ANSI/IPC-SM-840, COLOR SHALL BE GREEN.
- APPLY FINISH OR PLATING TO EXPOSED COPPER, BOTH SIDES AS SPECIFIED IN PURCHASE DOCUMENTS.
- INDICATED AREA ON BOTTOM SIDE AVAILABLE FOR APPLICATION OF PCB MANUFACTURE LOGO, UL MARKING, DATE-CODE AND ROHS COMPLIANT SYMBOL. USE OF OTHER LOCATION TO BE APPROVED BY PURCHASER.
- APPLY SILKSCREEN TO COMPONENT SIDE OF BOARD USING NON-CONDUCTIVE ROHS COMPLIANT WHITE EPOXY INK.
- SEE ARTWORK WITH SAME DRAWING NUMBER AND REVISION AS THIS DRAWING.
- HOLE LOCATIONS SPECIFIED IN SEPARATE DRILL FILE TAKE PRECEDENCE OVER THIS DWG AND ARTWORK. DIMENSIONS ON DWG TAKE PRECEDENCE OVER ARTWORK. TOLERANCE ARE: .XX=+/- .01; .XXX=+/- .005; ANGLES=2 DEG
- SEE SEPARATE DRILL FILE FOR HOLE LOCATIONS. SELECTED HOLE LOCATIONS SHOWN ON THIS DWG FOR REF ONLY.
- HOLE SIZES ARE SPECIFIED AS FINAL DIMENSIONS AFTER PLATING AND FINISHING. UNLESS OTHERWISE SPECIFIED ALL HOLES TO BE PLATED.
- HOLE PLATING TO BE AS SPECIFIED IN PURCHASE DOCUMENTS.
- TRIM SOLDER FILLETS AND COMPONENT LEADS TO 0.100" (MAX) BEYOND BOARD SURFACE ON BACK SIDE.
- DESIGN GEOMETRY MINIMUM FEATURE SIZES:
 TRACE WIDTH 10 MILS
 HOLE-TO-HOLE 15 MILS
 SILKSCREEN LINE 8 MILS
 TRACE-TO-TRACE; TRACE-TO-PAD; PAD-TO-PAD 10 MILS
 BOARD EDGE-TO-COPPER 20 MILS
 SILKSCREEN-TO-BARE COPPER 8 MILS



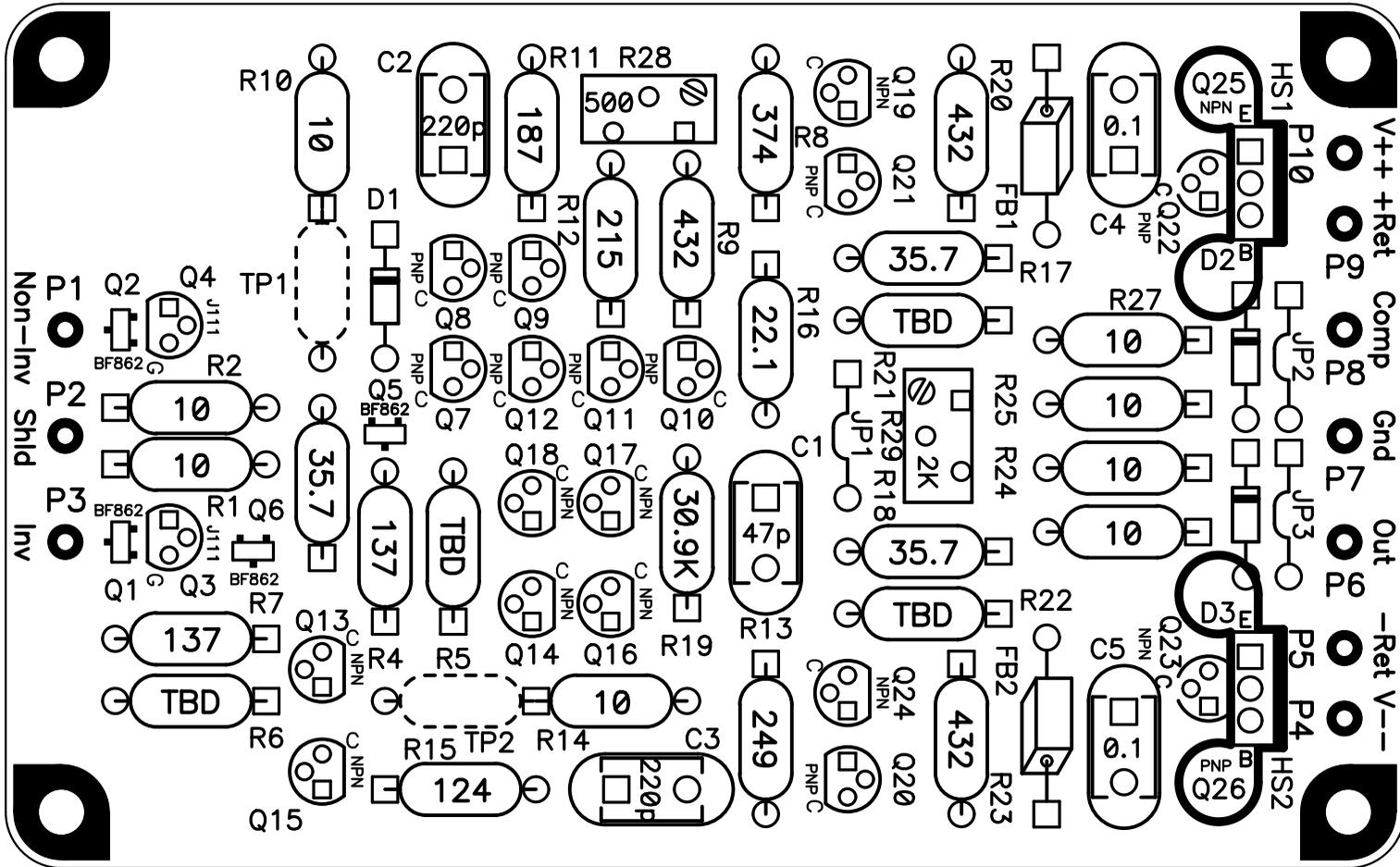
COMPONENT PLACEMENT

Solid transistor outlines for EBC pinout; dashed outlines for CBE pinout.
 Component values shown for ref only. See Parts List for correct values.

REVISION HISTORY

- DEFAULT TRACE WIDTH INCREASED TO 25 MILS; SOME TRACE WIDTHS FURTHER INCREASED. TRACE AND COMPONENT LOCATIONS ADJUSTED TO MAINTAIN SPACING.
- WORKING DWG FOR PRELIMINARY DEVELOPMENT. NOT RELEASED.

Title SWOPA DISC OPAMP THD(1) PWB		
Size 8.5x14	Number SWOPA2885PWB1	Rev B
Date Thu May 09, 2013	Drawn by D. Chisholm	
File SWOPA_Post2885PWB_B.pcb	Sheet of	

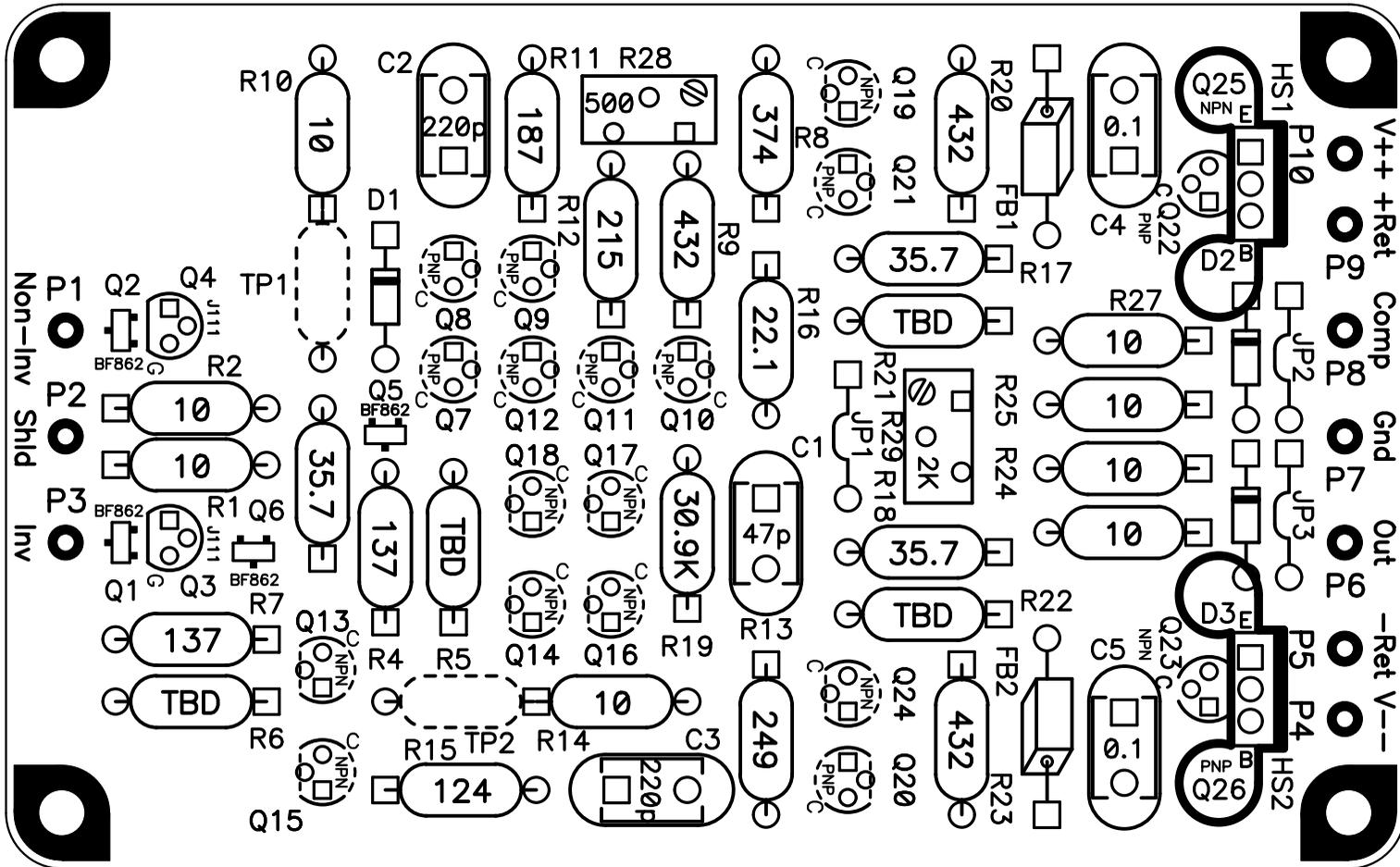


PARTS LOCATIONS FOR TRANSISTORS WITH EBC PINOUT

Component outlines shown for transistors with EBC pinout, such as 2N4401/2N4403.

Component values shown for ref only. See Parts List for correct values according to variant & Dwg Rev level.

Title SWOPA DISC OPAMP THD(1) PWB		
Size 8.5x14	Number SWOPA2885PWB1	Rev B
Date Thu May 09, 2013	Drawn by D. Chisholm	
File SWOPA_Post2885PWB_B.pcb	Sheet	of



PARTS LOCATIONS FOR TRANSISTORS WITH CBE PINOUT

Component outlines shown for transistors with CBE pinout, such as BC550/BC560.

Component values shown for ref only. See Parts List for correct values according to variant & Dwg Rev level.

Title SWOPA DISC OPAMP THD(1) PWB		
Size 8.5x14	Number SWOPA2885PWB1	Rev B
Date Thu May 09, 2013	Drawn by D. Chisholm	
File SWOPA_Post2885PWB_B.pcb	Sheet	of

A

B

C

D

E

F

1

1

2

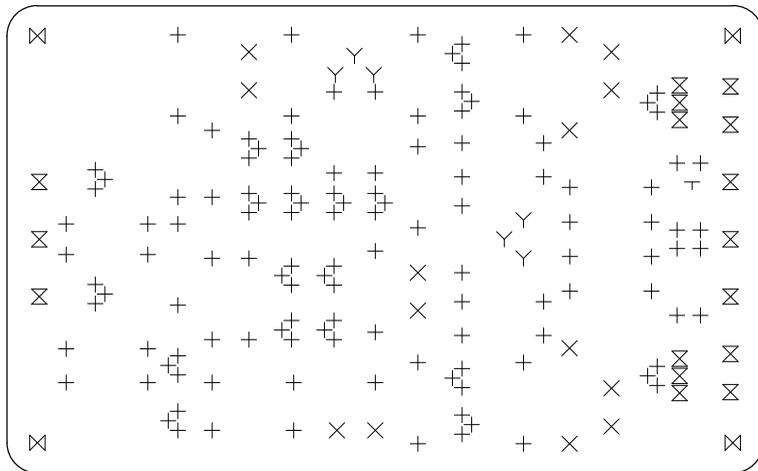
2

3

3

4

4



Drill Table			
Hole Dia (inch)	Symbol	Quantity	Plated
0.020	⊢	1	Yes
0.029	Y	6	Yes
0.032	+	128	Yes
0.036	X	14	Yes
0.043	⊗	16	Yes
0.125	⊠	4	Yes

Approx Hole Locations
 Refer to Excellon drill file for exact locations

Title SWOPA DISC OPAMP THD(1) PWB		
Size 8.5x14	Number SWOPA2885PWB1	Rev B
Date Thu May 09, 2013	Drawn by D. Chisholm	
File SWOPA_Post2885PWB_B.pcb	Sheet	of

A

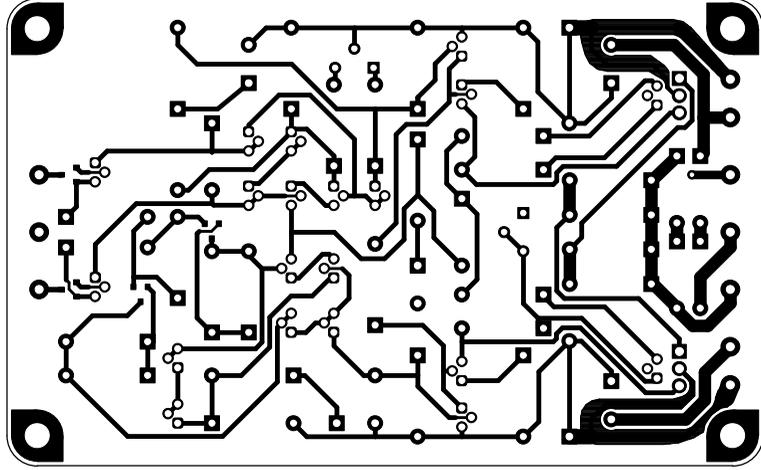
B

C

D

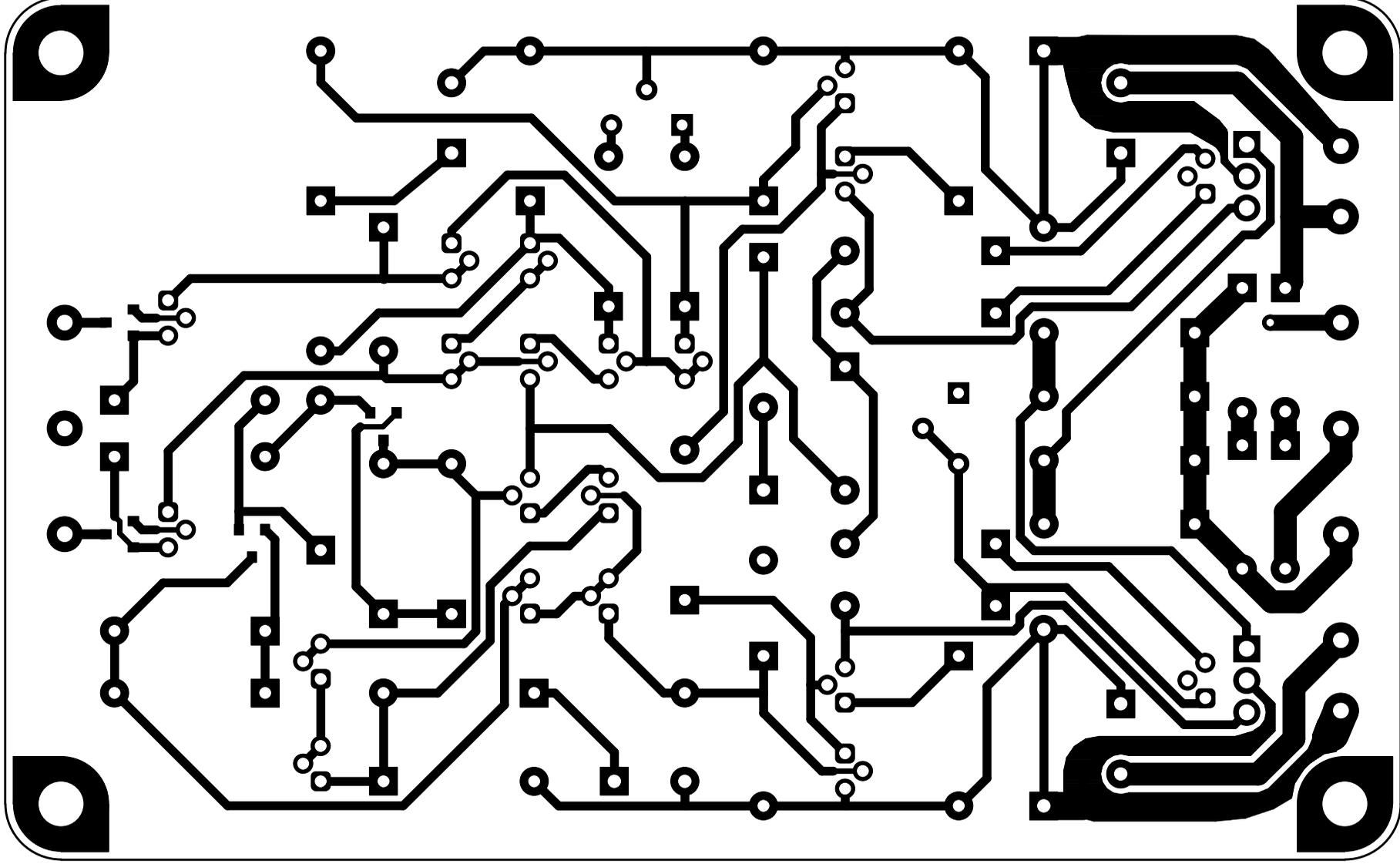
E

F

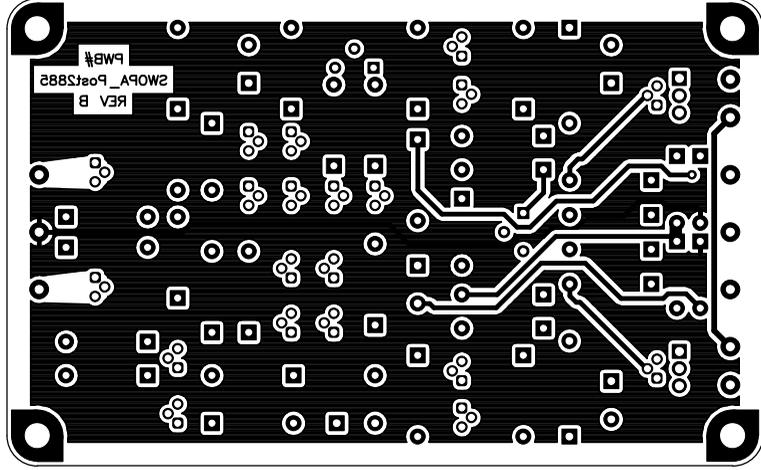


TOP CIRCUIT LAYER

Title			SWOPA DISC OPAMP THD(1) PWB		
Size	Number			Rev	
8.5x14	SWOPA2885PWB1				B
Date	Thu May 09, 2013		Drawn by		D. Chisholm
File	SWOPA_Post2885PWB_B.pcb		Sheet		of

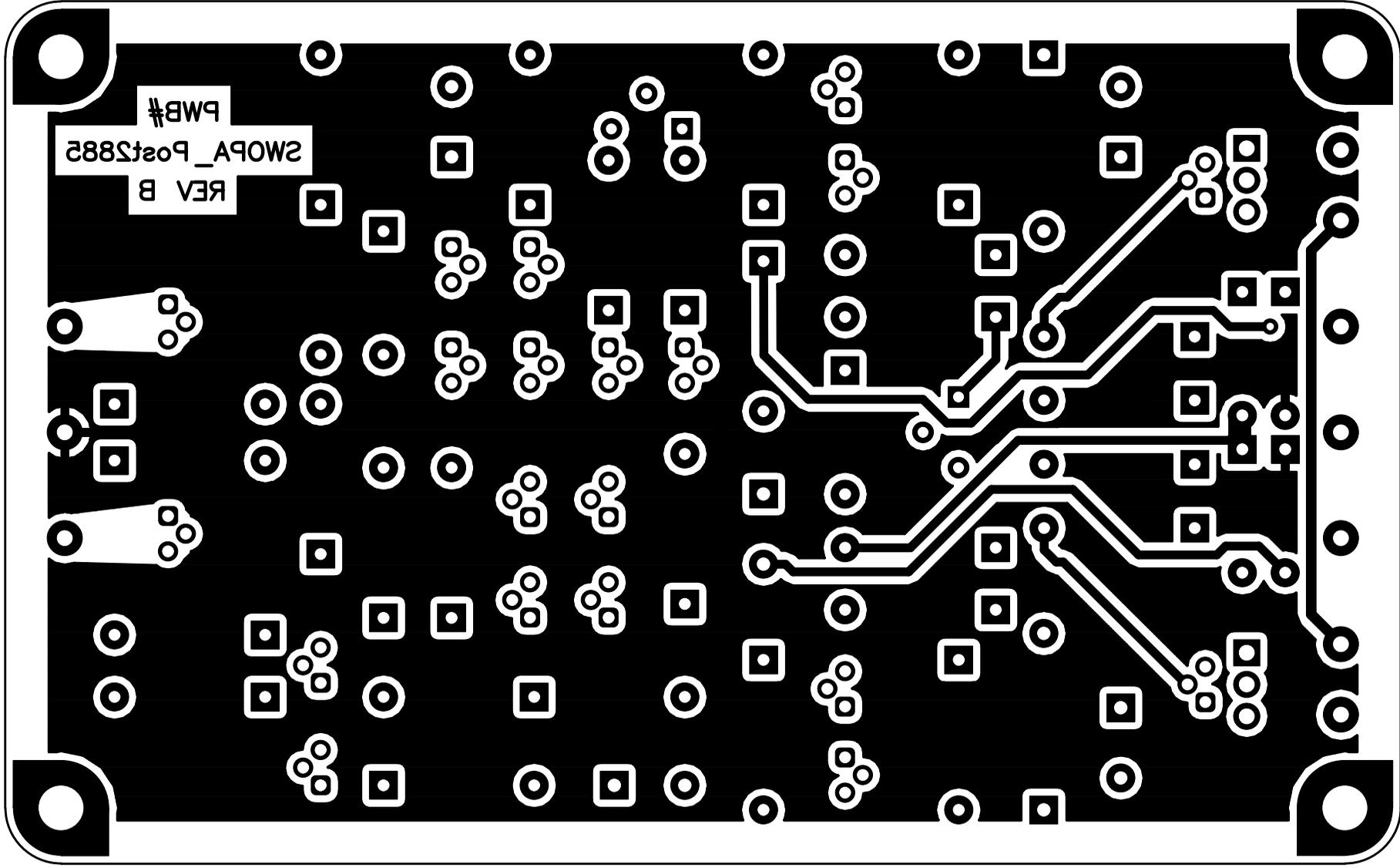


TOP CIRCUIT LAYER



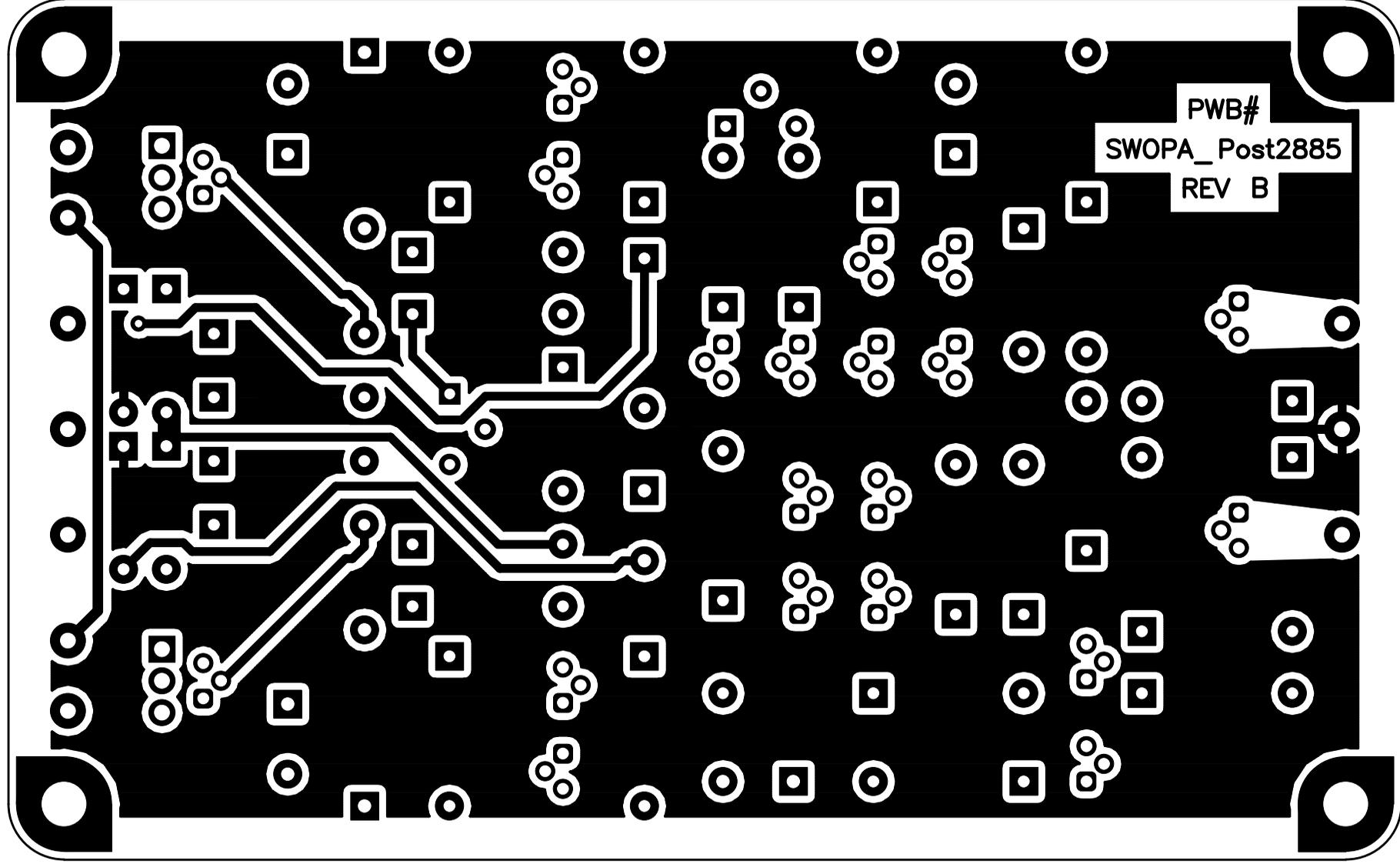
BOTTOM CIRCUIT LAYER

Title SWOPA DISC OPAMP THD(1) PWB		
Size 8.5x14	Number SWOPA2885PWB1	Rev B
Date Thu May 09, 2013	Drawn by D. Chisholm	
File SWOPA_Post2885PWB_B.pcb	Sheet	of



BOTTOM CIRCUIT LAYER

БОТЛОМ ЦИРКУИТ ПЛАТЕН

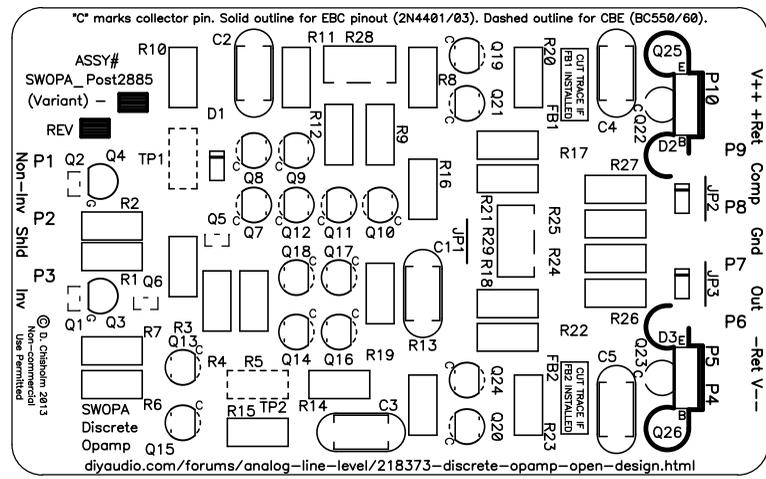


PWB#

SWOPA_Post2885

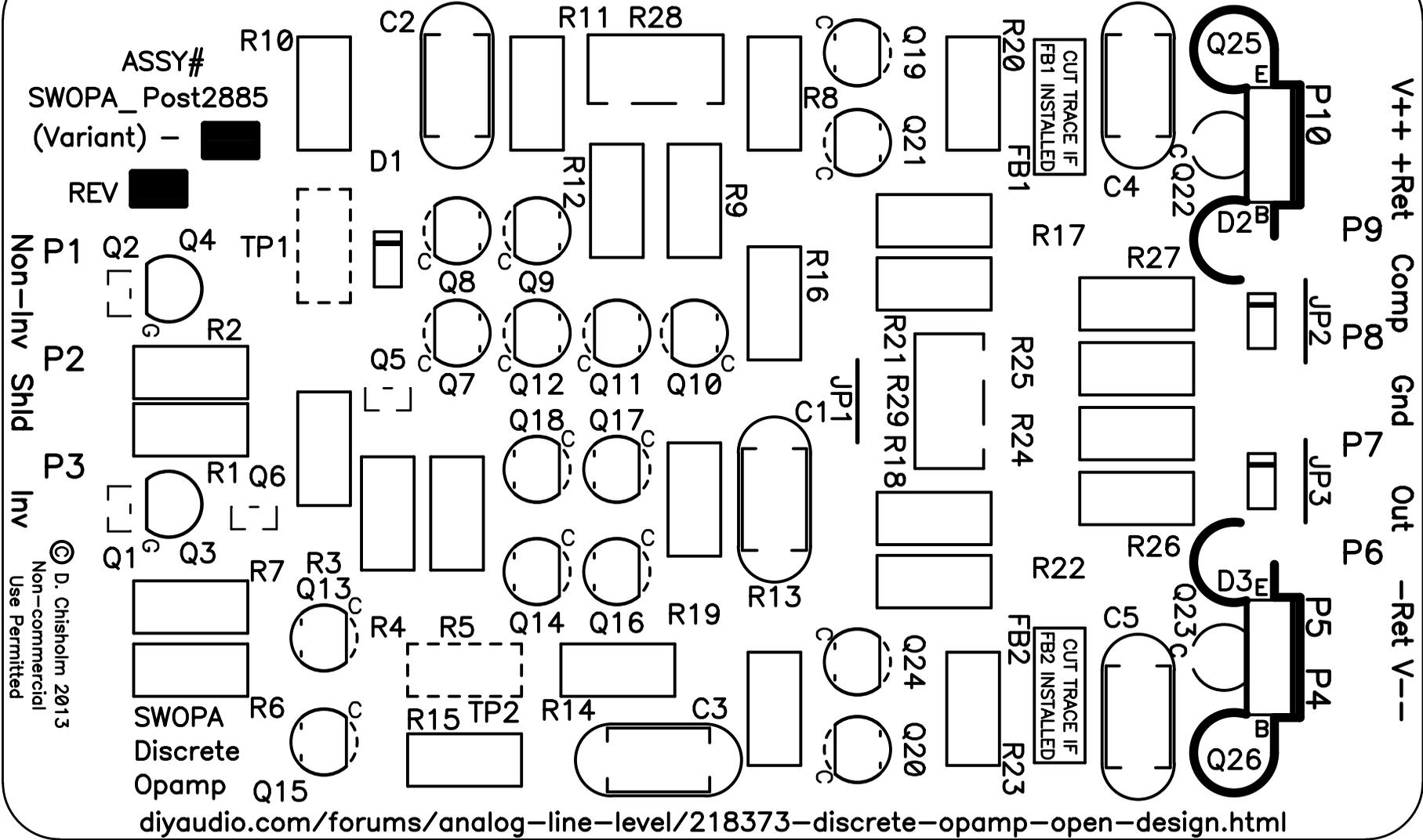
REV B

SILK SCREEN TOP



Title SWOPA DISC OPAMP THD(1) PWB		
Size 8.5x14	Number SWOPA2885PWB1	Rev B
Date Thu May 09, 2013	Drawn by D. Chisholm	
File SWOPA_Post2885PWB_B.pcb	Sheet	of

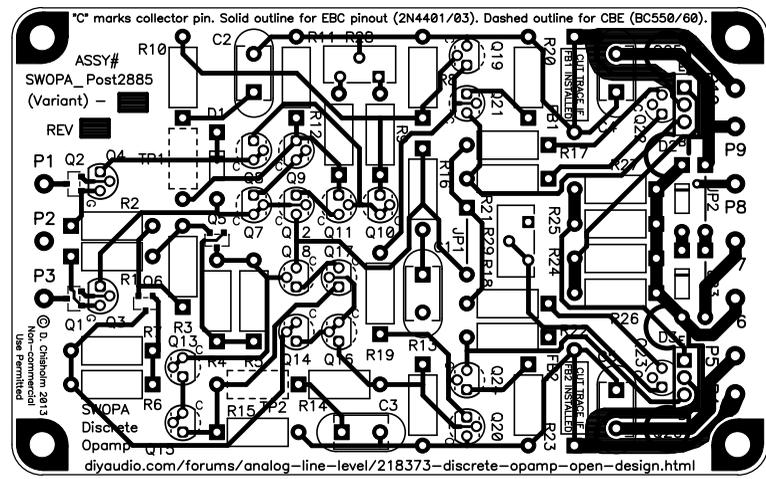
C marks collector pin. Solid outline for EBC pinout (2N4401/03). Dashed outline for CBE (BC550/60).



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Use Permitted

diyaudio.com/forums/analog-line-level/218373-discrete-opamp-open-design.html

SILK SCREEN TOP



TOP CIRCUIT LAYER

Title SWOPA DISC OPAMP THD(1) PWB		
Size 8.5x14	Number SWOPA2885PWB1	Rev B
Date Thu May 09, 2013	Drawn by D. Chisholm	
File SWOPA_Post2885PWB_B.pcb	Sheet	of

PWB Drawing Sheet Index

The printed wiring board (PWB) human-readable drawing (filename: SWOPA2885PWB_B_ALL.pdf) includes sheets described below. Print at 1:1 scale ("Actual Size", not "Fit to Page") on 8.5" x 14.0" paper (US "Legal" size) in "Landscape" orientation.

Sheet 1: SWOPA2885PWB1_BRD Overall dimensions and overview of the PWB as used in the intended assembly. Magnified component placement view. Fabrication notes used by the PWB etching house. Mounting hole detail.

Sheet 2: EBC_PLACEMENT Magnified view of component placement on completed PCB assembly. Transistor outlines for TO-92 packages are shown for devices with "EBC" pinout, such as the 2N4401/2N4403. Component values are also shown, but not guaranteed to be accurate - consult parts list for the particular varainat and revision level being constructed. This sheet is most likely used as a guide during assembly and inspection check-print.

Sheet 3: CBE_PLACEMENT Magnified view of component placement on completed PCB assembly. Transistor outlines for TO-92 packages are shown for devices with "CBE" pinout, such as the BC550/BC560. Component values are also shown, but not guaranteed to be accurate - consult parts list for the particular varainat and revision level being constructed. This sheet is most likely used as a guide during assembly and inspection check-print.

Sheet 4: DRILL_LOCATIONS View showing all holes. Hole locations are actually defined in the Excellon drill file, included in the "Gerbers" folder. This sheet is most likely used as a check-print for sample inspections to verify that boards were manufactured correctly.

Sheet 5: TOP_COPPER Pads and traces on the top (component) side of the PWB.

Sheet 6: TOP_COPPER_ONLY Same as sheet 5, but the drawing title block and border has been removed and the top circuit layer has been magnified to fit the page (magnification factor approx 2.4:1). Of particular interest to masochists wanting to replicate this layout in a different PWB program. May also be used for home etching of PCB's (using, e.g., toner transfer) if you spend enough time finagling the printer scale factor.

Sheet 7: BOTTOM_COPPER Pads and traces on the bottom side (traditionally called the "solder side") of the PWB. Note that this is a view "looking through" the PWB from the top side, which is a de-facto standard for the PCB fabrication industry.

Sheet 8: BTM_COPPER_ONLY Same as sheet 7, but the drawing title block and border has been removed and the bottom circuit layer has been magnified to fit the page.

Sheet 9: BTM_COPPER_MIRROR A "mirror image" of sheet 8. (Note that the etched copper drawing number reads correctly from left to right.) This is the image a home constructor might use for the bottom side of his board - if he's willing to not only finagle the scale factor, but also wrestle with top/bottom registration.

Sheet 10: TOP_SILK Component outlines, reference designators, and other information printed in ink on the top side of the board. (Traditionally called the "silkscreen" or "legend" layer.) A few of the reference designators are placed in ambiguous locations - refer to the component placement diagram on sheet 2 or sheet 3.

Sheet 11: TOP_SILK_ONLY Same as sheet 10, but the drawing title block and border has been removed and the silkscreen layer has been magnified to fit the

page .

Sheet 12: TOP_SILK_COPPER Combined view of top-side traces and silk-screen may be useful for critiquing the PWB layout.