

Fairchild QFET for Synchronous Rectification DC to DC Converters

by K.S. Oh

1. Introduction

Fairchild is currently developing and marketing a new QFET series that has improved $R_{DS(on)}$, gate charge, and switching speed characteristics. The superior features of these QFETs are very useful for increasing the efficiency of low output voltage power supplies, making it specially appropriate for computer microprocessor power supply applications which require high efficiency.

This application note describes the use of a Fairchild QFET (FQP60N03L) in the power supply (DC-DC converter) of computer microprocessors. Chapter 2 describes QFET's organizational features and the improvements in its electrical characteristics based on these features. Chapter 3 outlines the required input voltage and current based on the latest trends in microprocessors, and describes the optimum DC-DC converter circuit configuration that will meet these input conditions. The synchronous rectification DC-DC converter introduced in Section 3-1, which increases the overall efficiency by converting the loss due to the forward voltage drop of the rectifier diode to the MOSFET's low $R_{DS(on)}$ loss, is explained in detail in the main body of this note. Lastly, Chapter 4 describes an example of a synchronous rectification DC-DC converter design that uses the Fairchild PWM control IC RC5058, and the loss and efficiency associated when FQP60N03L is used.

2. QFET

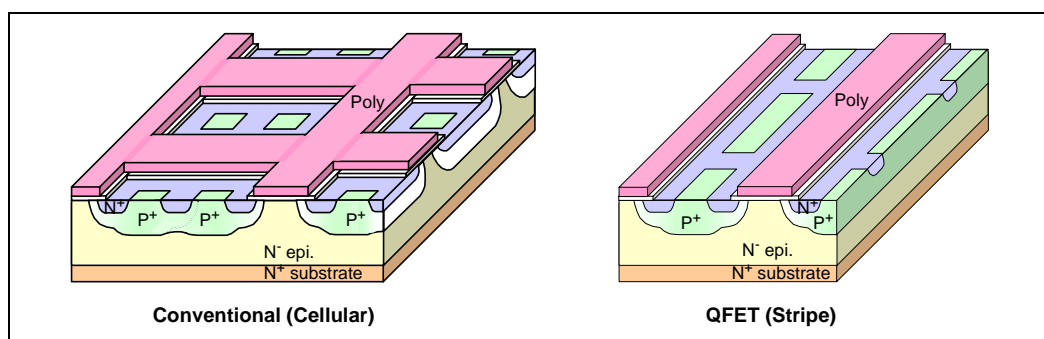


Figure 2-1. Comparison of a QFET and a Conventional MOSFET Structure

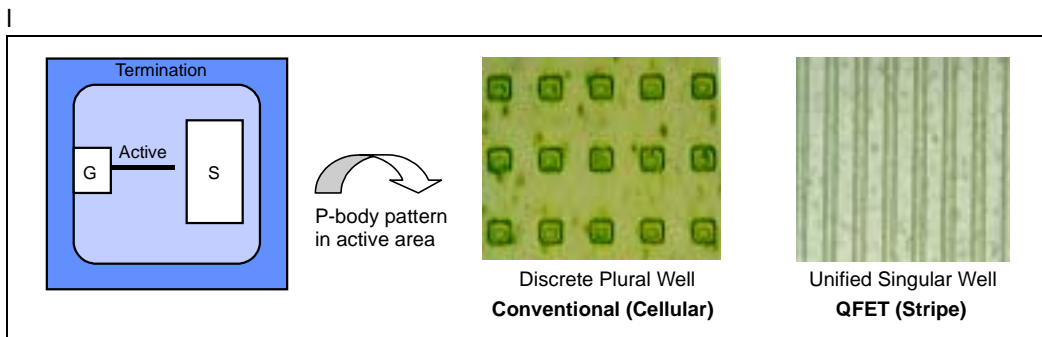


Figure 2-2. Comparison of a QFET and a Conventional MOSFET Active Cell

The most noticeable difference between a QFET and a conventional MOSFET is in the P-well design (Figure 2-1). The conventional MOSFET is composed of a discrete P-well, cellular in shape, working alone as an active cell. Whereas, a QFET consists of a unified P-well, striped in shape, which is connected together at the edge of the active area, working in unison (See Figure 2-2). Unlike the spherical P-well junction in cellular devices such as the conventional MOSFET, the QFET has a cylindrical P-well junction allowing a higher breakdown voltage for a given epitaxial layer. This improvement of breakdown voltage efficiency provides lower on resistance by reducing resistivity and thickness of the epitaxial layer for a given breakdown voltage. Furthermore, the gate charge and the switching characteristics are improved in a QFET due to the reduction in the input capacitance by the increase in gate oxide thickness and optimization of the gate overlap area. $R_{DS(on)}$, gate charge, and switching characteristics are all important for determining the MOSFET loss in the set (Refer to Section 4-2). Hence, a QFET is appropriate for computer microprocessor power supply applications which require high efficiency.

The Fairchild FQP60N03L, a new 30V logic level MOSFET product, is appropriate for low voltage DC-DC converters. Figure 2-3 is a graph of $R_{DS(on)}$ as a function of the FQP60N03L's Junction temperature (T_J) at $V_{GS}=5[V] / 10[V]$ and $I_D=30[A]$. The change in $R_{DS(on)}$ which corresponds with the change in temperature is approximately $0.07[m\Omega/^{\circ}C]$ when $V_{GS}=5[V]$ and $0.05[m\Omega/^{\circ}C]$ when $V_{GS}=10[V]$.

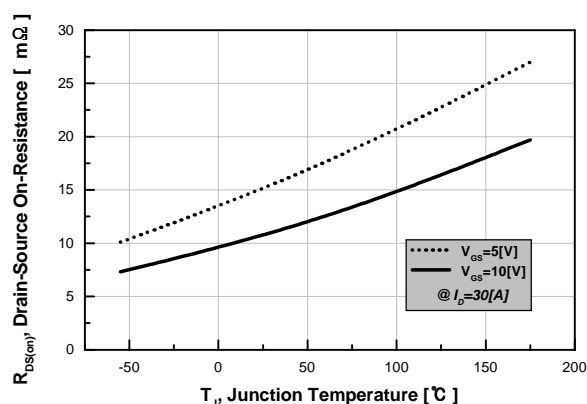


Figure 2-3. Change in $R_{DS(on)}$ as a function of temperature

3. Synchronous Rectification DC to DC Converter

Recent increases in computer microprocessor processing speed have demanded lower operating voltages. A broad range of input voltages and currents are required by Intel microprocessors with processing speeds that range from 233-1000MHz. Tables 3-1 and 2 list voltage and current specifications recommended by Intel Corp for the Celeron™ and Pentium® III processors. (Refer to Intel VRM 8.4 DC-DC Converter Design Guidelines)

Table 3-1. Pentium® III processor ($\geq 2.0V$) Voltage and Current Specifications

Symbol	Parameter	Processor core frequency [MHz]	Min.	Typ.	Max.	Unit
V _{CC} CORE	V _{CC} for processor core	<600 600 / 600B		2.00 2.05		V
	V _{CC} CORE static tolerance at processor connector pins on system board		-0.070		0.070	V
	V _{CC} CORE transient tolerance at processor connector pins on system board		-0.140		0.140	V
I _{CC} CORE	Current for V _{CC} CORE	600 / 600B 550 533B 500 450			17.8 17.0 16.7 16.1 14.5	A
I _{CC} SGNTCORE	I _{CC} for Stop-Gain V _{CC} CORE				1.68	A
I _{CC} DSLPCORE	I _{CC} for Deep-Sleep V _{CC} CORE				0.50	A
dI _{CC} CORE/dt	I _{CC} slew rate				20	A/μs

Table 3-2. Pentium® III processor ($\leq 1.7V$) Voltage and Current Specifications

Symbol	Parameter	Processor core frequency [MHz]	Min.	Typ.	Max.	Unit
V _{CC} CORE	V _{CC} for processor core	All SECC2		1.65		V
		All PC-GPA		1.60		
	V _{CC} CORE static tolerance at processor connector pins on system board	All SECC2	-0.080		0.040	V
		All FC-PGA	-0.080		0.040	
	V _{CC} CORE transient tolerance at processor connector pins on system board	All SECC2	-0.080		0.050	V
		All FC-PGA	-0.130		0.080	
I _{CC} CORE	Current for V _{CC} CORE	700-733 600-667 500-550			14.6 13.3 11.0	A
I _{CC} SGNTCORE	I _{CC} for Stop-Gain V _{CC} CORE				2.5	A
I _{CC} DSLPCORE	I _{CC} for Deep-Sleep V _{CC} CORE				2.2	A
dI _{CC} CORE/dt	I _{CC} slew rate				20	A/μs

The DC-DC converter responsible for supplying only the microprocessor input voltage and current recommended in Tables 3-1 and 2, used in the computer motherboard, is required to output high quality DC voltage almost free of ripples. Because of system characteristics, a step-down DC-DC converter that employs feedback control through the PWM controller is generally used. Figure 3-1 shows the basic circuit of a step-down (Buck topology) DC-DC con-

verter used to supply power to the microprocessor. Section 3-2 briefly explains the operation of a Buck converter.

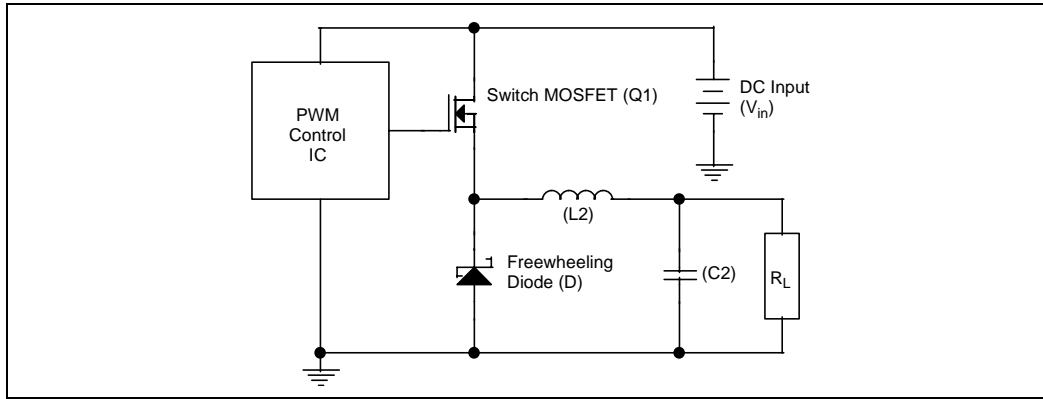


Figure 3-1. Step-down (Buck) DC-DC Converter

3-1. Efficiency of Buck Converter

In order to increase the overall efficiency, it is important to reduce the loss generated in each component, as much as possible, in low output voltage power supplies. Equation (3-11) in Section 3-2 shows the reduction in system efficiency due to the loss associated with semiconductor components such as the switch MOSFET (Q1) and freewheeling diode (D). If the freewheeling diode (D) is substituted with the MOSFET (Q2), the semiconductor component loss can be reduced because the loss from the diode's forward voltage drop is greater than the loss from the MOSFET's $R_{DS(on)}$. This effect is represented by the following equation. First, assume the following conditions: output current $I_{out}=18[A]$, duty ratio $D=0.49$, freewheeling (Schottky) diode's forward voltage drop $V_D=0.52[V]$ (the typical value when $i_F=18[A]$, $T_J=100[^\circ C]$ in MBRD835L data sheet Figure 2), and MOSFET $R_{DS(on)}=14.70[m\Omega]$ (the typical value when $V_{GS}=10[V]$, $T_J=100[^\circ C]$ in Figure 2-3). Then, the freewheeling diode (D) loss can be calculated by the following equation (3-1):

$$\begin{aligned} P &= V_D I_{out} (1 - D) \\ &= 0.52[V] \times 18[A] \times (1 - 0.49) \dots \dots \dots (3 - 1) \\ &= 4.77[W] \end{aligned}$$

If substituted with the MOSFET (Q2), the MOSFET (Q2) loss is calculated by equation (3-2) as follows.

$$\begin{aligned} P &= [I_{out} \sqrt{(1 - D)}]^2 R_{DS(on)} \\ &= [18[A] \times \sqrt{(1 - 0.49)}]^2 \times 14.70[m\Omega] \dots (3 - 2) \\ &= 2.43[W] \end{aligned}$$

The calculation results of equations (3-1) and (3-2) verify the increase in efficiency if the freewheeling diode (D) is substituted with a MOSFET(Q2). This method is called synchronous rectification, and the MOSFET, a synchronous rectifier (Q2). Figure 3-2 is a remodeling of the circuit shown in Figure 3-1 employing synchronous rectification. If the Schottky diode (D2) is used in parallel with the synchronous rectifier (Q2) in this circuit, the inductor (L2) current that previously flowed through the parasitic diode of the synchronous rectifier (Q2) starts flowing through the faster and low loss Schottky diode (D2) during the switching dead time of the two MOSFET's (Q1, Q2). This flow pattern makes the circuit more efficient.

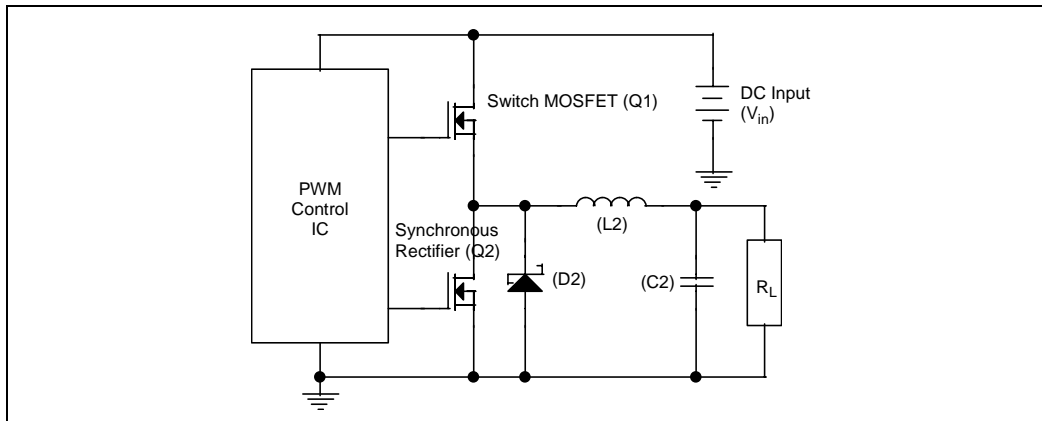


Figure 3-2. Synchronous Rectification Step-down DC-DC Converter

3-2. Buck Converter

The Buck converter is the most basic and simplest DC-DC converter topology suitable for obtaining low capacity, low voltage output. The Buck converter uses the step-down technique, in which the output voltage is always less than or equal to the input voltage. The output to input voltage ratio is controlled with the duty ratio.

Figure 3-3 shows the basic circuit of the Buck converter, and Figure 3-4 shows the operating waveforms for each portion.

When $Q1$ turns on at time $t1$, the reverse-biased D turns off, and current flows through $L2$, inducing $v_L(t) = L \times di_L(t)/dt$ voltage at both $L2$ terminals according to Faraday's law. Then the power is delivered to the output load. When $Q1$ turns off at time $t2$, the current energy that was stored in $L2$, during $Q1$'s on period, discharges through the forward-biased D , and power is delivered to the output load.

D in this circuit is used to make the pass required to reduce the energy that was stored in $L2$ during $Q1$'s on period to the original value. $L2$ and $C2$ are used to eliminate the ripple of the output voltage by forming a low pass filter.

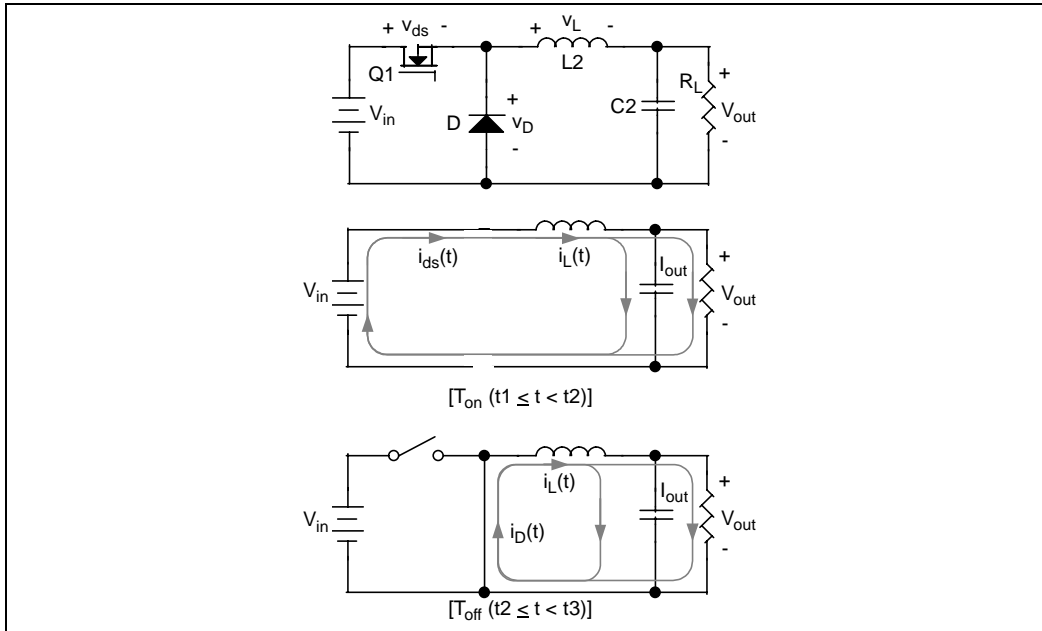


Figure 3-3 Buck Converter's Basic Circuit

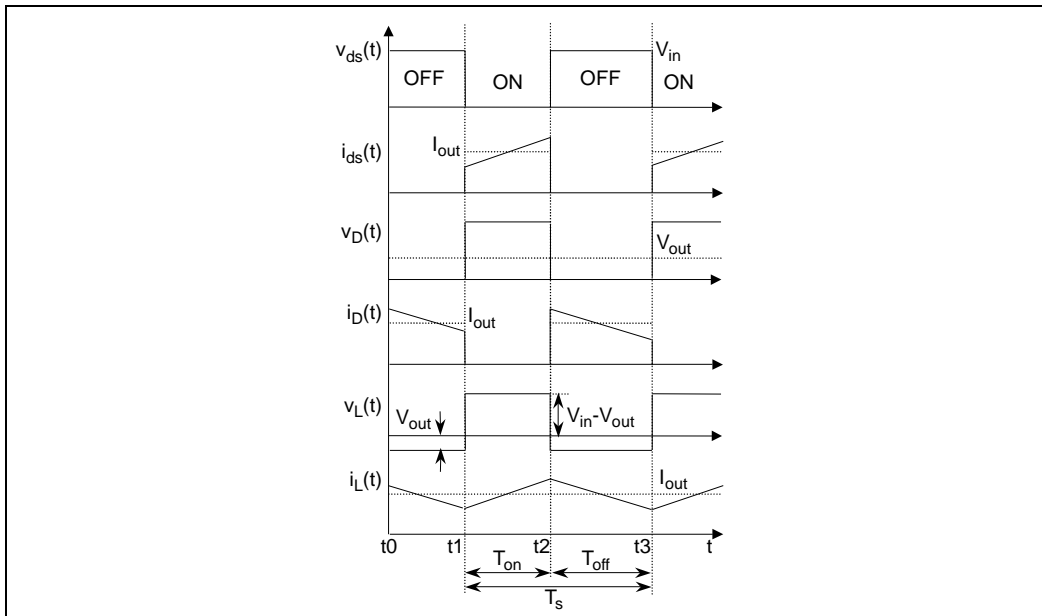


Figure 3-4. Waveforms of each portion of the Buck Converter

A DC-DC converter is primarily used to obtain a specific DC voltage from any DC voltage. The output to input voltage ratio of the Buck converter is described as follows. First, assume an ideal circuit, where the losses associated with each portion of the circuit have been ignored. Because L2 current $i_L(t1)$ and $i_L(t3)$ must be equal, as shown in Figure 3-4, equation 3-3 is derived as follows:

$$\frac{1}{L} \int_{t1}^{t3} v_L(t) dt = \int_{t1}^{t3} di_L(t) = i(t3) - i(t1) = 0 \dots \dots \dots (3-3)$$

Equation (3-4) can be obtained from Equation (3-3):

$$\int_{t1}^{t3} v_L(t) dt = 0 \dots \dots \dots (3-4)$$

When this is divided into Q1's on and off periods, the following can be derived:

$$\int_{t1}^{t2} v_L(t) dt = - \int_{t2}^{t3} v_L(t) dt \dots \dots \dots (3-5)$$

The left hand side of Equation (3-5) represents the integral of L2 voltage with respect to time during Q1's on period and the right hand side represents the integral of L2 voltage with respect to time during Q1's off period. When this equation is applied to the Buck converter, the following equation is derived.

$$(V_{in} - V_{out})DT_s = V_{out}(1 - D)T_s \dots \dots \dots (3-6)$$

Where T_s = period

The $V_{in} - V_{out}$ of the left hand side of the equation represents the L2 voltage in the (DT_s) period when Q1 is on, and V_{out} of the right hand side represents the L2 voltage in the $((1 - D)T_s)$ period when Q2 is off. Equation 3-6 can be reduced to the following to calculate the output to input voltage ratio.

$$V_{out} = DV_{in} \dots \dots \dots (3-7)$$

Equation (3-7) shows the output to input voltage ratio for an ideal case. However, the forward voltage drop component of the switch MOSFET Q1 and the freewheeling diode D exists in an actual system operating environment.

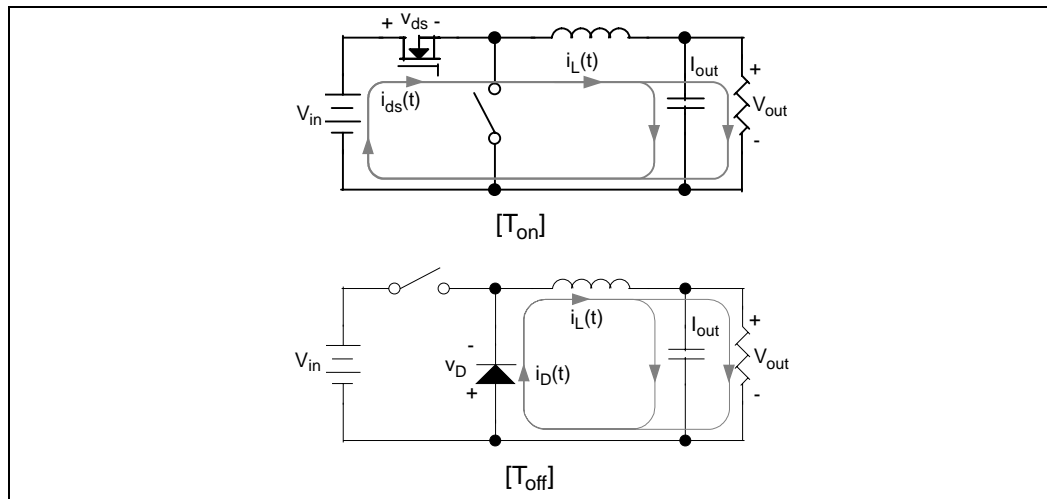


Figure 3-5. Equivalent circuit of an ON and OFF Step-down (Buck) Converter, which accounts for the forward voltage drop of the switch MOSFET(Q1) and the freewheeling diode (D)

Equation (3-8) can be obtained as in Equation (3-6) by referring to Figure 3-5:

$$(V_{in} - v_{ds}(t) - V_{out})DT_s = (V_{out} + v_D(t))(1 - D)T_s \dots \dots \dots (3 - 8)$$

Equation (3-9) represents this equation with respect to V_{out} :

$$V_{out} = DV_{in} - [Dv_{ds}(t) + v_D(t)(1 - D)] \dots (3 - 9)$$

Rearranging the above equation (3-9) in terms of D,

$$D = \frac{V_{out} + v_D(t)(1 - D)}{V_{in} - v_{ds}(t)} \dots \dots \dots (3 - 10)$$

The efficiency (η) can be obtained from equation (3-11) using the input to output current ratio, $I_{in}/I_{out}=D$, and equation (3-10):

$$\eta = \frac{V_{out}I_{out}}{V_{in}I_{in}} = \frac{V_{out}}{V_{in}} \frac{V_{in} - v_{ds}(t)}{V_{out} + v_D(t)(1 - D)} < 1 \dots \dots \dots (3 - 11)$$

As shown by equations (3-9) and (3-11), the forward voltage drop of the switch MOSFET and the freewheeling diode reduces the output voltage and the entire system efficiency. Besides these factors, the inductor coil resistance and the capacitor ESR also drop the efficiency. Hence, a low coil resistance inductor and low ESR capacitors must be used. In the case of the capacitor, it is advantageous to use several capacitors in parallel.

A high quality output DC voltage with low ripple, if possible, is considered the best. The following is a description of the Buck converter output voltage ripple.

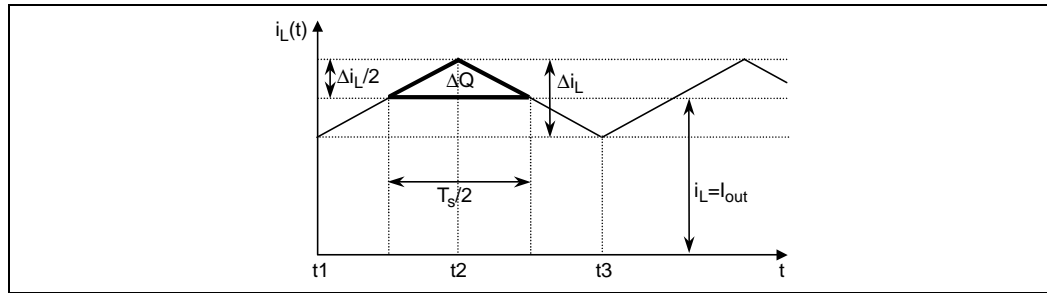


Figure 3-6. Inductor Current

Ripples appear in the output voltage as the L2 current ripple component, Δi_L charges and discharges C2 as illustrated in Figure 3-6. C2 is charged during the period when $i_L(t)$ is greater than I_{out} . The charge (ΔQ) that flows into C2 at this time divided by the value of C2 (C) is the output voltage ripple component. First, the following equation calculates the Δi_L in Figure 3-6:

$$\Delta i_L = DT_s \frac{V_{in} - V_{out}}{L} = \frac{D(1 - D)V_{in} T_s}{L} \dots \dots \dots (3 - 12)$$

ΔQ , the portion indicated by the thick line in Figure 3-6, can be calculated as a triangular area of $\Delta i_L/2$ in height and $T_s/2$ in width.

$$\Delta Q = \left(\frac{1}{2}\right)\left(\frac{\Delta i_L}{2}\right)\left(\frac{T_s}{2}\right) \dots \dots \dots (3-13)$$

The following equation is derived when equation (3-12) is substituted into equation (3-13), where the peak-to-peak output voltage ripple component is Δv_{out} :

$$\Delta v_{out} = \frac{\Delta Q}{C} = \frac{D(1-D)V_{in}T_s^2}{8LC} = \frac{\pi^2(1-D)V_{out}\left(\frac{f_c}{f_s}\right)^2}{2} \dots \dots \dots (3-14)$$

where:

$f_c = \frac{1}{2\pi\sqrt{LC}}$: output LPF resonant frequency

f_s : switching frequency

As shown by equation (3-14), the output voltage ripple can be reduced, if f_s is increased or if it is designed so that f_c becomes $f_c < f_s$.

4. Synchronous Rectification DC-DC Converter Design

4-1. Design Example

The design in Figure 4-1 outputs the processor core voltage $V_{CC_{CORE}}$ (1.3[V] ~ 3.5[V]), V_{tt} termination (1.5[V]), V_{clock} (2.5[V]), and V_{agg} (Selectable 1.5[V] / 3.3[V]) using the Fairchild PWM control IC RC5058. Of these outputs, only $V_{CC_{CORE}}$ is output by the synchronous rectification DC-DC converter and the remaining outputs are output through the linear regulator. This section describes the calculations for the input (L1) / output (L2) inductor and input (C1) / output (C2) capacitor for the synchronous rectification DC-DC converter design shown in Figure 4-1.

The following initial design conditions are set.

- $D = 0.49 \left(= \frac{V_{out} + V_D}{V_{in} + V_D - V_{DS(on)}} \right)$
- $f_s = 310[\text{kHz}]$
- $V_{DS(on)} = 0.37[\text{V}]$ (Q1's on-state drain-to-source voltage = $I_{out} \times R_{DS(on)}$)
- $\Delta i_L \leq 2[\text{A}]$: set it to twice the value of the minimum output current to operate in the continuous mode.
- $V_{out} = 2.0[\text{V}]$: refer to table 3-1.
- Output voltage ripple $\Delta v_{out} \leq 0.04[\text{V}]$: set within $\pm 1[\%]$ of $V_{out} = 2.0[\text{V}]$
- Input voltage ripple $\Delta v_{in} \leq 0.5[\text{V}]$: set within $\pm 5[\%]$ of $V_{in} = 5[\text{V}]$
- Input current $I_{in} = 8.47[\text{A}]$: set to 85% efficiency at max load condition ($V_{in} = 5[\text{V}]$, $V_{out} = 2.0[\text{V}]$, $I_{out} = 18[\text{A}]$).

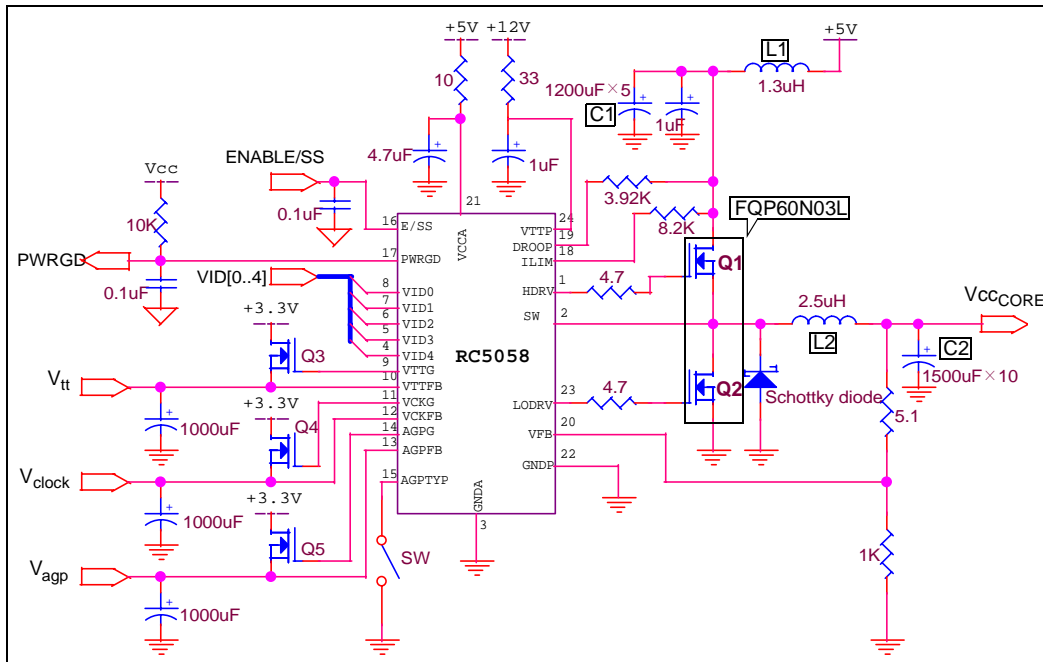


Figure 4-1. Synchronous Rectification DC-DC Converter using the PWM Control IC RC5058

1) L1/L2 design

(1) Output Inductor, L2

The output inductor must be designed so that it operates in a continuous mode having no discontinuous interval in the output inductor current to stabilize frequency and optimize load regulation.

When Q1 is on, the voltage at both terminals of L2 is $V_L = V_{in} - V_{DS(on)} - V_{out}$. L2 can be calculated with the following equation (4-1).

$$\begin{aligned}
 L2 &\geq \frac{V_{in} - V_{DS(on)} - V_{out}}{\Delta i_L} T_{on} \\
 &\geq \frac{(5[V] - 0.37[V] - 2[V])}{2[A]} \times 1.58[\mu\text{sec}] \geq 2.08[\mu\text{H}] \\
 L2 &= 2.50[\mu\text{H}] \dots \dots \dots (4-1)
 \end{aligned}$$

(2) Input Inductor, L1

Used after the 5V terminal to eliminate the switching noise caused by the input ripple current, a L1 of 1.3uH is generally sufficient. Care must be taken not to make L1 too large because an excessively large input inductor can restrict the current change rate at the converter input, which in turn, can weaken the converter transient response characteristics.

2) C1/C2 design

(1) Output Capacitor, C2

C2 can be calculated from equation (4-2), which is derived from equations (3-13) (output voltage ripple calculation equation) and (3-14).

$$\begin{aligned}
 C2 &\geq \frac{\Delta i_L}{8f_s \Delta v_{out}} \\
 &\geq \frac{2[A]}{8 \times 310[kHz] \times 0.04[V]} \geq 20.16[\mu F] \\
 C2 &= 1500[\mu F] \times 10 \dots \dots \dots (4-2)
 \end{aligned}$$

A capacitor with low ESR should be used, if possible, to minimize the ESR loss. The maximum ESR of C2 can be calculated from equation (4-3) below.

$$\begin{aligned}
 ESR &\leq \frac{\Delta V_{out}}{\Delta i_L} \\
 &\leq \frac{0.04[V]}{2[A]} = 0.02[\Omega] \dots \dots \dots (4-3)
 \end{aligned}$$

C2 is set with a value much greater than the minimum value, and connected in parallel to reduce the output voltage ripple and ESR.

(2) Input Capacitor, C1

In order to reduce ESR, C1, which is used as the input low pass filter, should be designed in parallel, if possible. The following equation (4-4) shows the calculation for C1.

$$\begin{aligned}
 C1 &\geq \frac{I_{in} T_{on}}{\Delta v_{in}} \\
 &\geq \frac{8.47[A] \times 1.58[\mu sec]}{0.5[V]} \geq 26.77[\mu F] \\
 C1 &= 1200[\mu F] \times 5 \dots \dots \dots (4-4)
 \end{aligned}$$

4-2. Power Loss Analysis

The losses generated mainly in the synchronous rectification DC-DC converter in Figure 4-1 are as follows:

- MOSFET conduction losses: $I^2 R_{DS(on)}$
- Inductor equivalent resistance DC losses
- PCB copper losses
- MOSFET gate-charge losses
- Diode-conduction losses
- Transition losses of power MOSFET
- Capacitor ESR losses
- Losses due to the PWM control IC

Among the losses, conduction losses ($I^2 R_{DS(on)}$), gate-charge losses, and transition losses are specifically associated with the MOSFET and can be represented by the following equation.

Conduction losses (P_c)

This loss is defined as the loss generated between the drain and source during the MOSFET on period and can be easily calculated with equation $P=I^2R$, where the current, I , is the RMS value of I_{out} , ($I_{out}\sqrt{D}$), and the resistance, R , is $R_{DS(on)}$. The conduction loss can be calculated with equation (4-5) as follows.

$$P_c = (I_{out}\sqrt{D})^2 R_{DS(on)} [W] \dots \dots \dots (4-5)$$

where $R_{DS(on)}$ is determined by the gate-source drive voltage and junction temperature

Gate-charge losses (P_{g-c})

The gate-charge loss is defined as the loss generated during charging and discharging of C_{iss} for driving the MOSFET. The gate-charge loss can be calculated from equation (4-6).

$$P_{g-c} = V_{GS} Q_g f_s [W] \dots \dots \dots (4-6)$$

where V_{GS} : Gate drive voltage
 Q_g : Total gate charge at V_{GS}

Transition losses (P_t)

This loss is defined as the loss generated between the drain and source during the transition period when an on MOSFET turns off or an off MOSFET turns on. The equation to calculate this loss can be derived from the method of calculating the triangular area where $v_{ds}(t)$ and $i_{ds}(t)$ overlap at on and off transition, as shown in Figure 4-2.

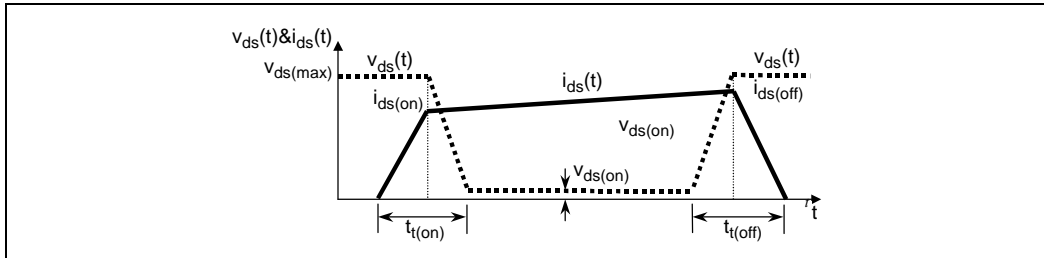


Figure 4-2. Transition Waveform of MOSFET for inductive loads

$$\begin{aligned} P_t &= P_{t(on)} + P_{t(off)} \\ &= \frac{[v_{ds(max)}(i_{ds(on)}t_{t(on)} + i_{ds(off)}t_{t(off)})f_s]}{2} [W] \dots \dots \dots (4-7) \end{aligned}$$

where $P_{t(on)}$: Turn-on transition loss
 $P_{t(off)}$: Turn-off transition loss
 $i_{ds(on)}$: Maximum value of the drain-to-source current at turn-on
 $i_{ds(off)}$: Maximum value of the drain-to- source current at turn-off
 $t_{t(on)}$: Turn-on transition time
 $t_{t(off)}$: Turn-off transition time

Equations (4-5), (4-6) and (4-7) show that the MOSFET used in the DC-DC converter needs low $R_{DS(on)}$, low Q_g , and fast switching speed characteristics in order to increase the system efficiency.

Now let's calculate the losses using the measured data, after having applied FQP60N03L to Q1 and Q2, as shown in Figure 4-1, and where the test conditions are input voltage = 5V, output voltage = 2V, and load current = 7A.

(1) Q1

$$\begin{aligned}
 P_c &= 4.97^2[A] \times 19.03[m\Omega] \cong 470.06[mW] \\
 P_{g-c} &= 6.30[V] \times 18.04[nC] \times 311[kHz] \cong 35.35[mW] \\
 P_{t(on)} &= 0.7[V] \times 2.8[A] \times 130[ns] \times 311[kHz] \cong 79.24[mW] \\
 P_{t(off)} &= \frac{5.50[V] \times 8.04[A] \times 241[ns] \times 311[kHz]}{2} \cong 1657.17[mW] \\
 P_t &= P_{t(on)} + P_{t(off)} \\
 &\cong 79.24[mW] + 1657.17[mW] = 1736.41[mW] \\
 P_{Q1} &= P_c + P_{g-c} + P_t \\
 &\cong 470.06[mW] + 35.35[mW] + 1736.41[mW] \\
 &= 2241.82[mW]
 \end{aligned}$$

(2) Q2

$$\begin{aligned}
 P_c &= 2.89^2[A] \times 11.55[m\Omega] \cong 96.47[mW] \\
 P_{g-c} &= 10.32[V] \times 27.22[nC] \times 311[kHz] \cong 87.36[mW] \\
 P_{Q2} &= P_c + P_{g-c} \\
 &\cong 96.47[mW] + 87.36[mW] \\
 &= 183.83[mW] \\
 *P_{total} &= P_{Q1} + P_{Q2} \\
 &\cong 2241.82[mW] + 183.83[mW] = 2425.65[mW]
 \end{aligned}$$

The $R_{DS(on)}$ value used in the above calculation was taken from the Figure 2-3 graph, and it corresponds to the $R_{DS(on)}$ value when the MOSFET temperature has reached saturation after 1 hour of set operation. Q2 transition loss is almost zero because there is almost no current flowing between Q2's drain and source during the transition period, but rather most of the current flows through D2, which forms a current pass during dead time. The waveforms in Figure 4-3 are of currents flowing between the drain and source of Q1 and Q2 MOSFETs.

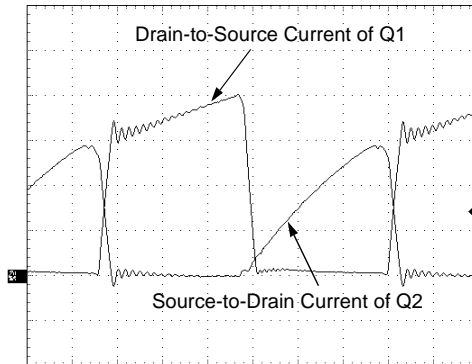


Figure 4-3. Current waveforms between the drain and source of switch MOSFET (Q1) and Rectifier MOSFET (Q2)
 \Rightarrow Vertical Division: 2[A]/div, Horizontal Division: 500[ns]/div

The graph in Figure 4-4 depicts the actual set efficiency measured under the following two conditions.

- Output voltage change
 Can program voltages from 1.30[V] ~ 3.5[V] according to the 5-bit DAC input of the RC5058 IC. The two voltages tested are 1.550V and 2.000V.
- Load current change
 Varies the output current from 1A to 18A when the output voltage is 2.000V, and varies the output current from 1A to 13A when the output voltage is 1.550V.

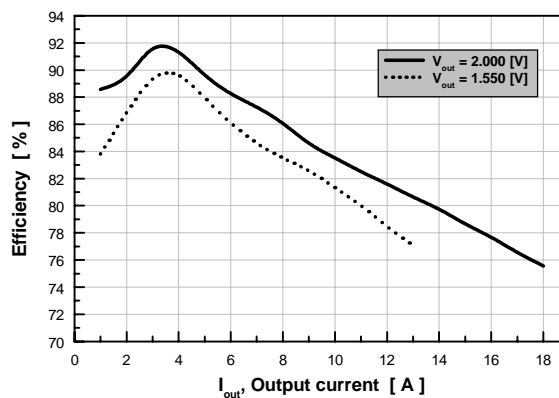


Figure 4-4. When the output voltages (V_{out}) are 1.550[V], and 2.000[V], efficiency of each output current (I_{out})

The reason that the efficiency of the 1.550V output voltage is less than that of the 2.000V output voltage, as shown in Figure 4-4, is largely due to inductor loss.

The efficiencies above can change depending on the diode forward voltage drop, inductor equivalent resistance, capacitor ESR and the PCB layout. Two suggestions are made by POWER PLANES of the Fairchild Application Bulletin AB-11 (PC Board Layout Checklist: DC-DC Converters) for the layout to minimize the loss, that is, 1) High currents are located on planes, not traces 2) and an internal power plane connects the source of the highside MOSFET, the inductor, and the flyback Schottky diode (or the drain of the lowside MOSFET) together.

5. Conclusions

The computer microprocessor power supply (DC-DC converter) is operated at 200[kHz]~400[kHz] high frequency to supply high-quality DC low voltage required by the computer microprocessor. However, operating at high frequencies can increase the loss, emphasizing the need to increase the efficiency. As shown by the MOSFET loss calculation (gate-charge loss, transition loss or switching loss), high efficiency can be obtained if a small gate-charge and a fast switching speed MOSFET are used, the higher the frequency of operation. Furthermore, a product with a low $R_{DS(on)}$ is required to reduce the MOSFET conduction loss, the more serious obstacle when supplied with a high load current.

The FQP60N03L developed by Fairchild is a QFET 30V product with improved $R_{DS(on)}$, gate charge, and switching speed characteristics which offers a higher level of set efficiency as described in Section 4-2.

References

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