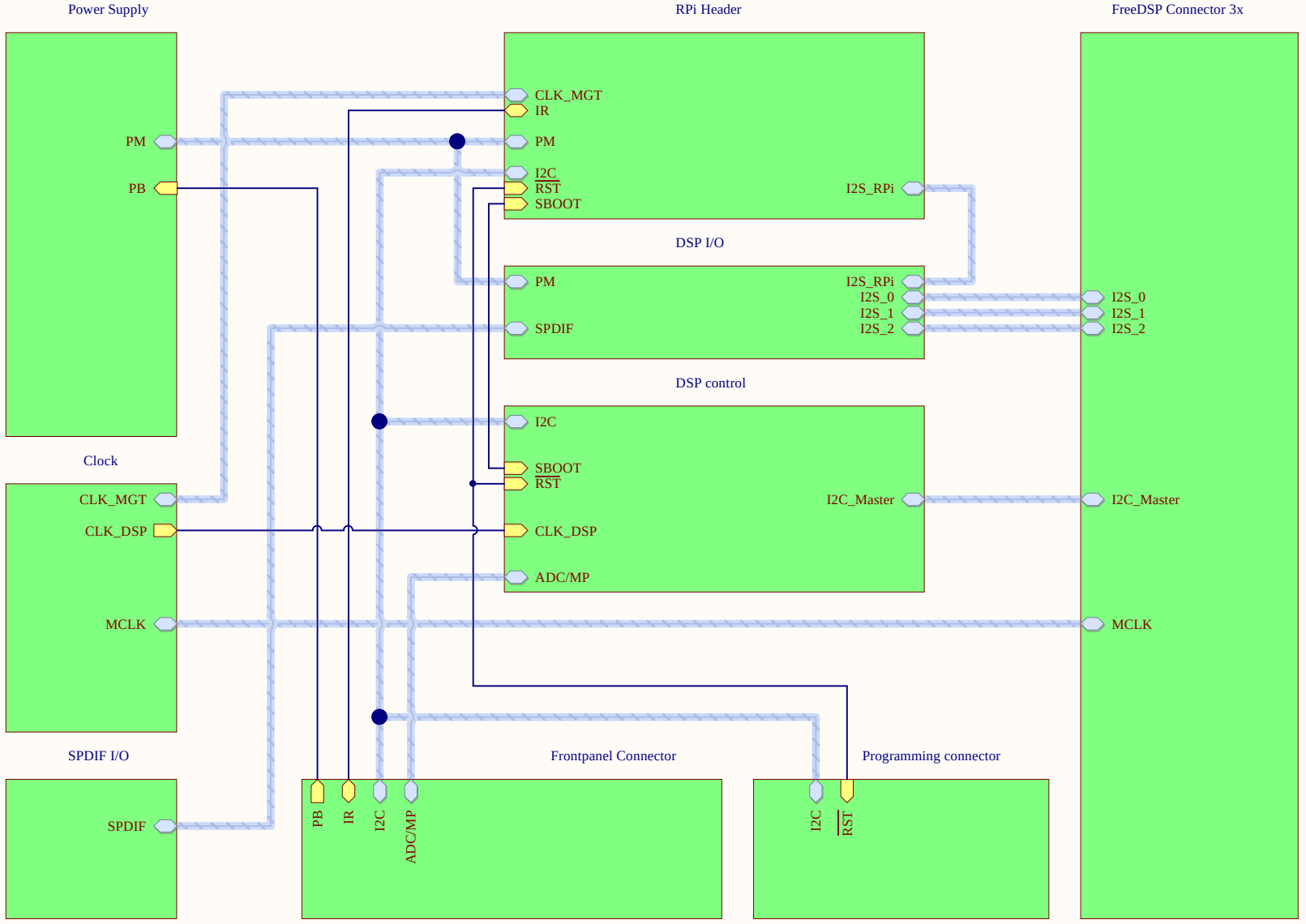
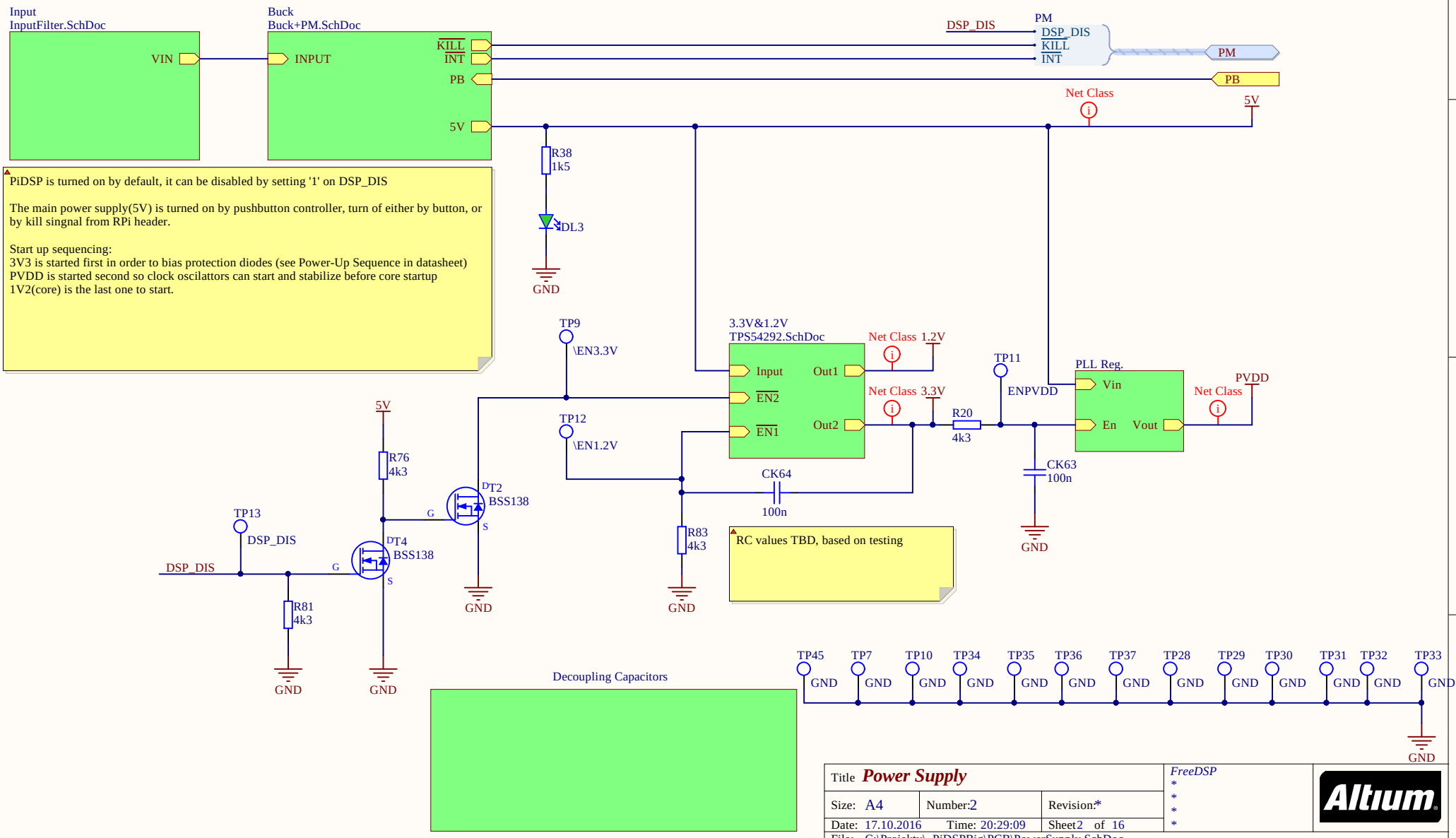
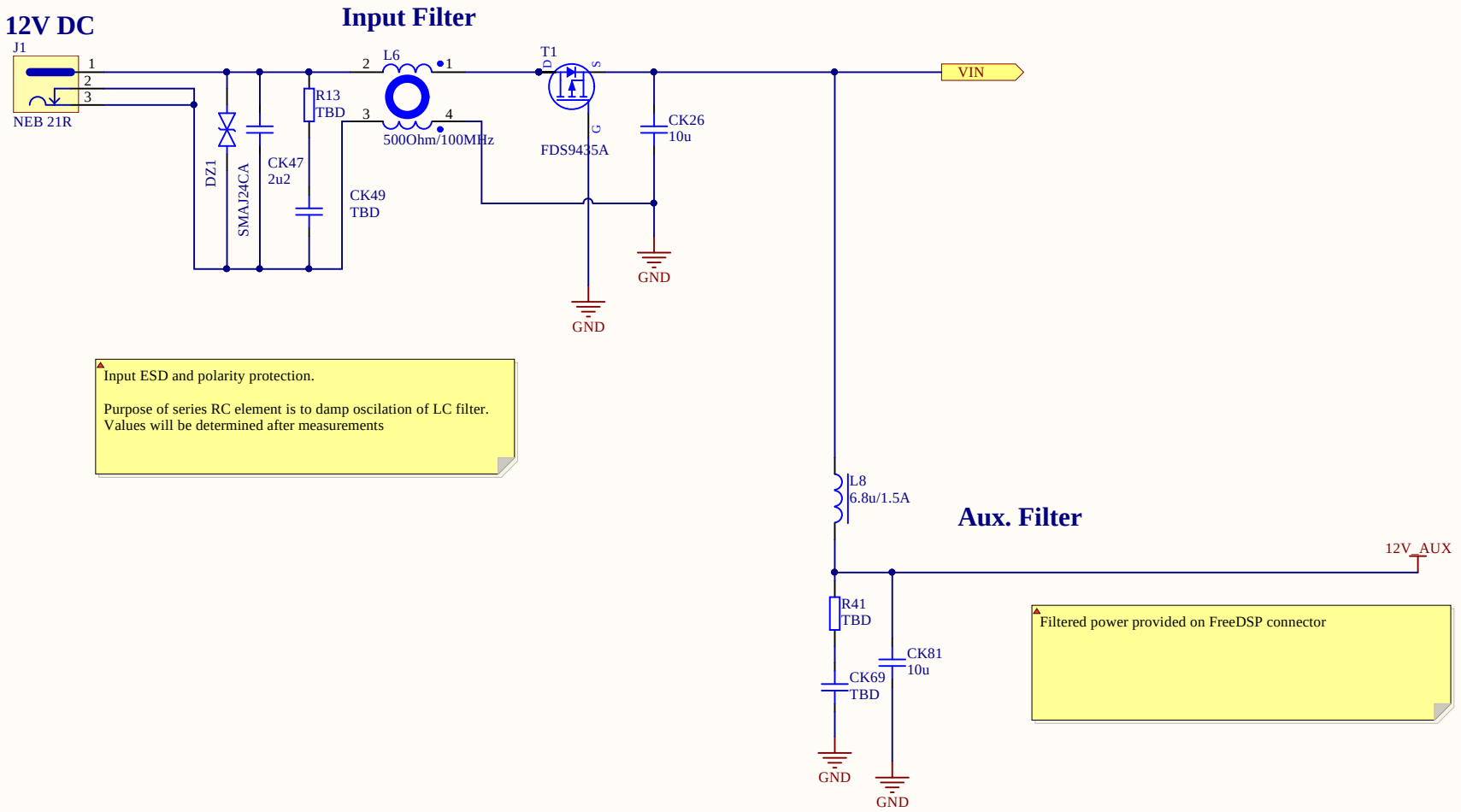


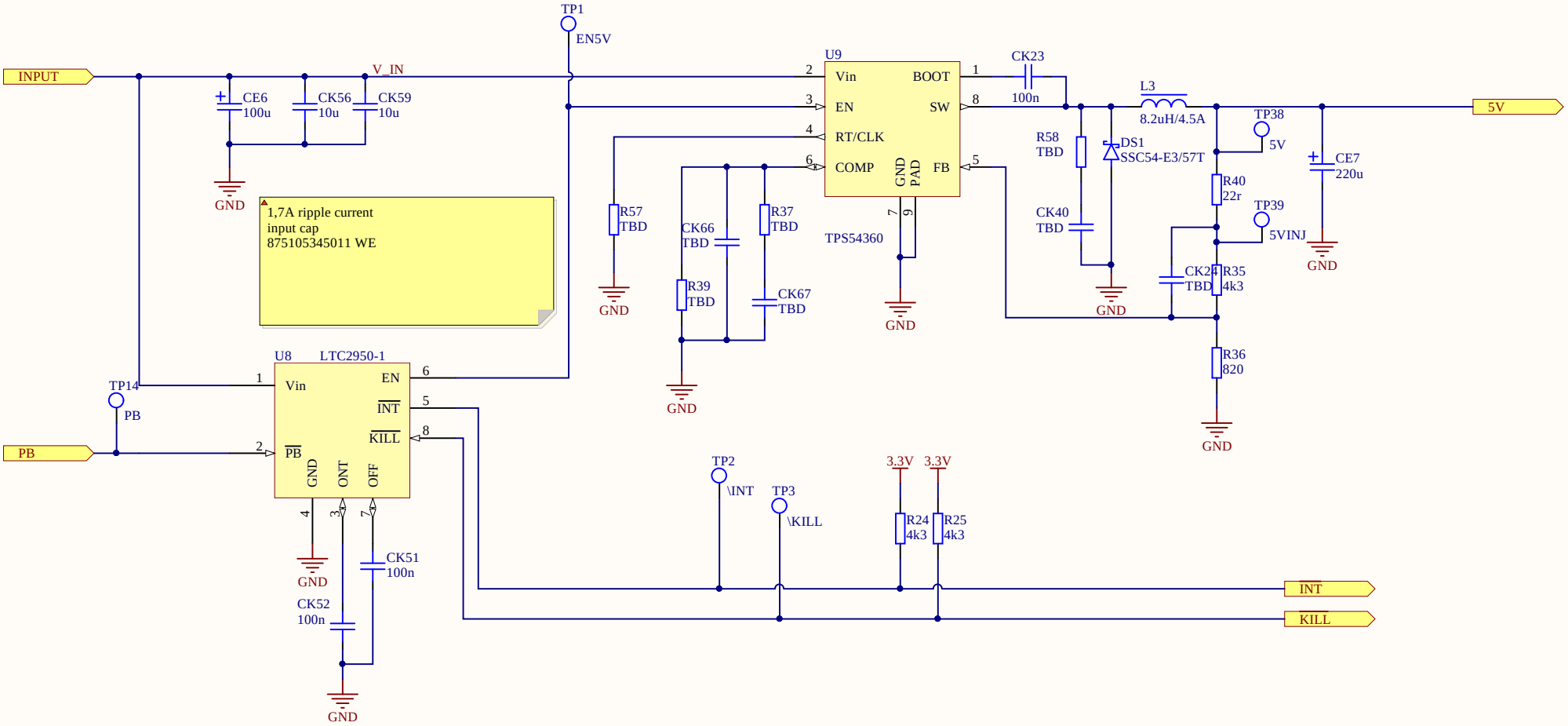
Title	***Top Sheet***		*FreeDSP*
Size: A4	Number:1	Revision:*	*
Date: 17.10.2016	Time: 20:29:09	Sheet1 of 16	*
File: C:\Projekty_PiDSPBig\PCB\DSP.SchDoc			*

Altium


Input
InputFilter.SchDoc
VIN
Buck
Buck+PM.SchDoc
INPUT
KILL
INT
PB
5V
DSP_DIS
PM
DSP_DIS
KILL
INT
PM
PB
Net Class
5V
R38
1k5
DL3
GND
PiDSP is turned on by default, it can be disabled by setting '1' on DSP_DIS
The main power supply(5V) is turned on by pushbutton controller, turn of either by button, or by kill singnal from RPi header.
Start up sequencing:
3V3 is started first in order to bias protection diodes (see Power-Up Sequence in datasheet)
PVDD is started second so clock oscilattors can start and stabilize before core startup
1V2(core) is the last one to start.
TP9
\EN3.3V
3.3V&1.2V
TPS54292.SchDoc
Input
Out1
EN2
EN1
Out2
Net Class 1.2V
Net Class 3.3V
TP11
ENPVDD
PLL Reg.
Vin
En
Vout
Net Class
PVDD
R20
4k3
CK63
100n
GND
TP12
\EN1.2V
CK64
100n
5V
R76
4k3
DT2
BSS138
G
S
TP13
DSP_DIS
DT4
BSS138
DSP_DIS
R81
4k3
R83
4k3
RC values TBD, based on testing
GND
Decoupling Capacitors
TP45
TP7
TP10
TP34
TP35
TP36
TP37
TP28
TP29
TP30
TP31
TP32
TP33
GND
Title Power Supply
Size: A4
Number:2
Revision:*
Date: 17.10.2016
Time: 20:29:09
Sheet2 of 16
File: C:\Projekty_PiDSPBig\PCB\PowerSupply.SchDoc
FreeDSP
Altium



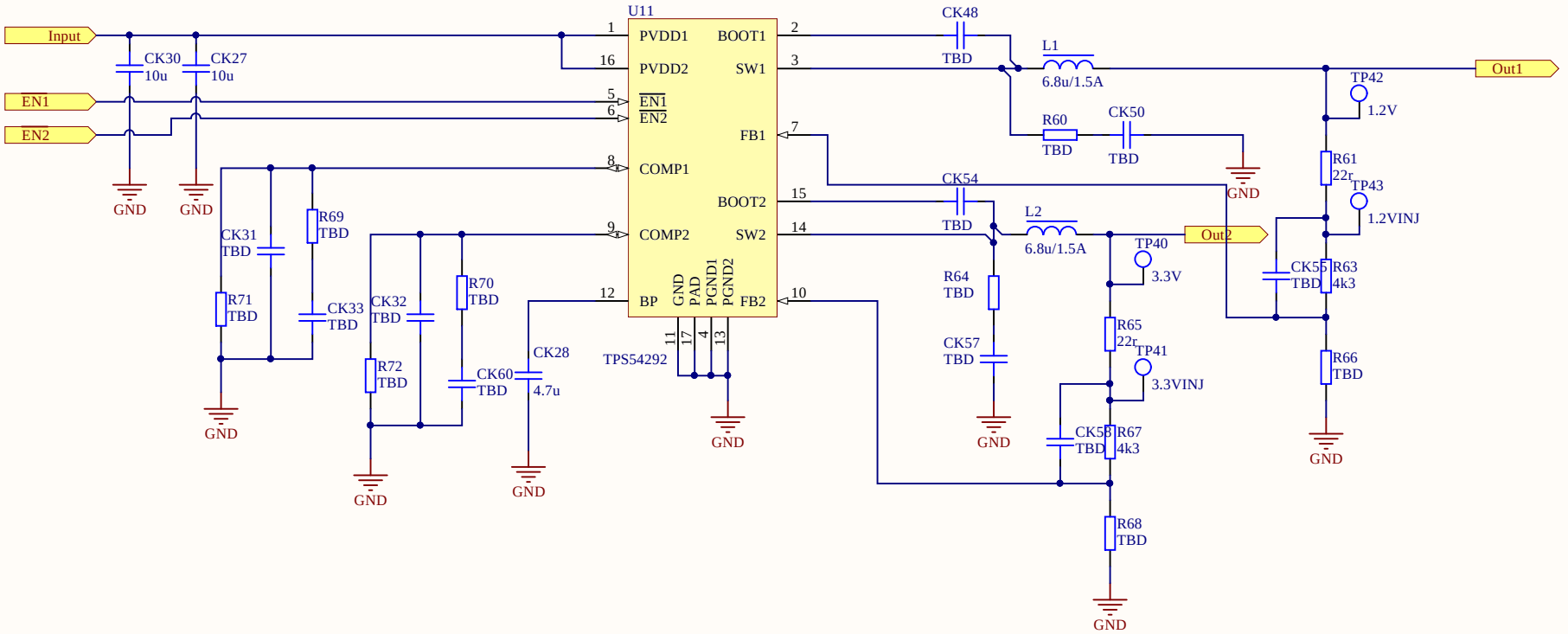
Title	***Input Filter***		*FreeDSP*
Size: A4	Number:3	Revision:*	*
Date: 17.10.2016	Time: 20:29:09	Sheet3 of 16	*
File: C:\Projekty_PiDSPBig\PCB\InputFilter.SchDoc			*



Title	**5V Regulator**		*FreeDSP* * * * *
Size: A4	Number:4	Revision:*	
Date: 17.10.2016	Time: 20:29:09	Sheet4 of 16	
File: C:\Projekty_PiDSPBig\PCB\Buck+PM.SchDoc			

3.3V and 1.2V Regulator

3.3V - IOVDD + general use. Output is aviable on front panel connector.
1.2V - ADAU core
Powered from 5V



Title	*3.3V + 1.2V Regulator*		*FreeDSP*
Size: A4	Number:5	Revision:*	
Date: 17.10.2016	Time: 20:29:09	Sheet5 of 16	
File: C:\Projekty_PiDSPBig\PCB\TPS54292.SchDoc			

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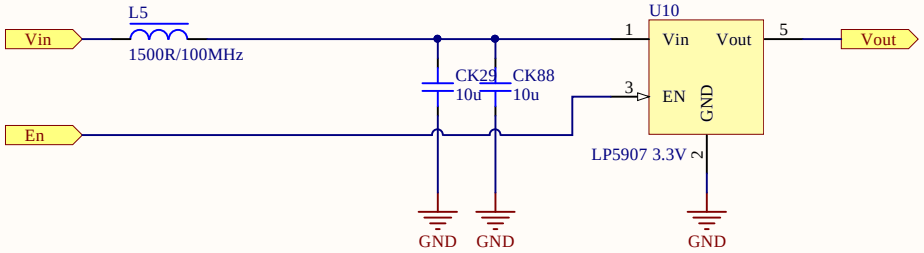
3.3V PVDD Regulator

Low noise regulator provides 3.3V for oscillators and AVDD and PVDD of ADAU1452.
Powered from 5V rail.



Title **PVDD Regulator**			*FreeDSP* * * * *
Size: A4	Number:6	Revision:*	
Date: 17.10.2016	Time: 20:29:09	Sheet6 of 16	
File: C:\Projekty_PiDSPBig\PCB\LP5907MFX-3.3NPB.SchDoc			

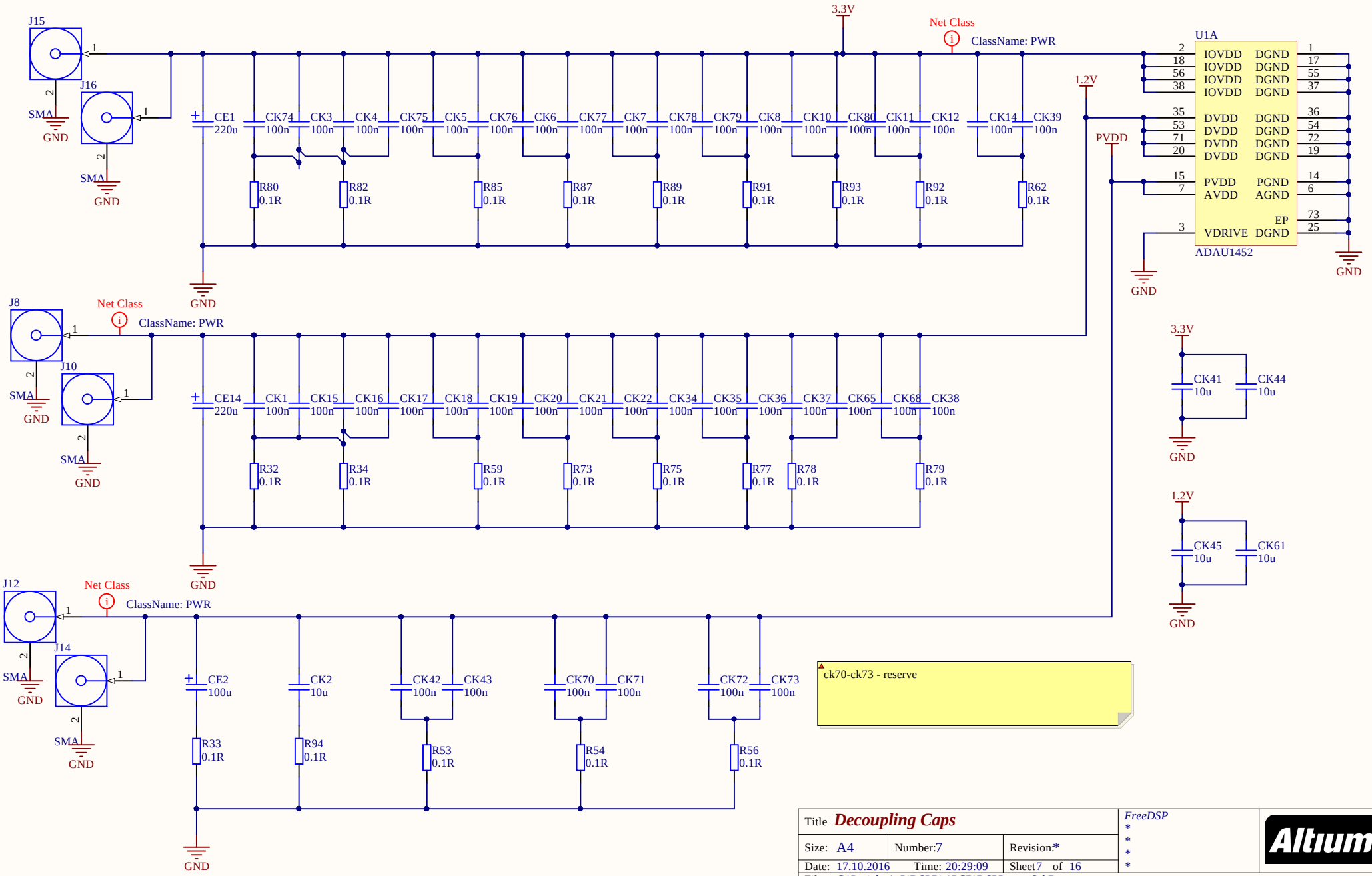

J15
J16
SMA
GND
3.3V
Net Class
ClassName: PWR
1.2V
PVDD
U1A
IOVDD
DVDD
PVDD
AVDD
DGND
PGND
AGND
EP
VDRIVE
ADAU1452
CE1 220u
CK74 100n
CK3 100n
CK4 100n
CK75 100n
CK5 100n
CK76 100n
CK6 100n
CK77 100n
CK7 100n
CK78 100n
CK79 100n
CK8 100n
CK10 100n
CK80 100n
CK11 100n
CK12 100n
CK14 100n
CK39 100n
R80 0.1R
R82 0.1R
R85 0.1R
R87 0.1R
R89 0.1R
R91 0.1R
R93 0.1R
R92 0.1R
R62 0.1R
J8
J10
CE14 220u
CK1 100n
CK15 100n
CK16 100n
CK17 100n
CK18 100n
CK19 100n
CK20 100n
CK21 100n
CK22 100n
CK34 100n
CK35 100n
CK36 100n
CK37 100n
CK65 100n
CK68 100n
CK38 100n
R32 0.1R
R34 0.1R
R59 0.1R
R73 0.1R
R75 0.1R
R77 0.1R
R78 0.1R
R79 0.1R
CK41 10u
CK44 10u
CK45 10u
CK61 10u
J12
J14
CE2 100u
CK2 10u
CK42 100n
CK43 100n
CK70 100n
CK71 100n
CK72 100n
CK73 100n
R33 0.1R
R94 0.1R
R53 0.1R
R54 0.1R
R56 0.1R
ck70-ck73 - reserve
Title Decoupling Caps
Size: A4
Number:7
Revision:*
Date: 17.10.2016
Time: 20:29:09
Sheet7 of 16
File: C:\Projekty_PiDSPBig\PCB\DSPPower.SchDoc
FreeDSP
Altium

Table 8. Input Mux and Output Enable Logic

CLK_SEL	CLK0	CLK1	OE[1]	Q[2]
L	L	X	H	L
L	H	X	H	H
H	X	L	H	L
H	X	H	H	H
X	X	X	L	Tri-state

Notes:
1. Output enable active high.
2. On the next negative transition of CLK0 or CLK1.

OE features internal pull-up

Clock Buffer

ClassName: CLK
ClassName: 50R
Net Class

U2
Si53360

R8 22R
R16 22R
R18 22R
R19 22R

J9

CLK
MCLK1
MCLK2
MCLK3
MCLK

UFL connector provides high fidelity clock signal to other boards in system.

MCLK is also provided on FreeDSP connector

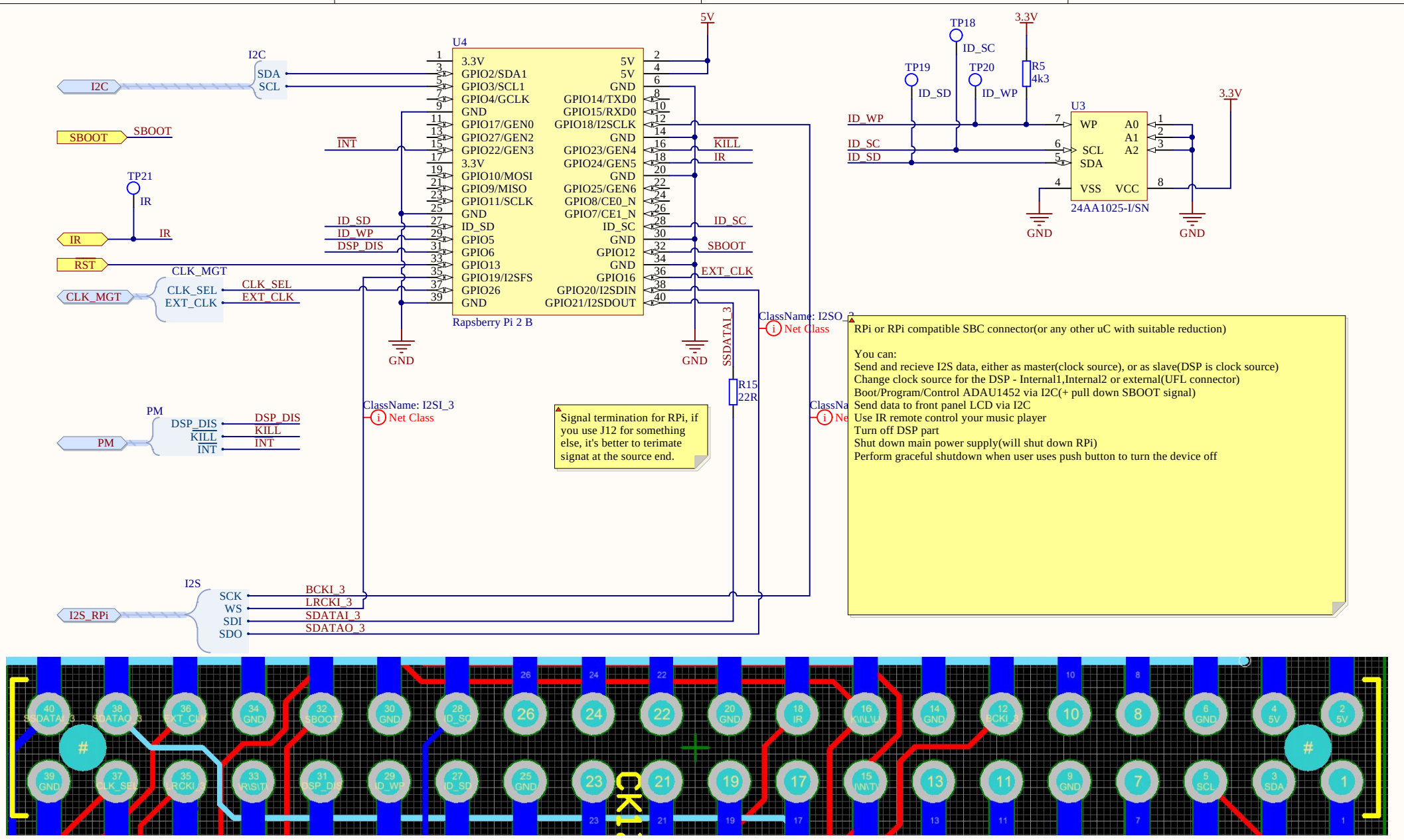
Oscillators

TP5 EXT_CLK
TP4 CLK0
J7
CLK_IN
Net Class
ClassName: CLK
ClassName: 50R
R42 4k3
CLK_MGT
EXT_CLK
CLK_SEL
R10 4k3
TP6 CLK_SEL
TP17 CLK_DSP
X1 NZ2520SD
X2 NZ2520SD
R43 4k3
TP8 CLK_SEL_X2
DT3 BSS138

X1 is enabled by defalut.
In order to switch to X2, set CLK_SEL to '1'

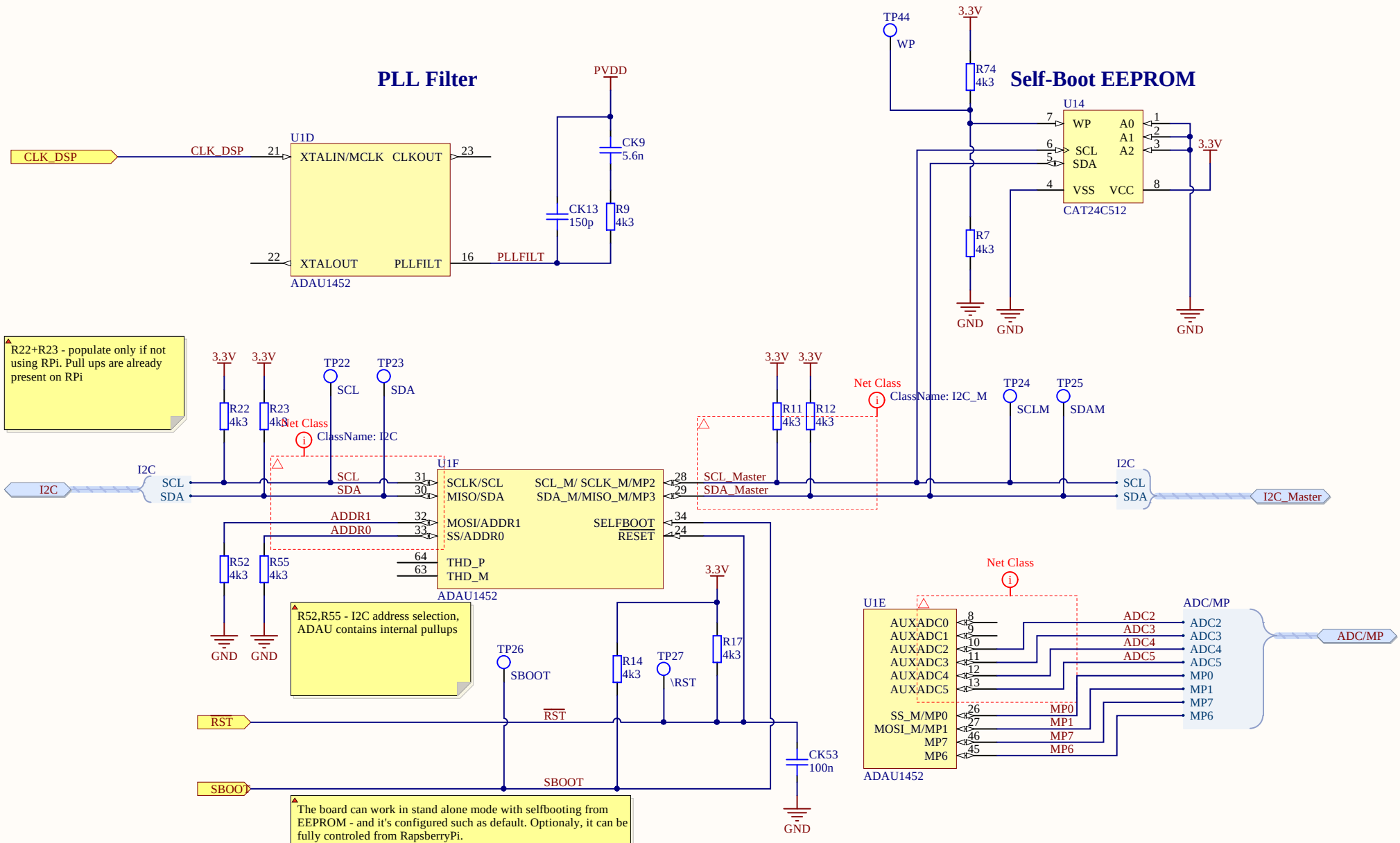
On board oscillators are used by defalut.
In order to use external clock, set EXT_CLK to '1'

Title	Clock Management		FreeDSP
Size: A4	Number:8	Revision:*	
Date: 17.10.2016	Time: 20:29:09	Sheet8 of 16	
File: C:\Projekty_PiDSPBig\PCB\DSPclk.SchDoc			

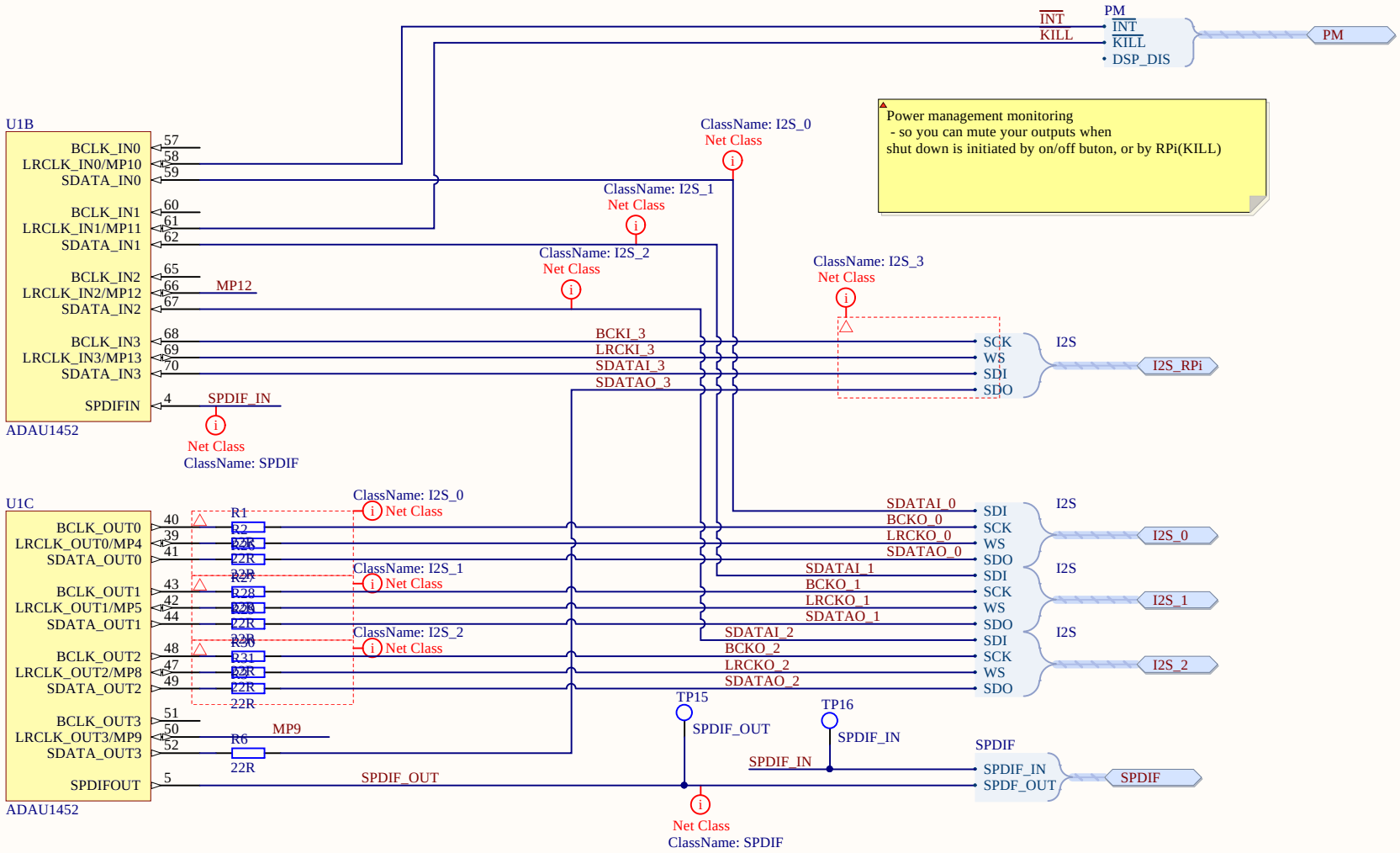


Title	**RPi**		*FreeDSP*
Size: A4	Number:9	Revision:*	
Date: 17.10.2016	Time: 20:29:09	Sheet9 of 16	
File: C:\Projekty_PiDSPBig\PCB\RPi&MCU.SchDoc			

Altium



Title	***DSP Control***		*FreeDSP*
Size: A4	Number:10	Revision:*	
Date: 17.10.2016	Time: 20:29:10	Sheet 10 of 16	
File: C:\Projekty_PiDSPBig\PCB\DSPcontrol.SchDoc			



Title **DSP I/O**			*FreeDSP* * * * *
Size: A4	Number:11	Revision:*	
Date: 17.10.2016	Time: 20:29:10	Sheet11 of 16	
File: C:\Projekty_PiDSPBig\PCB\DSP_DIO.SchDoc			