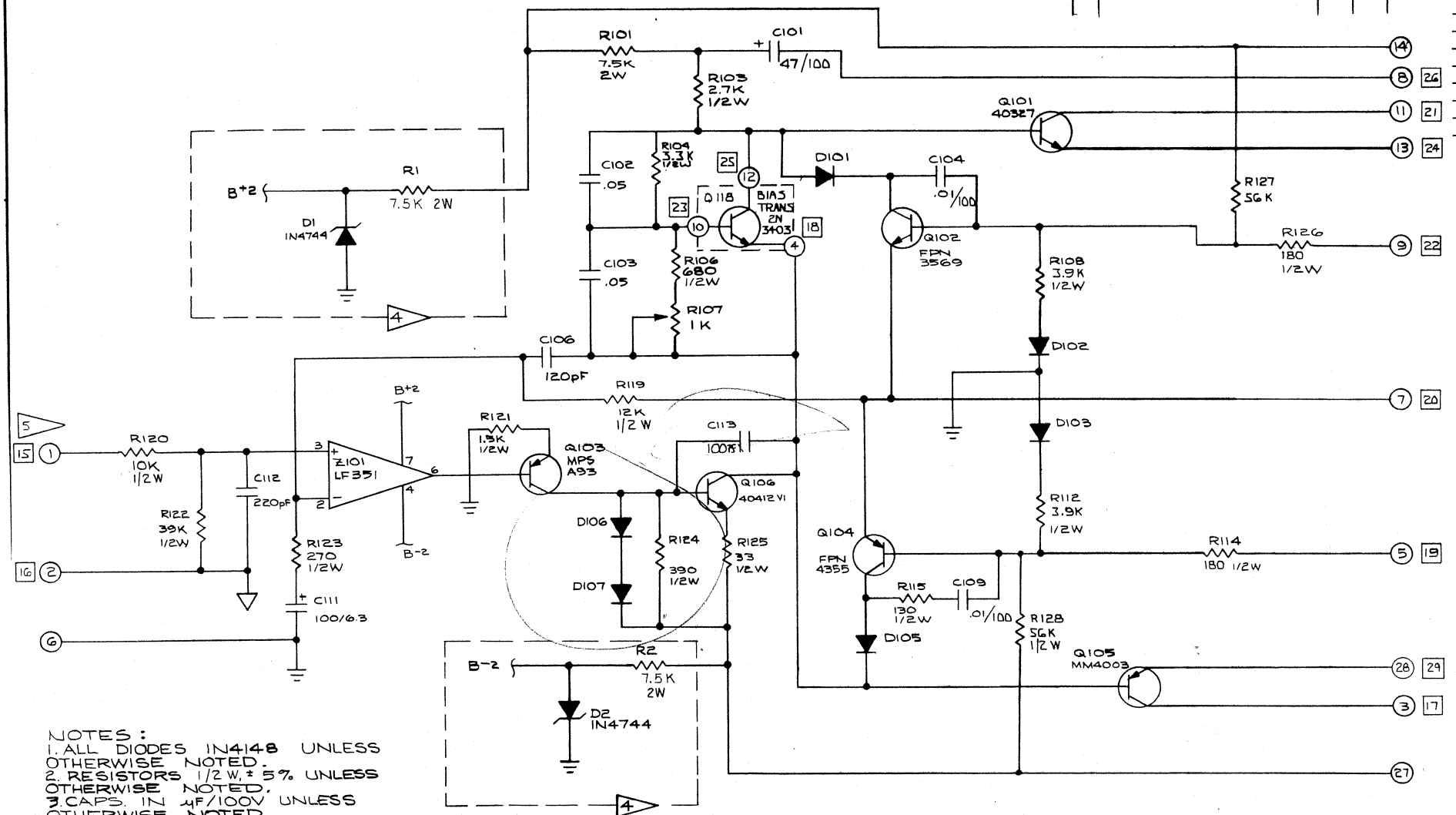
REVISIONS				
LTR	DESCRIPTION	BY	DATE	APPROVED
A	PER ECO 1049	[illegible]	1-31-80	



NOTES:
1. ALL DIODES IN4148 UNLESS OTHERWISE NOTED.
2. RESISTORS 1/2 W, ± 5% UNLESS OTHERWISE NOTED.
3. CAPS. IN µF/100V UNLESS OTHERWISE NOTED.
4. "200" SERIES REF. DESIGNATORS (NOT SHOWN) - IS IN IDENTICAL SCHEMATIC CONFIGURATION AS SCHEMATIC SHOWN, EXCLUDING COMPONENTS INCLUDED IN — 4
5. "BOXED" NUMBERS INDICATE CHANNEL B PIN-OUTS

UNLESS OTHERWISE SPECIFIED DIM. AND TOL. ARE IN INCHES AND SHALL BE INTERPRETED PER (ANSI) Y14.5-1966.
TOLERANCES ARE:
1 DEC ±: .1 3 DEC ±: .005
2 DEC ±: .01 4 DEC ±: .0005
ANGLES ±: 0° 30'
REMOVE BURRS, BRK SHARP EDGES MACH SURFACES
MAT'L:
FINISH:
HT. TREAT:

DRAWN	[illegible]	6/13/77
CHECKED	TLP	12/29/77
APPROVED		/ /
RELEASE STATUS		
PREL.		/ /
FINAL		/ /
		/ /
		/ /
DO NOT SCALE DWG.		

Phase Linear

PCB SCHEMATIC
AMPLIFIER
700/400 SERIES TWO (COMP)

SIZE	DWG. NO.	REV.
C	PL 36 210-0290-0	A

SCALE: NONE SHEET 1 OF 1