

PASS LABS ALEPH 0 SERVICE MANUAL REV 1.4 - 1.6

PRODUCT DESCRIPTION

The Aleph 0 is a high performance Mosfet single-ended Class A audio power amplifier, intended for maximum performance in reproduction of music. It is a simple design, having only three gain stages: input differential pair, cascoded voltage gain stage, and output followers. All three gain stages are biased by current sources from the negative supply. The output stage will operate as a single ended system at lower power levels and will operate as a push-pull system at levels above the bias point of the constant current source.

Revision 1.4 and 1.6 represent the first major revisions since product inception in 1992. Rev 1.4 began with serial numbers above 4500. There were only a few pieces of Rev 1.4 produced, and they incorporated an auto-standby circuit to lower dissipation in the amplifier when it was unused. It was dropped in Rev 1.6 by customer demand. Rev 1.5 was an in-house prototype, which was not released.

SIMPLIFIED SCHEMATIC

To best understand the operation of the amplifier, refer to the simplified schematic Figure 1. The front end of the amplifier accepts a balanced or unbalanced input signal at two N channel Mosfets operating as a differential pair. They are provided with bias by a current source from the negative rail which operates at a constant 10 milliamps. The output of the differential pair drives a P channel Mosfet which provides voltage and current gain. At the output of this second stage you will see the full voltage swing of the amplifier.

This second gain stage is provided with a single-ended Class A current bias from another current source from the negative supply which provides a constant 40 milliamps current. Between the current source and the drain of the P channel device is a constant voltage source which is used to provide voltage bias to the output Mosfet transistors.

The amplifier has N channel output transistors operated as source followers, so that they provide only current gain. High current single ended Class A bias is provided by a current source from the negative supply. This current source provides greater than 2 amps of constant current, which can be modulated by the P channel level shifting transistor to produce greater amounts of negative current on demand past the bias point. The control circuitry of the current

source is further set up to behave as if a negative 16 ohm resistor were placed in parallel with it, extending the bias range of the output stage.

COMPLETE SCHEMATIC

For purposes of clarity and simplicity, the complete schematic of the Aleph 0 is broken up into the following sections: Power supply, Output Stage, and Front end.

Figure 2 shows the power supply schematic. An IEC standard AC line connector connects to the primary of a toroidal power transformer through a fast blow fuse, a power switch, and power inrush suppression thermistor. Fig 2 shows the transformer wired for 120 VAC, and the transformer can be adapted to 240 VAC by connecting the two primary windings in series.

The unregulated secondary system consists of a bridge rectifier, and four 31,000 uF capacitors. The secondary DC voltage is approximately plus and minus 40 volts. Note the power thermistor which connects the earth ground to the chassis and circuit ground.

The blue LED indicator runs off the unregulated supply, and it remains lit for a period of time after the amplifier is shut down. It amuses the designer.

Fig 3 shows the output stage block, as found on each transistor mounting bar in the amplifier.

There are 4 such blocks in the amplifier, all identical. Two blocks are in parallel on the positive half of the output stage, and two are in parallel on the negative half. Note that all the output devices are matched for gate to source voltage within .1 volts. The voltage match is written in felt pen on each output device, and it is necessary to obtain transistors with this number when requesting output transistors for repair.

Figure 4 shows the front end schematic. Schematics for Rev 1.4 and Rev 1.6 are both provided, as well as component layout diagrams on their respective PC boards.

The essential difference between versions 1.4 and 1.6 are the removal of the auto-standby circuit for the bias in rev 1.4, which is the circuitry comprised of Q1 1, Q12, D1, D2, C10 and associated resistors. Also in Rev 1.6 the input high frequency rolloff capacitors have been removed. and various bleed resistors have also been removed, as well as several electrolytic capacitors in the current source bias circuitry.

The basic signal path remains the same, however. Note that the schematic for Rev 1.6 also shows the output stage for the amplifier.

Referring specifically to the schematic for Rev 1.6, the operation of the circuitry is as follows:

The circuitry formed by Q5 and Q7 are constant current sources which are designed to power up the circuits which comprise the front end gain stage of the amplifier.

Current through R15 biases the zener diode Z3 to set a reference 9.1 volts for Q5 and Q7, each of which drives a constant 5 volts across their sources resistances R19 and R18. This makes them act as constant current sources.

Q5 sources 10 ma to the differential input pair Q1 and Q2. Q7 sources 40 ma for the second gain stage of the amplifier.

Q1 and Q2 are attached to the input and feedback signals through the differential networks of R1 through R6 and single-ended input R7. They are protected by zener diodes Z1 and Z2.

The output (drains) of Q1 and Q2 drive P channel gain device Q4, which is cascoded by Q7. Potentiometer P1 is used to set the DC offset of the amplifier.

Q7 provides a constant voltage load for Q4, reducing distortion, and is controlled by zener diode Z4. Z5 protects Q7.

The drain (output) of Q7 attaches to the constant current source Q7 through the voltage source bias network formed by Q3 and R14 and P2. Bias adjustment of the amplifier is accomplished through P2.

You will notice that throughout the amplifier, Mosfets have 221 ohms in series with their gate pins. This is to prevent parasitic oscillations on devices. Similarly, you will notice that virtually all Mosfets are protected from electrostatic discharge by zener diodes.

The output of Q7 directly drives the positive half of the output stage, follower transistors Q10 - Q13.

The negative half of the output stage, Mosfets Q14 - Q17 are biased up as constant current sources by the circuitry of Q9, R24, R25, and R26. R23 is used to provide a slight negative resistance to the character of the constant current source.

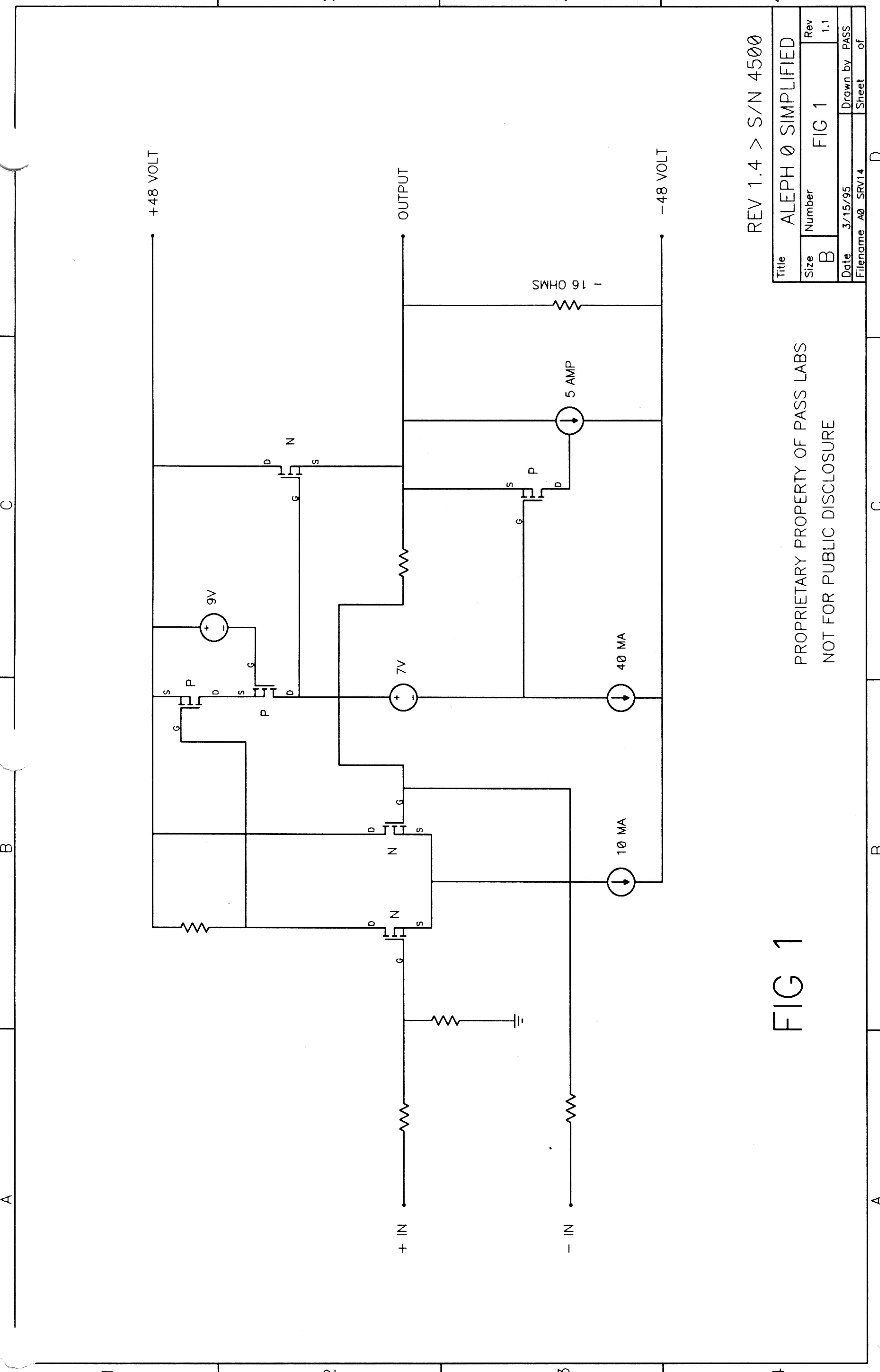
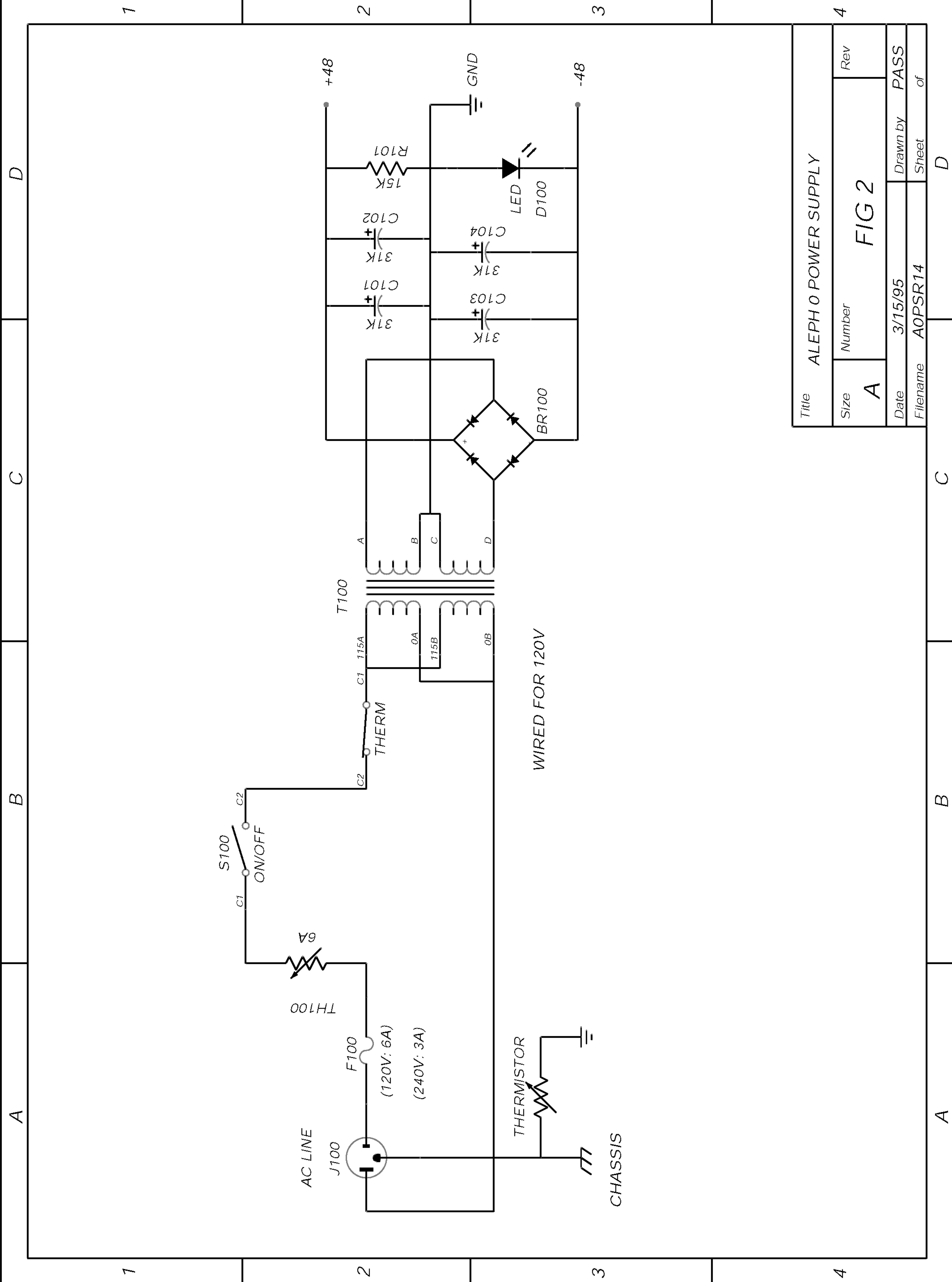


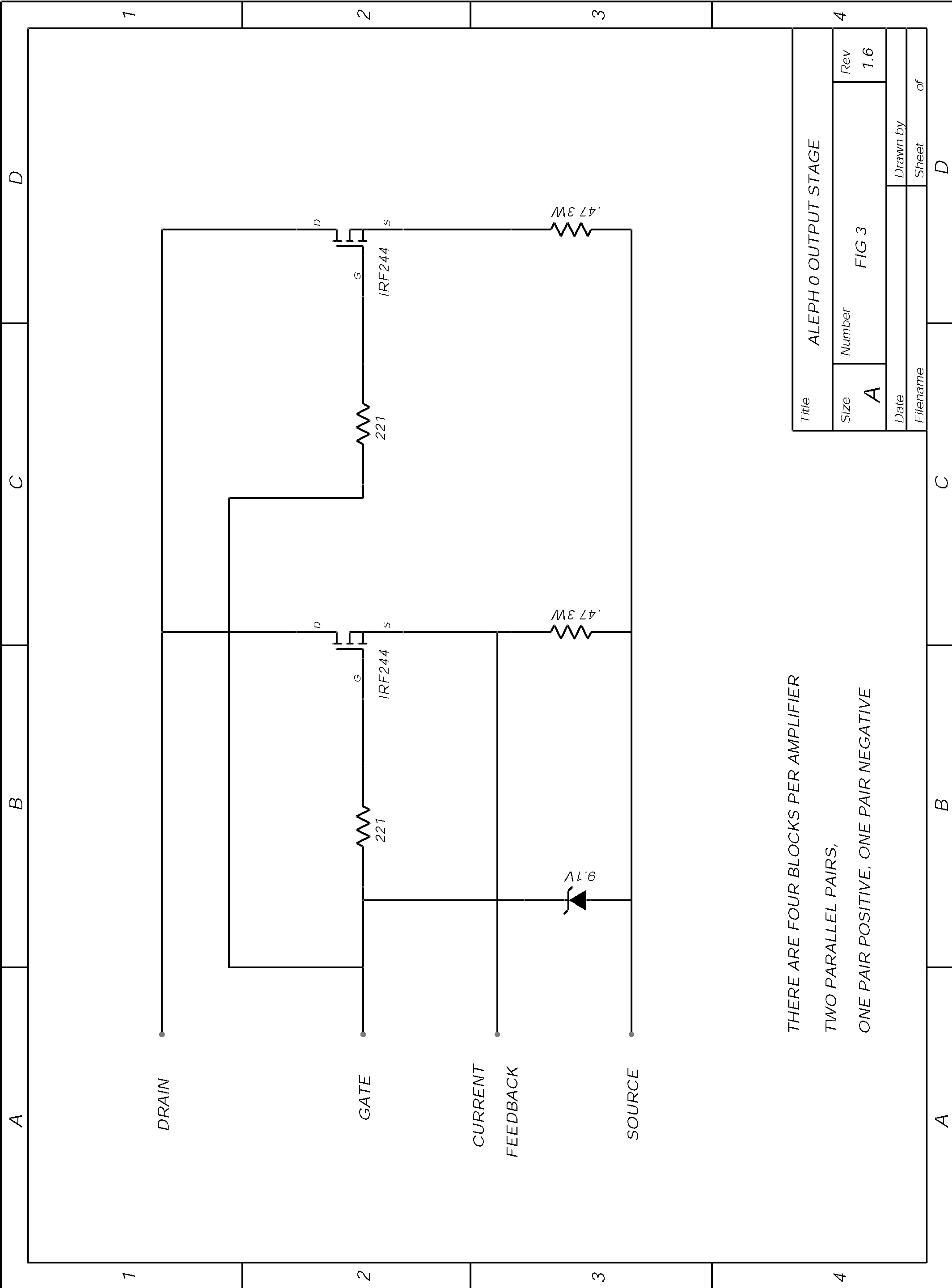
FIG 1

REV 1.4 > S/N 4500

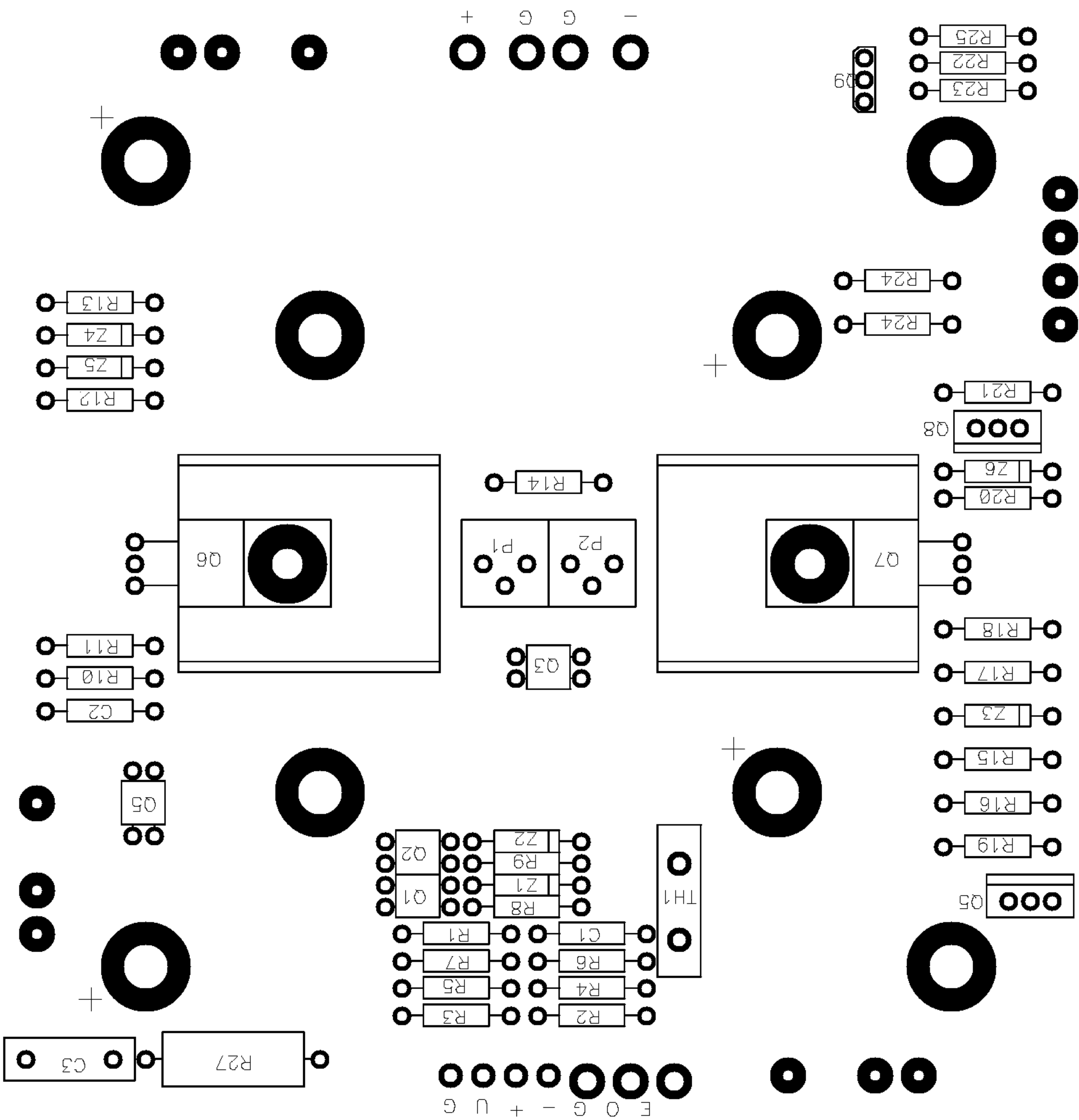
Title ALEPH Ø SIMPLIFIED			
Size B	Number	FIG 1	Rev 1.1
Date 3/15/95		Drawn by PASS	
Filename A0 SRV14		Sheet of	

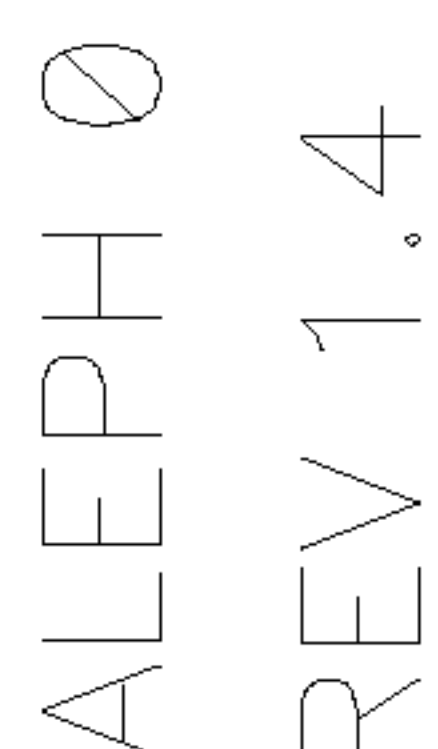
PROPRIETARY PROPERTY OF PASS LABS
NOT FOR PUBLIC DISCLOSURE





GREEN IN
WHITE IN
RED IN
BLACK IN
BLK OUT
RED OUT
GREEN EARTH





Q8 is set up as a level shifting device which will increase the drive of the negative output stage when the bias current is insufficient to drive the output load. It delivers current through R22 which overcomes the regulation characteristic of Q9, allowing for higher current through Q14 - Q17.

And that's it.

ADJUSTMENTS AND SERVICE

Initial power up procedures: For an amplifier in unknown adjustment or being powered up for the first time after repair or modification.

Minimum Essential Equipment: Oscilloscope, Audio signal source, Variable AC power source, True RMS AC line current meter, 8 ohm load.

A distortion analyzer is very helpful confirming proper operation, but is not essential to adjustment of an otherwise working amplifier.

If you do not have a True RMS reading AC line current meter, you may place a .1 ohm 5 watt power resistor in series with the AC line (cold) and measure the voltage across it ($1 \text{ amp} = .1 \text{ volt AC}$), taking care not to electrocute yourself. You must use a True RMS. AC voltmeter to read the voltage across the resistor. An averaging AC voltmeter will not do it.

Procedure:

Place P1 potentiometer in mid-position

Place P2 in full counterclockwise position

Check the AC line fuse

Set signal source to .1V at 1 KHz

Attach signal source

Attach 8 ohm load.

Monitor the amplifier output with oscilloscope, Set the AC line source to 0.

AC power switch on

Slowly turn up the AC line voltage to 1/3 while watching the current draw.

The current draw will initially be twice that of normal operation, and will decrease as power supply voltage is increased.

Approximate Initial current draw: 4 A RMS. for 120 VAC units, 5 A RMS. for 100 VAC units, 2 A RMS. for 240 VAC units.

At 1/3 input AC voltage, if the current draw is approximately at these values, check to see if the amplifier is producing the appropriate output voltage, which should be 1 volt AC. Adjust P1 for low DC offset.

If there is any question about whether any power transistors may have been damaged, or if you have replaced any output transistors or components on the output stage boards, at this point, confirm the equal sharing of current through all output transistors by measuring the DC drop across each source resistor for each power transistor. They should all be close, within .1 volts, and at approximately .5 volts each. You must remove the heat sinks to do this before you power the amplifier up. After you confirm the current through each device, power the amplifier down. Replace the heat sinks, making certain that the screws holding the sinks are sufficiently tight, *not too tight*, and power the amplifier back up to 1/3 VAC.

If it looks good at this point, you may increase the AC power slowly. As you do so, you should see the current draw decline to approximately 1/2 of its initial value.

If operation seems OK at full AC power, turn bias pot P2 clockwise until a slight increase in current draw is seen.

Then increase the signal level to full output of the amplifier, verifying proper operation into 8 ohms up to clipping. With the bias set low, there will be some distortion at higher power levels, which is expected.

The potentiometers P1 and P2 are accessible through holes in the top cover, so that adjustment of bias and offset need not require disassembly. Never adjust either of these potentiometers without monitoring the AC current draw of the amplifier. The Aleph O has no other adjustments.

Using the True RMS. reading of the AC line current draw, adjust bias potentiometer P2 so that the amplifier draws 250 watts.

For a 120 VAC line, this will be 2.1 amps RMS. For a 240 Volt line, this will be 1.05 amps RMS. For a 100 volt line, this will be 2.5 amps RMS.

Let the amplifier warm up for 1/2 hour. Readjust the DC offset and the bias.

Let the amplifier warm up for another hour. Readjust the DC offset and the bias.

Let the amplifier warm up for another 1/2 hour. Readjust the DC offset and the bias.

The temperature of the heat sinks should be 50 degrees Centigrade or so.

55 degrees is a little too hot. 45 degrees is a little too cold.

50 degrees is just right.

If the amplifier operates at 50 degrees or so after 2 hours of operation, and the DC offset is less than 50 mV, then you are done.

NOTE

If you don't have a TRUE RMS voltmeter for measurement of the current draw across the .1 ohm resistor, you really ought to get one. If all you have is some inaccurate way of measuring the AC line current, then use it as best you can, very slowly increasing the bias current over several hours until you can confirm that the heat sinks are constantly at 50 degrees Centigrade. Take your time, or you will be repairing the amplifier all over again.

Remember that 50 degrees Centigrade is just about at the limit for what you can comfortably touch. If you can hold the heat sink for 15 seconds, it is not too hot.

Notes on transistor matching:

Input Mosfets (IRFD110 or IRFD210) must have their threshold voltages matched to about 10 mV at 5 mA of current. This is accomplished by attaching the gate to drain and passing 4 mA of current through the device, typically with a 15 volt source and 220 ohms resistance. The voltage from the gate/drain to the source is measured. The devices to be matched must be under the same conditions and temperature.

Output Mosfets (TO-3 packages) must be matched to within 100 mv at 200 mA of current. The same procedure applies, except that 50 ohms is used.

PERFORMANCE SPECIFICATIONS

Gain	20.0 dB balanced (50 Ohm Source) 19.9 dB unbalanced 25.5 dB unbalanced with jumper, XLR pins 1,3
Freq. Response	0dB@DC -3dBat100 KHz
Power Output	75 watts @ 8 ohms 20 Hz - 20 KHz
Distortion	<1 %THD
Maximum Output	50 amps (pulse), 40 volts (peak)
Output Impedance	.01 ohm @ 1 KHz @ 8V @ 8 ohm
Input Impedance	25 KOhm, differential (XLR) 10 KOhm single-ended (RCA)
Common mode rejection	70dB @ 1 KHz @ .1V input common ground
Output Noise	600 microvolts
DC offset	100 mv after warm-up, balanced mode
Power Consumption	250 watts at idle
Operating Temperature	50 degrees C.
Warm up time	1 hour minimum