increasing LOAD current demand, J1 source current increases, simultaneously increasing J1 VDS and decreasing J2 VGS, moving J2 toward pinch off. Pinch off limits source current of J2 and thus J1, limiting current to Q1 base and thus limiting current to LOAD. The circuit in FIG. **5** allows output current limiting while keeping output impedance equal to the lowest possible value, that of a bipolar emitter follower transistor. It has a disadvantage of increasing the dropout voltage by the VDS of J2, which is small at nominal drain current and can be avoided completely by using a separate power supply at the collector of Q1 as with FIG. **6**.

[0044] FIG. **6**

[0045] Use of a separate power supply VLDO provides the benefit of limiting maximum output current with zero additional output impedance as in FIG. **5**, plus the benefit of even lower dropout voltage. Q1 collector is powered separately with voltage VLDO which is lower than VIN as shown in the embodiment of the invention in FIG. **6**, allowing the dropout voltage of the power delivery device Q1 to approach the saturation voltage of a bipolar transistor, which is on the order of 0.2V to 1V depending on the specific transistor used for Q1 and on the load current.

[0046] FIG. **7**

[0047] FIG. **7** illustrates an embodiment of the invention whereby the output signal is a precision constant current. The ground reference point is moved to the positive terminal of VIN , LOAD is between ground potential and the collector of Q1, and a fixed value resistor RSET is between VSET and the negative terminal of VIN . I_{LOAD} is calculated as VSET/RSET $-I_{BASE}$ of Q1. VSET is a regulated voltage equivalent to VOUT of FIG. **6** which, when imposed across RSET generates a fixed current from the emitter of Q1. At a fixed emitter current, Q1 base current is also fixed, generating a fixed current through LOAD equal to the difference of Q1 emitter and base currents. An additional voltage source VLOAD with a positive potential referenced to ground is used to supply the fixed current.

[0048] FIG. **8**

[0049] FIG. **8** illustrates an embodiment of the invention whereby the output signal is modulated using an AC signal or a combination of AC and DC as the reference basis, to provide voltage modulated power delivery. The resistor R12 of FIG. **4** is replaced in FIG. **8** by AC/DC SOURCE, which can be AC, DC or a combination of the two. The voltage source then drives the floating reference block **100**, such that

$$VOUT=(VREF*(1+R8/R9))+VACDC$$

where VOUT is no longer a fixed DC value but a variable value dependent on the value supplied by AC/DC SOURCE.

[0050] FIG. **9**

[0051] A negative voltage regulator is embodied in FIG. **9** using complementary device types, NPN instead of PNP and PJFET instead of NJFET, with the basic topology and function as described earlier for the positive voltage regulator in FIGS. **4** and **5**.

What is claimed is:

1. A voltage regulator circuit comprising:

an input terminal means for receiving power from an input voltage supply;

a common reference terminal means for providing a common voltage;

an offset voltage means for supplying a voltage offset difference between the common reference terminal means and a ground potential terminal means;

an output terminal means for delivering current to a load at a regulated voltage substantially independent of voltage transients on said input voltage supply and substantially independent of current transients on the output terminal means;

a current controlled output transistor having a first electrode connected to said input terminal means, a second electrode connected to said output terminal means and a third electrode means for controlling voltage at said second electrode;

a voltage controlled driver transistor having a first electrode connected to said input terminal means, a second electrode connected to the third electrode means of said current controlled output transistor and a third electrode to control current from the second electrode;

an output voltage sensing means for sensing at least a portion of said regulated voltage between said output terminal means and said offset voltage means;

a reference voltage generating means for generating a reference voltage having an output terminal means and a reference common terminal means; and

an error amplifying means for comparing voltage at said sensing voltage means with output voltage from said reference voltage generating means and for generating a control signal applied to said voltage controlled driver transistor third electrode, said error amplifying means comprising a positive input difference terminal, a negative input difference terminal, a positive power supply terminal, a negative power supply terminal and a difference output terminal.

2. The circuit of claim **1** wherein the voltage controlled driver transistor functions as a current control device with the voltage at the third electrode less than the voltage at the second electrode.

3. The circuit of claim **1** wherein the error amplifying means positive power supply terminal is connected to the output terminal means and the error amplifying means negative power supply terminal is connected to the common reference terminal.

4. The circuit of claim **1** wherein the output voltage sensing means includes a first resistor and a second resistor connected in series, a first end of the first resistor connected to the output terminal means, a second end of the first resistor connected to a first end of the second resistor and also to said error amplifying means negative difference input terminal, and a second end of the second resistor connected to said common reference terminal means.

5. The circuit of claim **1** wherein the offset voltage means is connected between the second resistor second end and said ground potential terminal means.

6. The circuit of claim **1** wherein said reference voltage generating means output terminal means is connected to said error amplifying means positive difference input terminal and a third resistor second end and with reference common terminal means connected to said offset voltage means.

7. The circuit of claim **1** wherein said third resistor first end is connected to the output terminal means, second end connected to the reference voltage generating means output terminal means and the error amplifying means positive difference input terminal, establishing a fixed current through the reference voltage generating means.

8. The circuit of claim **4** wherein a buffer transistor means for conducting the error amplifying means power supply current to said ground potential terminal means is connected

between the error amplifier negative power supply terminal and said ground potential terminal means.

9. The circuit of claim **5** wherein said offset voltage means comprises a fourth resistor between the common terminal means and the ground potential terminal, conducting a fixed current established by the sum of currents through said second resistor and said third resistor.

10. The circuit of claim **1** wherein a voltage controlled limit transistor limits current to said output terminal means, the voltage controlled limit transistor having a first electrode connected to said input terminal means, a second electrode connected to the voltage controlled driver transistor first electrode, said voltage controlled driver transistor first electrode no longer connected to said input terminal means, and a third electrode connected to the output terminal means.

11. The circuit of claim **10** wherein the current controlled output transistor has said first terminal connected to a low drop out power supply to provide a voltage less than the voltage supplied by said input terminal means.

12. The circuit of claim **1** wherein the current controlled output transistor has said first terminal connected to a load first terminal, load second terminal connected to a second power supply and said regulated output voltage connected to a fixed resistance first end, with the fixed resistance second end connected to said input voltage supply current return terminal means. Regulator delivers a constant fixed current to said load.

13. The circuit of claim **1** wherein the offset reference terminal is connected to an AC plus DC voltage source means for modulating the voltage at the output terminal means.

14. The circuit of claim **1** wherein complementary polarity devices deliver a complimentary polarity voltage at the output terminal means.

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