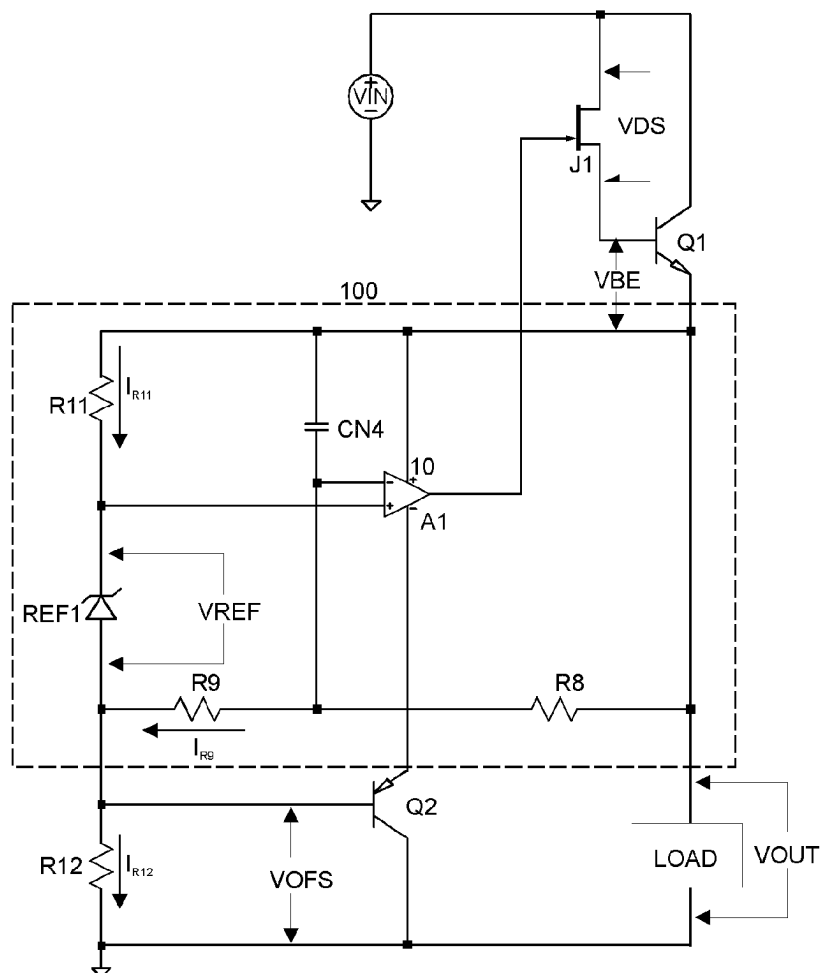


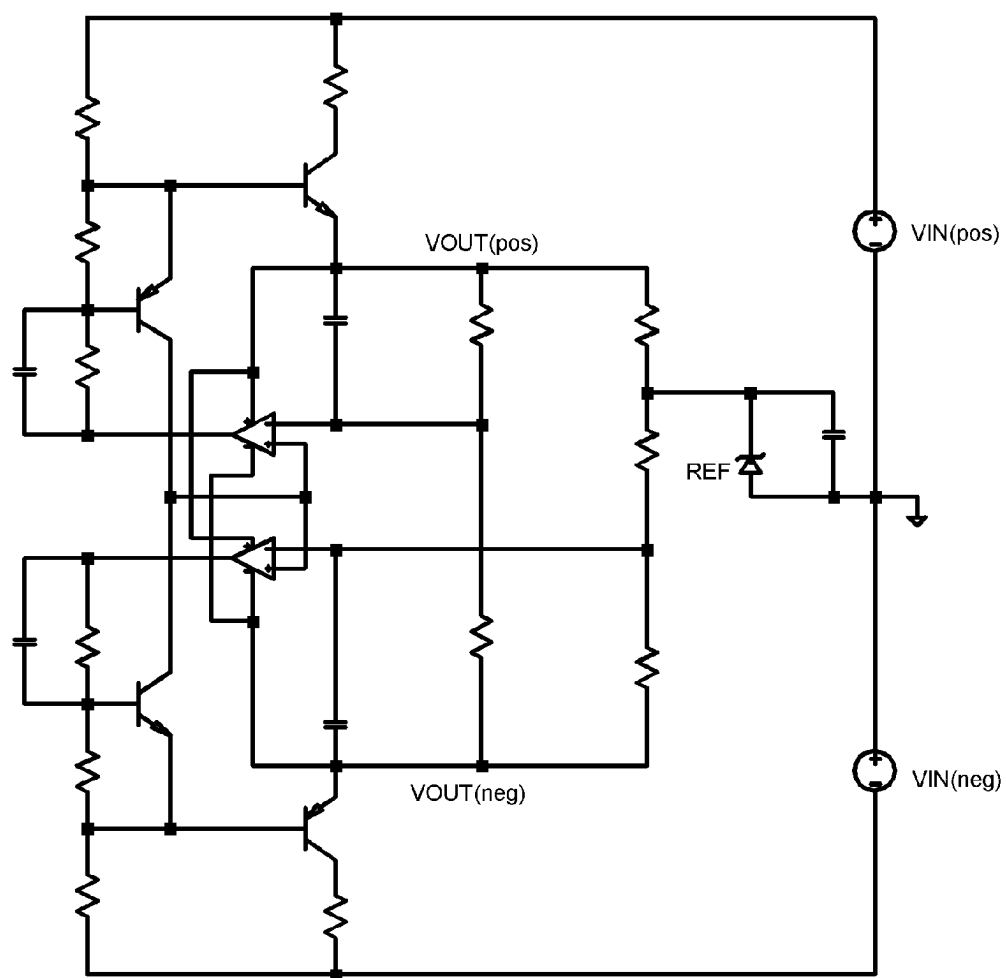


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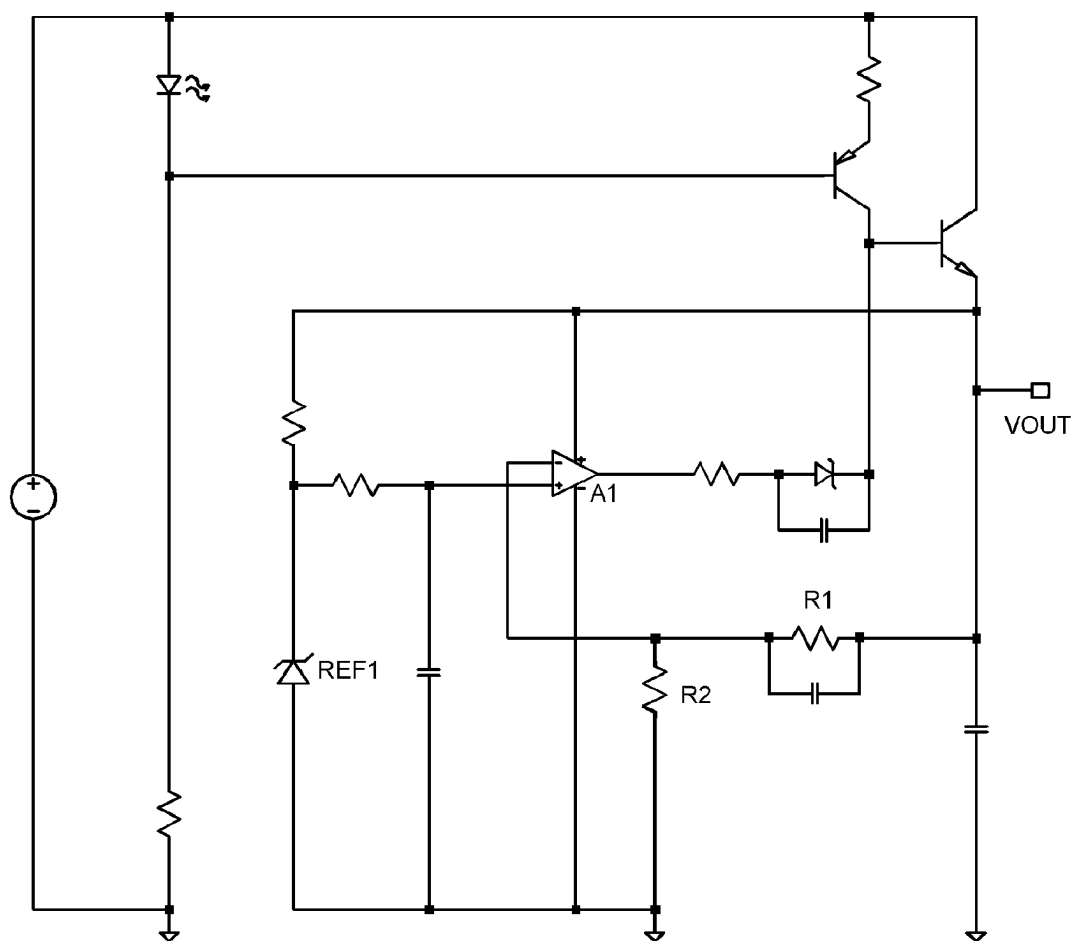
(19) **United States**(12) **Patent Application Publication**
Lowe, JR.(10) **Pub. No.: US 2010/0327834 A1**(43) **Pub. Date: Dec. 30, 2010**(54) **VOLTAGE REGULATOR USING DEPLETION
MODE PASS DRIVER AND BOOT-STRAPPED,
INPUT ISOLATED FLOATING REFERENCE**(52) **U.S. CL. 323/282**(76) Inventor: **Brian Albert Lowe, JR., Greer, SC
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317 Silver Creek Rd
Greer, SC 29650 (US)(21) Appl. No.: **12/728,211**(22) Filed: **Mar. 20, 2010****Related U.S. Application Data**(60) Provisional application No. 61/221,042, filed on Jun.
27, 2009.**Publication Classification**(51) **Int. Cl.**
G05F 1/10 (2006.01)(57) **ABSTRACT**

Multiple embodiments of a linear voltage regulator are described that use a bipolar output transistor to deliver current and a regulated voltage to a load. The bipolar output transistor assures low output impedance providing isolation from load induced noise. A first depletion mode field effect transistor FET drives the output transistor dependent on a correction signal from an error amplifier. The error amplifier compares a fixed voltage reference to a portion of the output voltage to set a control voltage for the FET gate. Output voltage is set with an offset voltage referenced to circuit ground and can be generated with a single resistor to circuit ground by a current through the resistor which is set from VREF and the regulated output voltage. Output current is limited with a second depletion mode FET that senses the difference in regulator output voltage and voltage at said first FET transistor drain. All circuitry except the output transistor and 2 FET drivers are bootstrap powered from the regulated output voltage to isolate almost all circuit elements from noise present on the input power source.





(PRIOR ART)
FIGURE 1



(PRIOR ART)
FIGURE 2

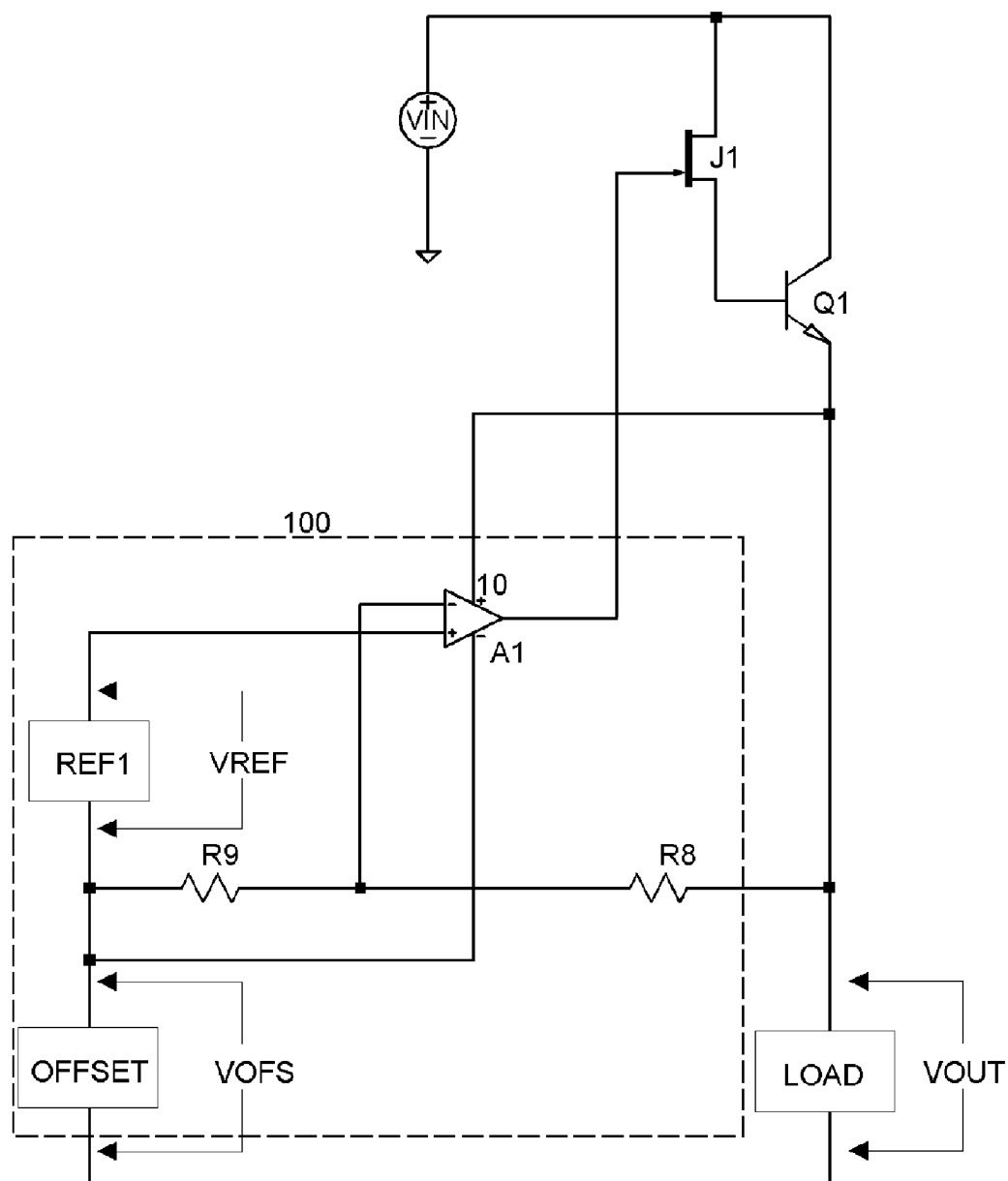


FIGURE 3

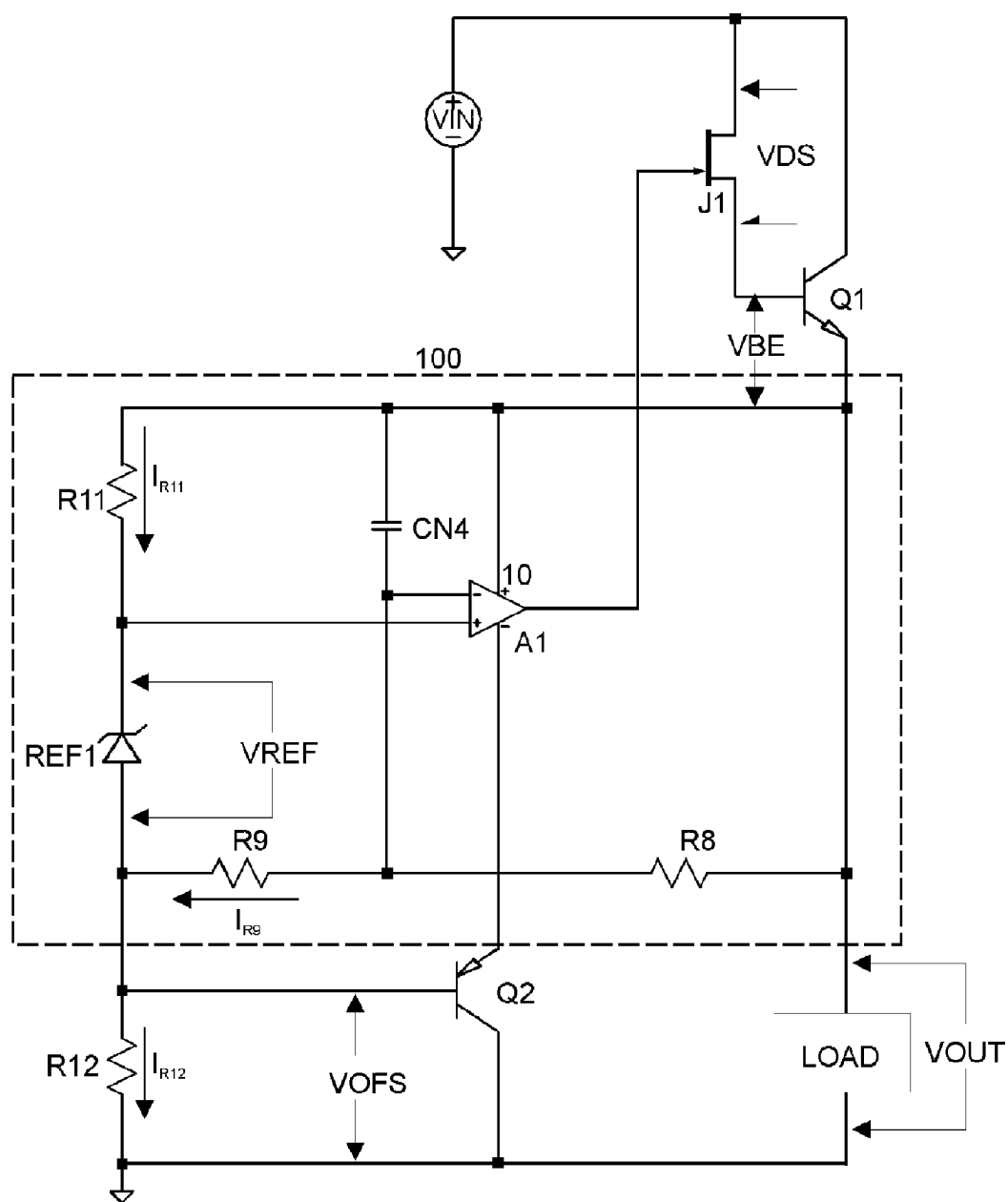


FIGURE 4

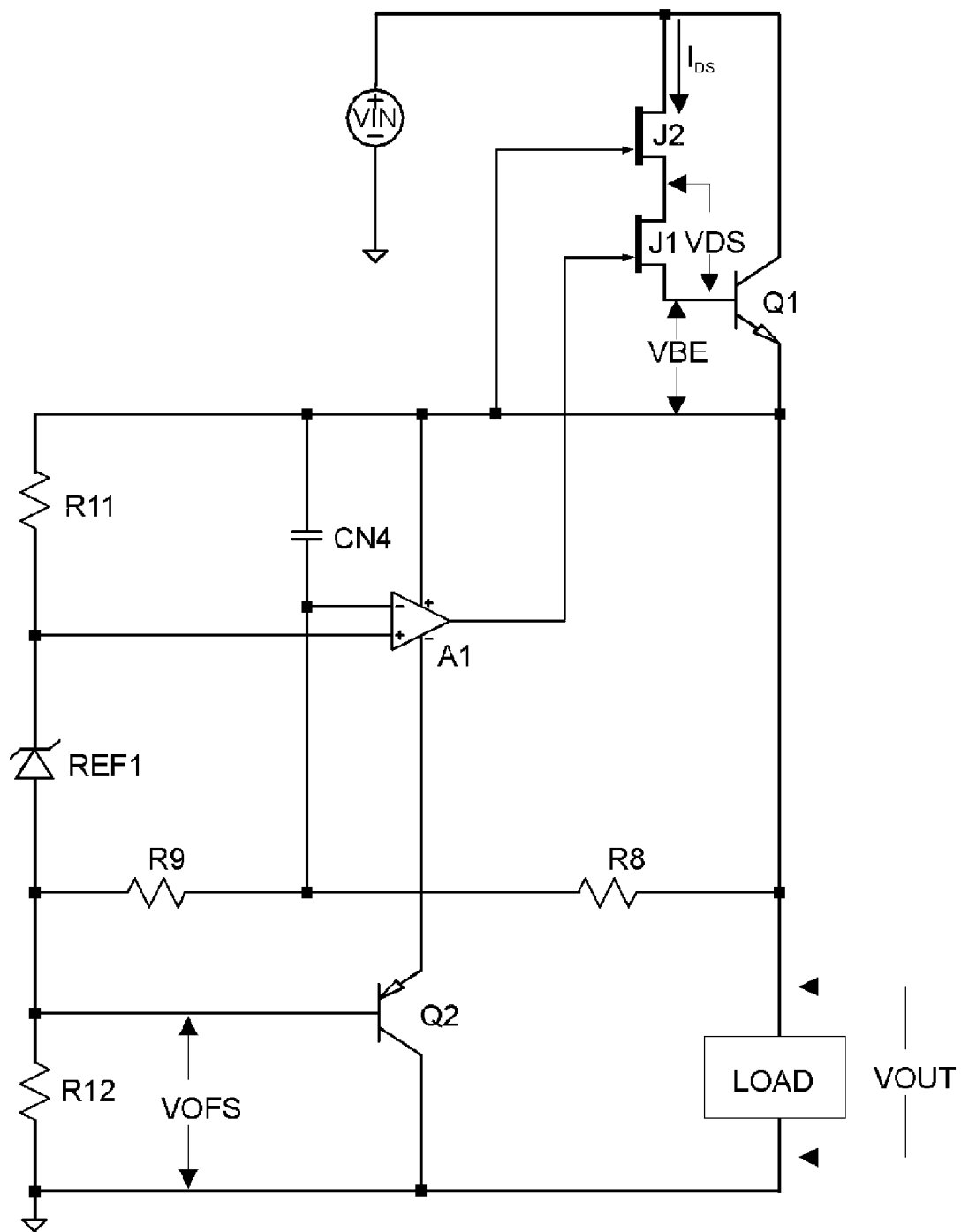


FIGURE 5

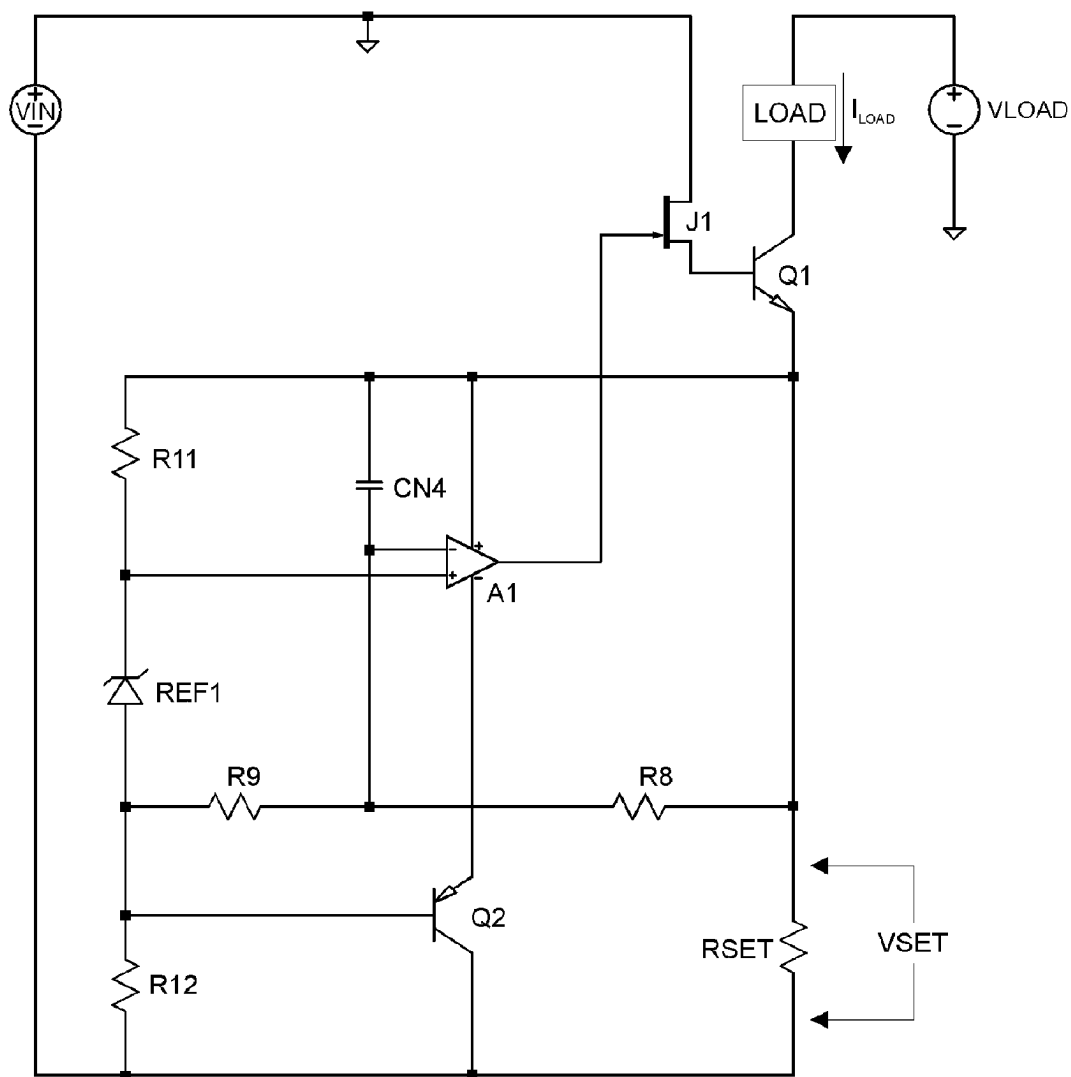


FIGURE 7

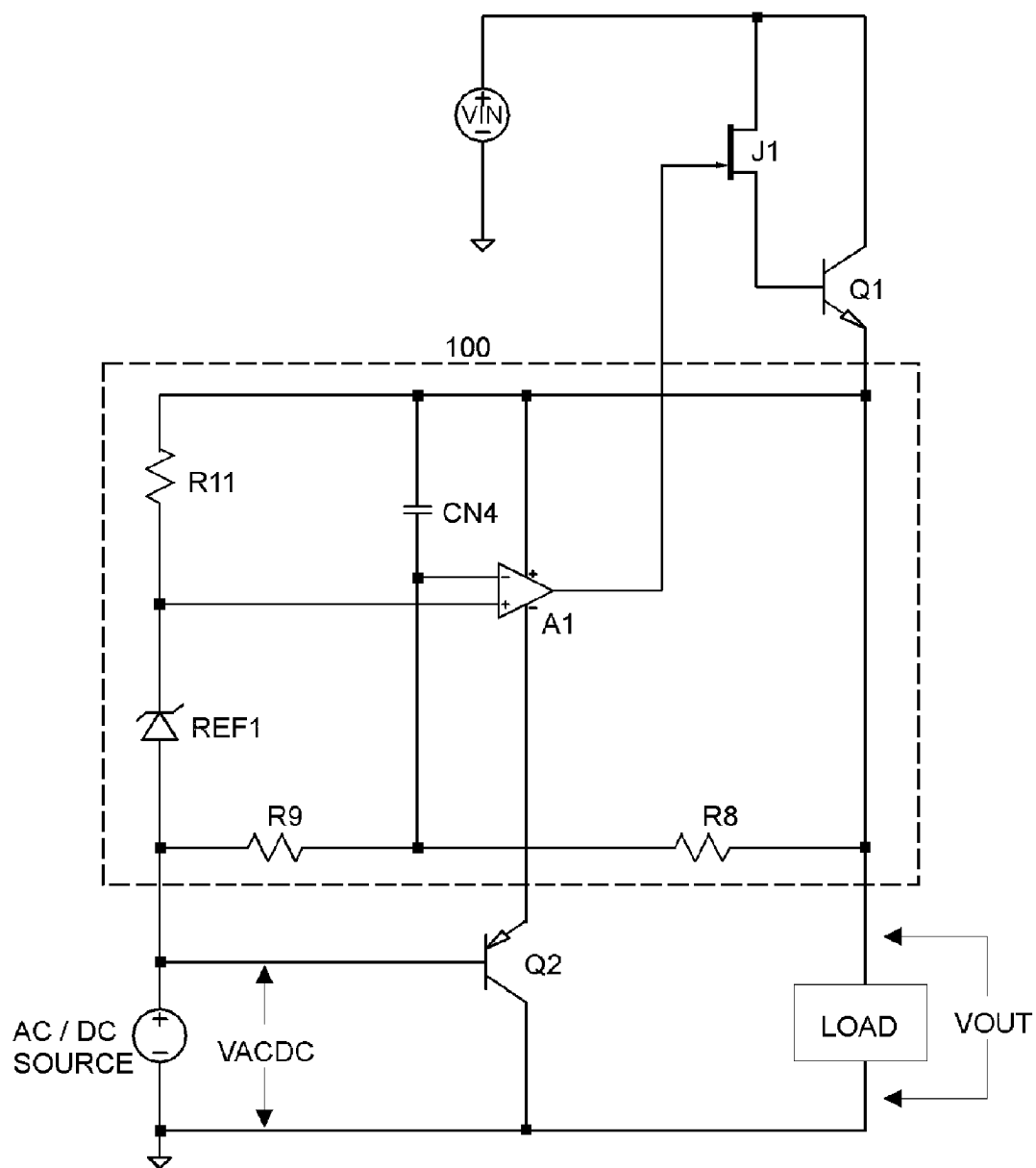


FIGURE 8

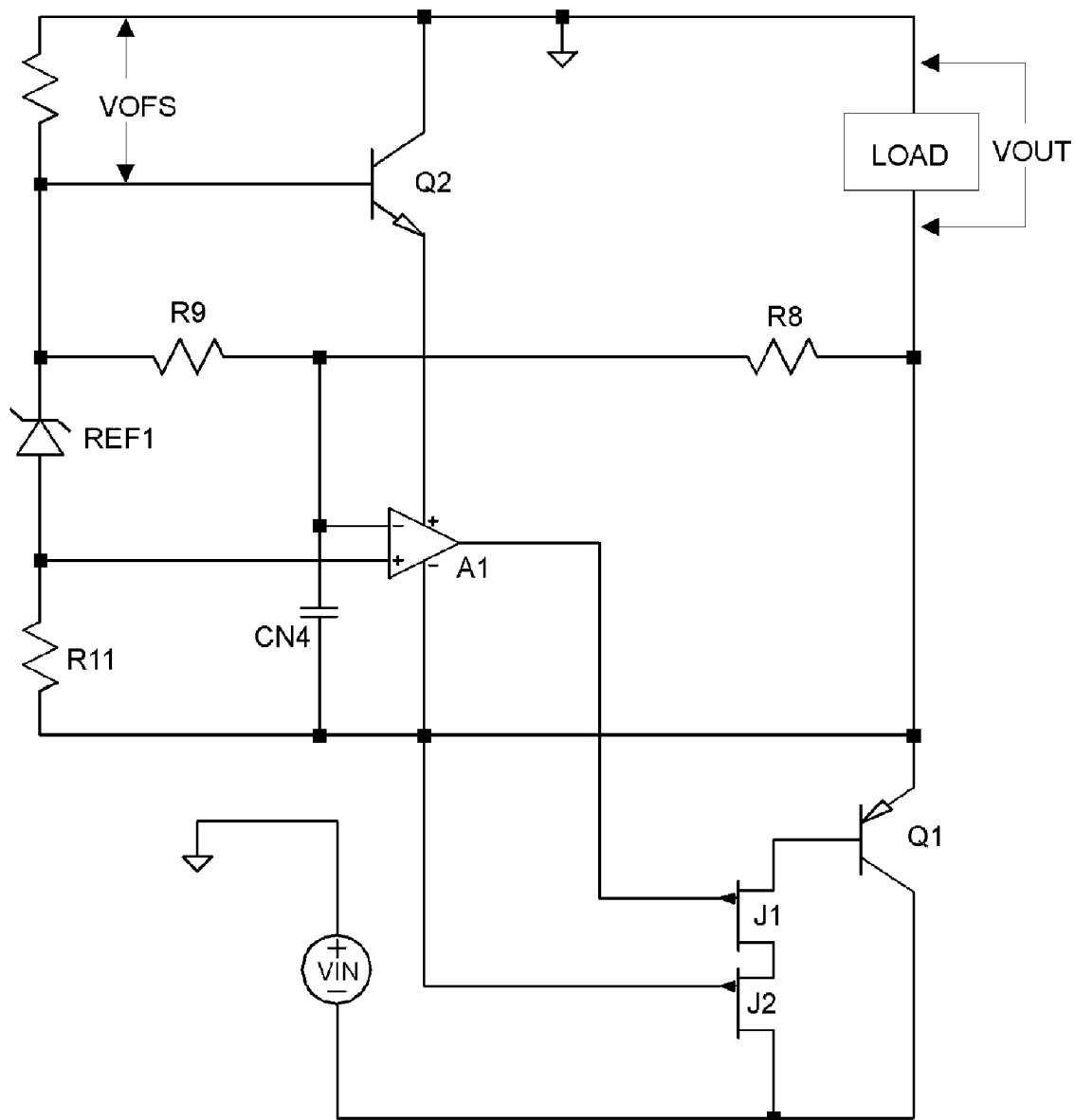


FIGURE 9