NO. 27.5 AC-8.5 THEORY OF OPERATION

The AC-8.5 PC Assembly contains buffer and voltage gain circuitry for the No. 27.5 Power Amplifier. Regulated DC Supplies and current gain circuitry are located on the AC-8 PC Assembly and interconnected via gold pins.

BUFFER STAGE ONE

The buffer input stage consists of a bipolar cascoded differential amplifier with passive collector loading and constant current source and sink for DC biasing. Q50, Q52 and R62 comprise a current sink for total first stage current of 2.4 mA. 800 μA is available to each half of Q64, a supermatch pair configured as a differential common emitter amplifier. The remaining 800 μA is sourced by Q62, Q63 and R55 for biasing of cascoded common base amplifiers Q51 and Q53 by CR68, CR69 and R61.

BUFFER STAGE TWO

The second buffer stage is comprised of a differential input amplifier, Q55 and Q59, with current mirror Q56 and Q58, for conversion to single-ended output. Half of the differential amplifier is cascoded by Q57 for isolation from driveline voltage swings. Passive DC biasing is accomplished by R75, R76 and R77. Approximately 9 mA is available to each side of the differential amplifier, with 1 mA bias through R76 and R77 to set DC bias of Q57's base.

BUFFER OUTPUT STAGE

The buffer output stage is comprised of a complimentary emitter follower configuration of Q60 and Q61, whose emitter currents are set at approximately 12 mA by bias elements CR62, CR63 and R80.

VOLTAGE GAIN STAGE ONE

The voltage gain input stage consists of a bipolar cascoded differential amplifier with passive collector loading and constant current source and sink for DC biasing. Q2, Q3, R13 and R14 comprise a current sink for total first stage current of 3.2 mA. 800 μA is available to each half of Q19, a supermatch pair configured as a differential common emitter amplifier. The remaining 1.6mA is sourced by Q4, Q5, R12 and R38 for biasing of cascoded common base amplifier Q1 by CR1, CR2 and R10, and Q6 by CR3, CR4 and R16.

VOLTAGE GAIN STAGE TWO

The second voltage gain stage is comprised of a differential common emitter amplifier Q9 and Q18, cascoded common base amplifiers Q10 and Q15, with current mirror Q11 and Q17, for conversion to single-ended output. Current mirror element Q17 is cascoded with Q16 as are their circuit complements, Q18 with Q15, for isolation from driveline voltage swing. Q13 provides bias for Q16 and, in conjunction with CR27 and CR28, for Q11 and Q17. CR19 provides a constant current load for Q13 to ensure that it never turns off.

Second stage current source Q12, Q14 and R29 provides 57.5mA, approximately 24mA to each side of the differential amplifier, and the remaining 10 mA through cascode bias chains CR13-CR18 and CR20-CR25 and current sink Q7, Q8 and R24.

NO. 27.5 AC-8 THEORY OF OPERATION

REGULATOR

Voltage gain stages are powered by regulated + and - 65V supplies. DC rectification is performed by a discrete full-wave bridge located on the VB-5 PC board. Two 1900 μF capacitors clamped to the chassis provide filtering before the unregulated voltages are brought to the channel's two separate, non-tracking regulators. Since the regulators are complimentary but identical in operation, only the positive regulator will be described in detail.

A reference voltage is set by 36V Zener diode CR206, and filtered by R207, C201 and C203. Zener current is available on power-up through R229 and CR211; as regulated output stabilizes, CR211 is reversed biased, CR203 becomes forward biased, and CR204 provides a regulated current for Zener operation. A differential amplifier comprised of Q201 and Q203 compares Zener reference to a portion of regulator output. Regulator gain {1 + (R225 + R215a)/(R215b + R219)} can be adjusted by varying R215. Voltage gain is provided by common emitter amplifier Q205, and current gain by emitter followers Q207 and Q209 for the required +65V, 132mA output.

ANTI-THUMP

During turn-on and turn-off, transients are minimized by clamping amplifier drive lines to ground. Clamping, comparator and timing circuitry is located on the AC-8 PC assembly.

1. COMPARATOR

Comparator Q213 monitors -VReg and develops the appropriate voltage across its collector load resistor, R240, to control clamping action. With Q213's base held to -12V by CR220, CR222 in Zener breakdown at 47V, and voltage across R244 setting emitter current, Q213 remains in saturation during normal amplifier operation. If -VReg falls below the Zener threshold of CR220 + CR222, emitter current through R244 ceases and voltage across R240 falls to zero.

Q214, an N-Channel J-FET, is switched by Q213 to control the voltage at the junction of R239 and R241. During normal operation, Q214's gate voltage is held at -12V, well below specified gate-source cutoff voltage. Drain current at this time is virtually zero. Diode CR219 is in Zener breakdown and voltage at the junction of R238 and R239 is approximately 12V. When Q213 is not conducting (at turn-on or after turn-off), Q214's gate voltage fall to 0V, Q214 saturates, and the junction of R238 and R239 is brought to ground.

2. TIMING

C213 will always charge to the voltage at the junction of R239 and R241. When Q214 is in cutoff (after turn-on and during normal amplifier operation), C213 charges slowly through R239, R241 and R242 to +12V. When Q214 saturates (at turn-on or after turn-off), C213 discharges quickly through CR223, R241 and the drain of Q214 to ground. Charge on C213 is applied to the gate of MOSFET Q216.

3. CLAMPING

Amplifier drive lines are clamped to ground during power-up and power-down by saturated bipolar transistors Q215 and Q217 and their associated steering diodes CR224 and CR225. Saturation of these transistors is controlled by Q216. When the charge on C213 is near 0V, Q216, an enhancement-mode device, does not conduct, and bases of Q215 and Q217 are biased heavily through R245 and R246. As C213 charges toward +12V, Q216 conducts heavily, shorting the bases of Q215 and Q217 together and diverting base current through its channel. With Q215 and Q217 now off, collector-diode junctions are pulled to power supply rails to prevent interference with drivelines during normal operation.

SOFT CLIP

Voltage limiting of drive lines is performed by Q115 and Q116. Base voltages for these devices are established by the resistor divider network of R131-R130-R132. Emitter current for Q115 and Q116 is set by R133 and R134. As unregulated rails sag due to current demands of the load, these voltages will adjust accordingly. When drive lines exceed these predetermined voltages, CR101, CR102 and CR103 or CR104, CR105 and CR106 will begin to conduct. Multiple breakpoints set by these diodes shape the limited drivelines before hard saturation of second stage, drivers or outputs can occur. Harsh diode turn-on characteristics are softened by parallel resistors R137, R139, R138 and R140. Soft clip circuitry is the primary limiting circuit when driving loads as low as two ohms.