

## Bipolar Mode Static Induction Transistor\*

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Junction gate static induction transistor (JSIT) is designed as normally-off device, where the channel is completely pinched-off by the gate to channel built-in voltage, thus establishing a potential barrier in the channel. An application of forward gate bias voltage lowers the potential barrier and allows the drain current to flow. This normally-off JSIT is called bipolar mode SIT (BSIT). Basic characteristics of BSIT is similar to that of bipolar transistor. BSIT is characterized by low impedance, high current gain, high transconductance and high current density, so that BSIT is promising for high current, high speed and high efficiency switching devices as well as low voltage and low energy integrated circuits.

Basic operational principle of BSIT is described by feedback theory with a consideration to the virtual base resistance.

### §1. Introduction

Junction gate SIT (JSIT)<sup>1-3)</sup> is easily designed as normally-off device, where the channel is completely pinched-off by the gate to channel built-in voltage, thus establishing a potential barrier in the channel. An application of forward gate bias voltage lowers the potential barrier and allows the drain current to flow. Normally-off JSIT is called bipolar mode SIT (BSIT). BSIT has been first applied to the  $I^2L$  equivalent static induction transistor logic circuit (SITI<sup>2</sup>L),<sup>4-6)</sup> which has shown experimentally excellent low energy operation.

BSIT exhibits the saturating current-voltage characteristic, while conventional SIT exhibits the non-saturating characteristic.<sup>4-7)</sup> BSIT is characterized by high current gain, high transconductance, high current density and low drain voltage for the onset of current saturation, i.e., low impedance.<sup>7)</sup> Operational principle of BSIT is described here, especially concentrating on low impedance characteristic. An application of BSIT to high current switching device is discussed in this paper.

BSIT is very promising to high current, high speed and high efficiency switching devices as well as low voltage and low energy integrated circuits.

### §2. Basic Operation of BSIT

Brief design theory of BSIT using two-dimensional rectangular channel structure has already been described analytically in the previous papers.<sup>6-8)</sup> It is natural to require that the gate to gate spacing and the impurity concentration must be designed in BSIT to realize the complete pinch-off of the channel due to the gate to channel built-in voltage. Moreover, the rate of the channel length to the gate to gate spacing is required larger than 0.7 in order to establish a potential barrier in the channel even when a certain drain voltage is applied. This rate must be increased to increase this blocking drain voltage.<sup>8)</sup>

The potential profile in the source to drain direction along the center of the channel is shown for three different channel length in Fig. 1, where the bias conditions are as follows,  $V_g = 0.125V_{bi}$  and  $V_d = 0.875V_{bi}$  which are representative bias conditions in the integrated circuit application. Here,  $l_n$  and  $N_{Dn}$  are normalized quantities, such as  $l_n = l/W$  and  $N_{Dn} = N_D q W^2 / \epsilon V_{bi}$ , where  $l$ ,  $W$ ,  $N_D$ ,  $V_{bi}$ ,  $q$  and  $\epsilon$  are the channel length, the gate to gate spacing, the impurity concentration in the channel, the gate to channel built-in voltage, unit charge and dielectric constant, respectively.

The potential barrier height decreases with decreasing the channel length. This comes from the fact that the drain and the source voltage

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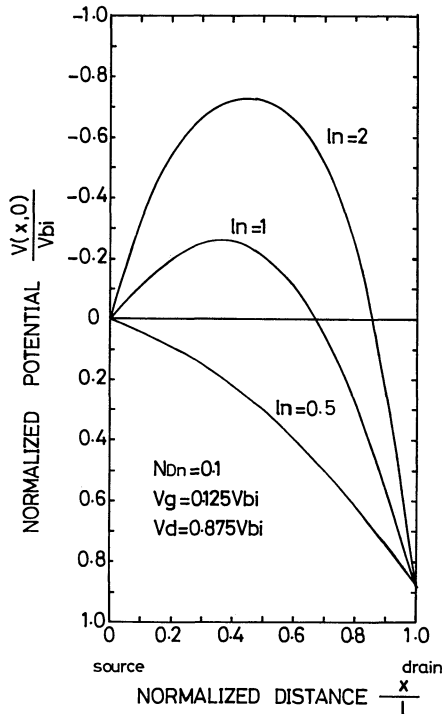


Fig. 1. Potential profile in the source to drain direction along the channel center where  $V_g=0.125 V_{bi}$ ,  $V_d=0.875 V_{bi}$  and  $N_{Dn}=0.1$ .

strongly control the potential profile in the channel in the sample having a short normalized channel length instead of gate potential. There does not appear the potential barrier in the channel in the sample having the normalized channel length of  $l_n=0.5$  even if the normalized impurity concentration is decreased less than 0.1. The potential barrier height naturally decreases with increasing the drain voltage and the impurity concentration in the channel.

Variations of operation in JSIT from normally-on characteristic to normally-off have been confirmed experimentally by fabricating surface gate structure n-channel JSIT having six different gate to gate spacings. These samples have 10 channels comprising of source length of  $200 \mu\text{m}$ , gate diffusion depth of  $2.6 \mu\text{m}$ , impurity concentration of  $3.6 \times 10^{13} \text{ cm}^{-3}$  and epilayer thickness of  $4.7 \mu\text{m}$  as shown in Fig. 3 in the ref. (7). The gate mask spacing is changed by one micron step from  $5 \mu\text{m}$  (ST4) to  $10 \mu\text{m}$  (ST9). Figure 2 illustrates the relationship of drain current  $I_d$  to gate voltage  $V_g$  for these samples, where the drain

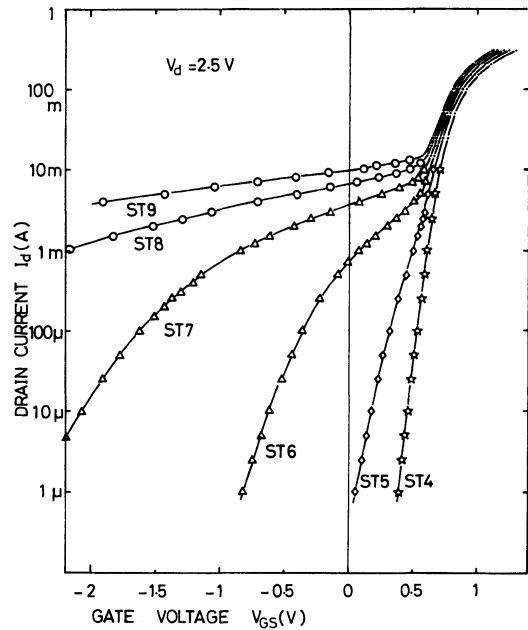


Fig. 2. Drain current vs. gate voltage in JSITs having six different gate spacing, where  $V_d=2.5 \text{ V}$ .

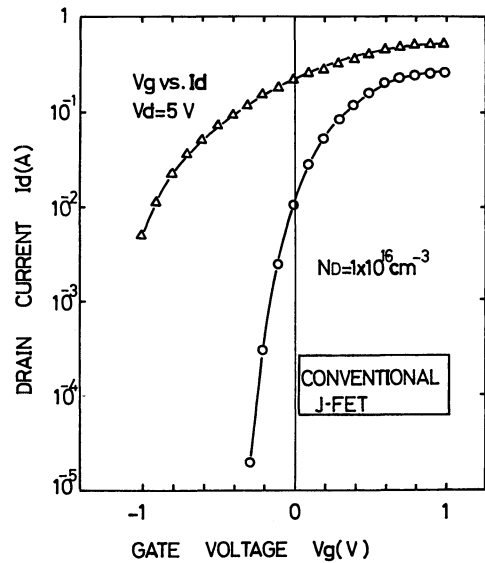


Fig. 3. Drain current vs. gate voltage in the conventional JFET, where  $V_d=5 \text{ V}$ .

voltage  $V_d$  is kept at  $2.5 \text{ V}$ . It is seen from Fig. 2 that samples of ST4 and ST5 are normally-off devices while samples of ST6 . . . and ST9 are normally-on devices. Even in normally-on JSIT, the drain currents start to increase rapidly with increasing forward gate bias voltages higher than about  $0.5 \text{ V}$ . Even in high forward gate bias voltages, on the contrary,

there does not appear the rapid increase of drain current in the conventional JFET having a long channel structure, as shown in Fig. 3. This difference stems from the fact that the highly doped source region exists quite near the intrinsic gate in BSIT in order to increase the injection efficiency of majority carriers from the source region to the channel while the situation is completely different in the conventional FET. In high forward gate bias voltages, the drain current is not so strictly sensitive to the channel dimension in BSIT. SIT is an injection device where majority carriers are directly injected into the channel from the highly doped source region, thus accompanying a rapid increase of drain current for high forward gate bias voltages. Characteristic of this rapid increase enables the current density of BSIT to become comparable to or larger than that of bipolar transistor, although the impurity concentration of the channel is very low in BSIT, such as  $10^{13} \sim 10^{14} \text{ cm}^{-3}$ .

BSIT exhibits the saturating current-voltage characteristics as shown in Fig. 4, where the sample has 5 channels comprising of source length of  $30 \mu\text{m}$  and gate to gate spacing of

$5 \mu\text{m}$  at mask level, gate diffusion depth of  $2.0 \mu\text{m}$ , impurity concentration of  $4.5 \times 10^{13} \text{ cm}^{-3}$  and epi-layer thickness of  $2.6 \mu\text{m}$ . In the current saturation region, the drain current increases with the increase of gate bias voltage, almost following the equation such as  $I_d \propto \exp(qV_g/KT)$  as shown in Fig. 5. In the low drain voltages, the I-V characteristic of BSIT seems complicate. This complicate behavior stems from the minority carrier injection from the gate region to the channel. In high forward gate bias voltages, the gate to drain junction is biased in a forward direction when the drain voltage is kept lower than the gate bias voltage. It is seen from Fig. 4 that the drain voltage for the onset of current saturation is less than  $0.1 \text{ V}$  and the drain current increases drastically by 4 or 5 orders of magnitude with an increase of drain voltages of  $1$  or  $2 \text{ mV}$  at the threshold voltage. The current density is easily up to several thousand  $\text{A/cm}^2$  even in the low drain voltages such as  $0.1 \text{ V}$ , leading to low impedance characteristic. Figure 5 indicates that BSIT exhibits high transconductance.

The drastic increase of drain current in

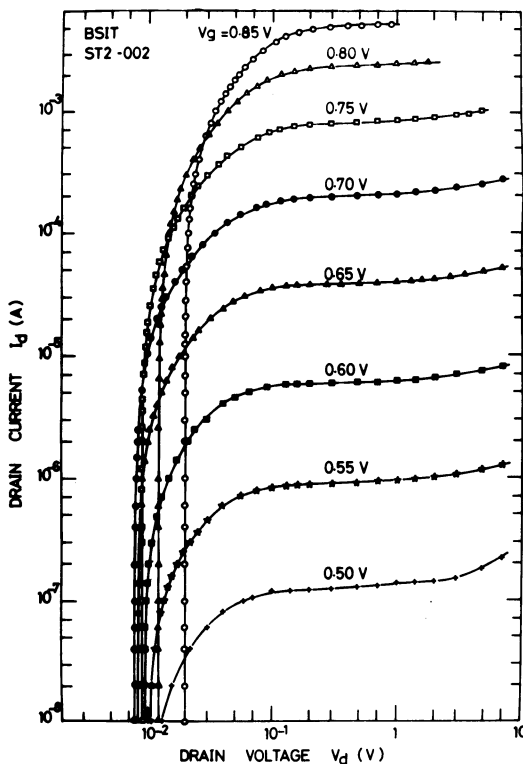


Fig. 4. Drain current vs. drain voltage in BSIT.

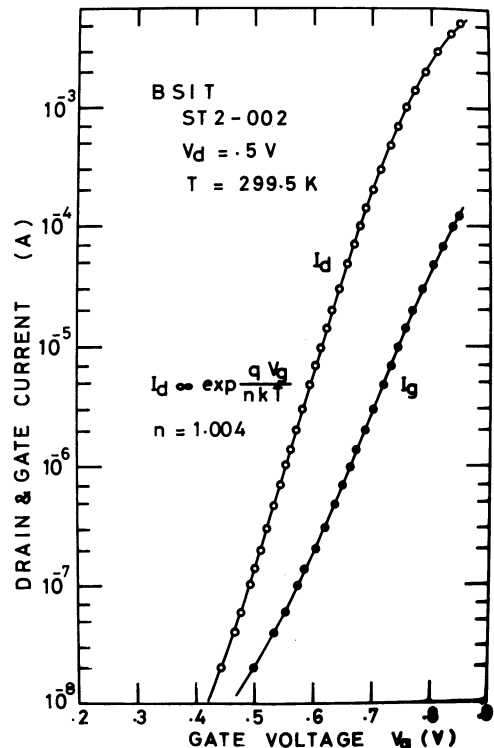


Fig. 5. Drain current vs. gate voltage in BSIT, where gate current is plotted for gate voltage.

BSIT at the threshold voltage can be explained by the feedback effect due to the virtual base resistance  $r_{vb}$  existing between the gate and the channel, as shown in Fig. 6. Most of electrons injected from the source region to the channel flow into the gate region in the low drain voltages, thus forming a part of gate current. The gate current causes a voltage drop across the virtual base resistance, so that there remains potential barrier at the center of the channel as illustrated by dashed line in Fig. 7 even if high gate bias voltage is applied in the forward direction. In this situation, if the drain voltage is increased over a certain value, injected electrons can cross over this potential barrier and flow into the drain. The decrease of the amount of electrons flowing into the gate region decreases the gate current accompanying the decrease of the potential barrier, which enhances the increase of the amount of electrons crossing the potential barrier and flowing into the drain region. Thus, the negative feedback effect due to the virtual base resistance disappears accompanying the drastic increase of

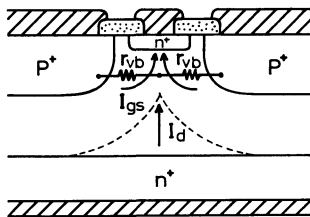


Fig. 6. Negative feedback mechanism due to the virtual base resistance  $r_{vb}$ .

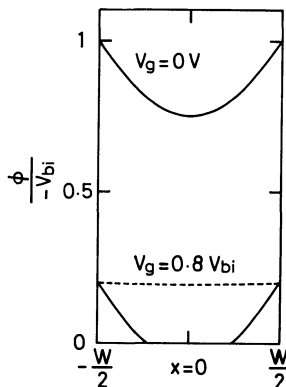


Fig. 7. Variation of potential profile in the cross-sectional direction of the channel due to an application of gate bias voltage and the negative feedback effect. Dashed line: potential profile due to the negative feedback effect of  $r_{vb}$ .

drain current, where the potential profile is approximately expressed by the solid line in Fig. 7.

### §3. Switching Performance

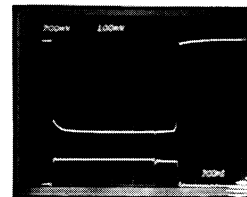
It has been demonstrated experimentally that the drain voltage for the onset of current saturation is very small in BSIT. The source current density in BSIT is easily increased up to  $10^4$  A/cm<sup>2</sup> in case the gate voltage is set around at 0.8 V. Moreover, BSIT has high transconductance. BSIT can be estimated, therefore, to exhibit high speed and high efficiency switching performance. Low energy application of BSIT in integrated circuits is described elsewhere,<sup>4-6,9)</sup> so that high current and high speed switching performance of BSIT is discussed in this paper.

BSIT having 790 channels has been fabricated, where the channel structure is as follows:

#### BSIT Switching Waveforms

$$R_L = 1 \Omega \quad V_b = 21.0 \text{ V}$$

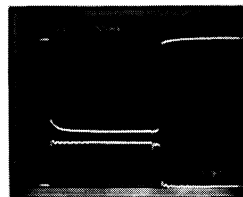
$$V_d : 4.55 \text{ V/div} \quad \text{Hor} : 200 \text{ nsec/div}$$



(a)

$$V_{gdc} = 0 \text{ V} : 0.9 \text{ V/div}$$

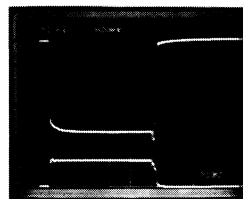
$$T_{off} = 220 \text{ nsec}$$



(b)

$$V_{gdc} = -3.0 \text{ V} : 1.8 \text{ V/div}$$

$$T_{off} = 90 \text{ nsec}$$



(c)

$$V_{gdc} = -5.0 \text{ V} : 4.5 \text{ V/div}$$

$$T_{off} = 50 \text{ nsec}$$

Fig. 8. Switching waveforms of drain voltage (upper trace: vertical scale 4.55 V/div) and gate voltage (lower trace), where the horizontal scale is 200 nsec/div.  $V_{gdc}$  and vertical scale of lower trace are (0 V, 0.9 V/div) (a), (-3 V, 1.8 V/div) (b) and (-5 V, 4.5 V/div) (c), respectively.

source length of 30  $\mu\text{m}$ , gate spacing at mask level of 6  $\mu\text{m}$ , gate diffusion depth of 2.6  $\mu\text{m}$ , impurity concentration of  $2.7 \times 10^{13} \text{ cm}^{-3}$  and epi-layer thickness of 6.8  $\mu\text{m}$ . Cell size is  $800 \times 520 \mu\text{m}^2$ . Three chips are mounted in a high frequency package.

Switching waveforms of drain voltage and gate voltage of this sample has been observed and displayed on an oscilloscope as shown in Fig. 8, where the load resistance is 1  $\Omega$  and switching occurs between two states of (20 A, 0.6 V) and (0 A, 21 V). The dc gate bias voltage  $V_{\text{gdc}}$  is kept at 0 V in Fig. 11(a), -3 V in Fig. 11(b) and -5 V in Fig. 11(c). Vertical scale in drain voltage is 4.55 V/div and horizontal scale is 200 nsec/div. Vertical scale of gate voltage is 0.9 V/div in (a), 1.8 V/div in (b) and 4.5 V/div, respectively. In BSIT, the turn off time is liable to become long due to the storage effect of minority carriers in the channel injected from the gate region when the gate bias voltage is higher than 0.9 V in forward direction. The turn off time  $T_{\text{off}}$  is 220 nsec, 90 nsec and 50 nsec for  $V_{\text{gdc}} = 0 \text{ V}$ , -3 V and -5 V, respectively. The turn off time is dominantly determined by the minority carrier storage effect in high forward gate bias voltages. Therefore, the increase of dc reverse gate bias voltage decreases the turn off time. The decrease of drain current rapidly decreases the turn off time, because the minority carrier storage effect has been proved experimentally negligibly small in the forward gate bias voltages less than 0.8~0.85 V. The forward voltage drop is about 0.6 V for the drain current of 20 A. It seems rather large for high efficiency switching performance. This somewhat large voltage drop comes from the extremely high current density, because the value of 20 A corresponds to the source current density of  $2.5\text{--}3 \times 10^4 \text{ A/cm}^2$ .

The turn off time of 30 A switching is 440 nsec, 170 nsec and 110 nsec for  $V_{\text{gdc}} = 0 \text{ V}$ , -3 V and -6 V, respectively, where the voltage drop is about 0.8 V.

It can be concluded from these results that BSIT exhibits excellent performances in high current, high speed and high efficiency switching operation if the current density is set at moderate level, i.e., the forward gate bias voltage is set less than about 0.85 V.

## §4. Conclusion

Operational principle and characteristic of BSIT has been discussed concentrating on low impedance, low saturation drain voltage, high current density and high transconductance. These basic properties of BSIT have been described to originate from the feedback effect due to the virtual base resistance existing between the gate and the channel. In BSIT, the saturation drain voltage is lower than that of bipolar transistor. Moreover, the current density and the transconductance in BSIT can be designed to be higher than that of a bipolar transistor in spite of its low impurity concentration in the channel as low as  $10^{13} \sim 10^{14} \text{ cm}^{-3}$ . High current, high speed and high efficiency switching in BSIT has been demonstrated experimentally by using the surface gate structure BSIT.

BSIT can be concluded as very promising to high current, high speed and high efficiency switching device as well as low voltage and low energy integrated circuits.

GaAs BSIT is even more promising especially to integrated circuit application, where two remarkable properties of GaAs such as high electron mobility and direct band structure increase the current density and decrease the minority carrier storage effect, thus increasing the driving capability and decreasing the switching time drastically.

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