

diodes  $D_1$  and  $D_2$  and adding one resistor, but the advantages gained from this are negligible.

**Circuit description**

The function of  $Tr_1$ ,  $Tr_2$ , and  $Tr_3$  is to convert an error voltage—the difference between the input and feedback voltage—into a proportional output current. Now to produce the required mutual conductance of this stage (1A/V) without sacrificing either noise performance or linearity, the design in Fig. 1 was used. Starting at the input transistor  $Tr_1$ , this p-n-p type is used mainly as a level shifter. If we assume that the

current gain of  $Tr_2$  was extremely large (> 500), then this input stage would have a maximum voltage gain of about five—not very much! If voltage gain was increased to the theoretical maximum of 30 (by decreasing the value of  $R_2$  and  $R_3$ ) problems would arise with the voltage offset at the speaker output due to increased emitter current flowing through  $R_1$ , and base current flowing through  $R_1$ .

Assuming for the moment that this first stage gain is a reasonable compromise, it now becomes obvious that the noise and distortion performance is dictated by the next stage. This stage ( $Tr_2, R_8$ ) is a straightforward class A amplifier with very high

gain (typically 400) and low distortion due to the limited modulation index of the collector current (0.04 max). The peak 2nd harmonic voltage generated is about  $10\mu V$  and, assuming this is referred to the input of the first stage, it represents less than 0.001% 2nd harmonic distortion with feedback. Thus this second stage is the work horse of the input section, the third device  $Tr_3$  being used both as a buffer to reduce the loading of  $R_{10}$  on  $R_8$ , and to convert the voltage changes across  $R_8$  into an output current to drive the emitters of the signal splitter.

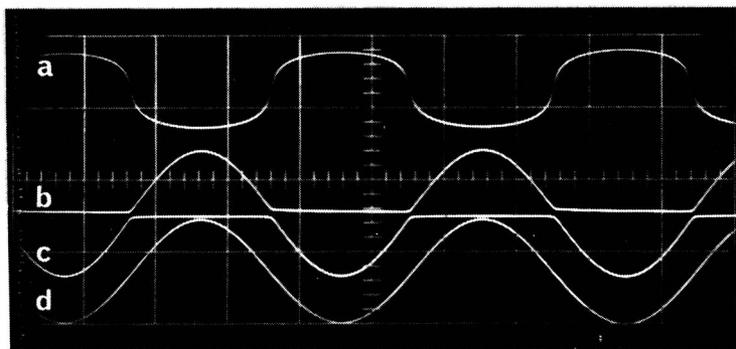
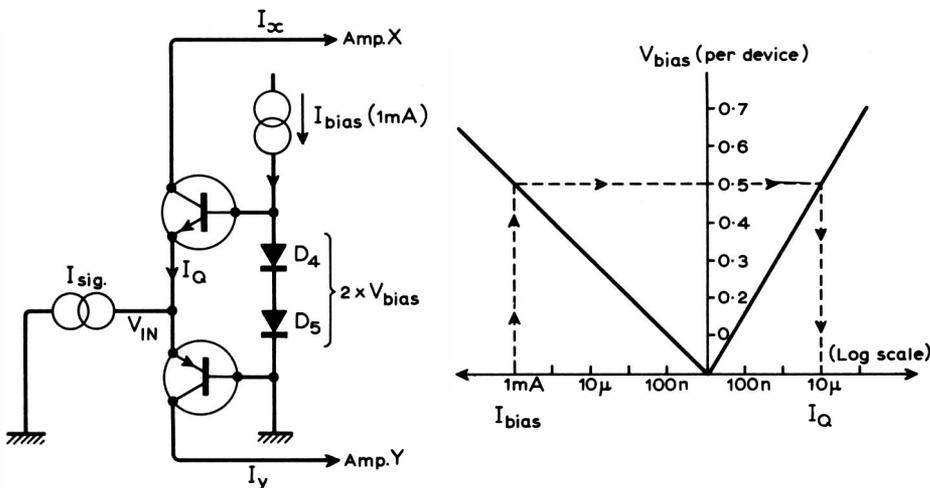
Resistor  $R_{10}$  performs two functions in this last stage of the input section. It defines the conversion constant  $Engmen$  for the stage, and it governs the maximum current which can be driven out of the collector of  $Tr_3$ . (This maximum current is defined by using the conducting voltages of  $D_3$  and  $Tr_2$  and the value of  $R_{10}$ .) Therefore this input section seems to have excellent performance during normal operation, but what can happen during an overload?

If the input transient was negative all would be well due to  $Tr_2$  entering saturation. But if the transient was positive  $Tr_1$  would turn off completely, the potential across  $R_{10}$  rising toward that at the end of  $R_8$ . ( $Tr_2$  would also be completely cut off.) This would cause excess currents to flow in  $Tr_3$ , upsetting the bias chain  $R_7, D_4, D_5, R_8$ . After the excessive input signal is removed some time would elapse before recovery would take place, hence diode  $D_3$  clamps the voltage and maintains  $Tr_2$  in full conduction to reduce recovery time and improve amplifier stability.

While discussing the problem of recovery from overload, the charge across the compensation capacitor  $C_4$  has also to be taken into account. The time for the accumulated charge to decay is a function of the amount of charge and the rate of decay. If the rate of decay is constant, the only way to reduce the recovery time is to limit the accumulated charge (in terms of voltage). Diode  $D_3$  performs this function as well as clamping the voltage across  $R_{10}$  at 1V thus limiting drive current into the signal splitter.

The second section is the signal splitter, unique to this approach, and consists of transistors  $Tr_4$  and  $Tr_5$  plus a current source transistor  $Tr_6$ . The signal current into the emitter of  $Tr_4$  or  $Tr_5$  is derived by subtraction of two current levels, one constant and set by the voltage across  $R_9$ , and the other the output current of the input section. This signal current either appears at the collector of  $Tr_5$ —causing a voltage change across  $R_{20}$ —or at the collector of  $Tr_4$ —causing a voltage change across  $R_{21}$ . These voltage changes are converted into positive and negative output currents in the output section, which are then added together to give the final waveform. The current gain of the output sections which are conventional triples are governed by the ratio of  $R_{20}$  to  $R_{17}$ , and  $R_{21}$  to  $R_{18}$ , and in this case the gain of 1000 seemed reasonable.

To keep the output triples above the minimum conduction level a bias current is provided by  $R_{11}$ . The procedure adopted for setting the standing current is to first set  $R_{20}$  and  $R_{21}$  to minimum (diode end).



- Curve a - Emitter voltage 200mV/cm
- b -  $I_y$  collector current 1mA/cm
- c - Collector current 1mA/cm
- d -  $I_{sig}$  1mA/cm

Vertical and horizontal scales = 0.2 millisecc/cm Frequency = 1kHz

Fig. 2. Input amplifier converts signal voltage to a proportional current to feed transistor signal splitter. Bias diodes reduce voltage excursion from 1.2V to 300mV pk-pk. Bottom trace is current signal input to splitter.

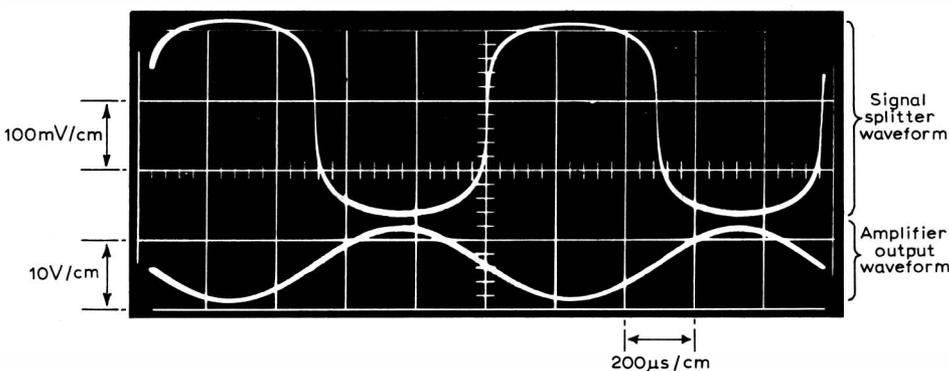


Fig. 3. Voltage excursion at signal splitter input with corresponding sinusoidal amplifier output current ( $R_L = 15\Omega$ ).