

# New Approach to Class B Amplifier Design

by Peter Blomley\*

(Concluded from February issue)

This article describes a 30-watt amplifier design which embodies the author's approach to class B design, outlined last issue. Although further work on this approach is still needed, the design illustrates the kind of problems involved. The author also discusses the application of integrated components in future designs.

The general design of a complete amplifier using the new approach is relatively conventional except for the inclusion of the signal splitter (described last month). In principle, the design of each half of the output stage is made simpler as there is no cut-off, hence

removing the necessity for predicting the performance in the cross-over region.

Examination of the circuit (Fig. 1) shows that the amplifier consists of three sections, the input amplifier, signal splitter and output amplifier.

**Input amplifier.** This converts the input voltage into a proportional output current

which drives the signal splitter. To enhance the performance of the amplifier as a whole, this section should have a reasonable mutual conductance (1A/V) and good linearity (1%). The latter does not represent a serious problem as the input amplifier is a low-level class A amplifier, but care is needed to control the maximum value of  $g_m$  otherwise frequency compensation problems arise.

**Signal splitter.** As many fundamental details of the signal splitter were described last month, further details are confined to the biasing system. If perfect bipolar devices were available and ideal current sources existed, voltage bias across the emitter-base junction would not be needed, but such situations do not exist and distortions due to conditions falling short of the ideal can be rendered negligible by employing simple bias diodes (Fig. 2). This reduces the voltage excursion at the input to the signal splitter from 1.2V to 300mV pk-pk. The waveform with a sinusoidal output current is shown in Fig. 3.

**Output stages.** This now is one of the easiest to design. As long as the gain remains constant throughout the output cycle all is well. In the initial version, used to evaluate system performance, a compromise was reached between complexity, performance and cost. Thus individual adjustment potentiometers were used instead of the matched devices.

The output sub-amplifiers are similar to the Quad triples, these giving excellent linearity down to very low output currents, coupled with outstanding thermal stability. To compensate for the effect of ambient temperature changes on the quiescent current of the amplifier, diodes  $D_1$  and  $D_2$  cancel  $V_{BE}$  changes in transistors  $Tr_7$  and  $Tr_8$ . It may have occurred to the reader that diodes in the forward path of the amplifier loop could generate appreciable distortion. However, in practice the maximum change in current is about 4:1 and thus almost corresponds to the change in collector current of transistors  $Tr_7$  and  $Tr_8$ . In this way the change in voltage drop across the transistors compensates for the change in the diodes. Even if this did not occur, the resultant gain change for the output sub-amplifier is less than 4% for  $I_{out}$  values between 0 and 2A. The problem can be alleviated by increasing the current into

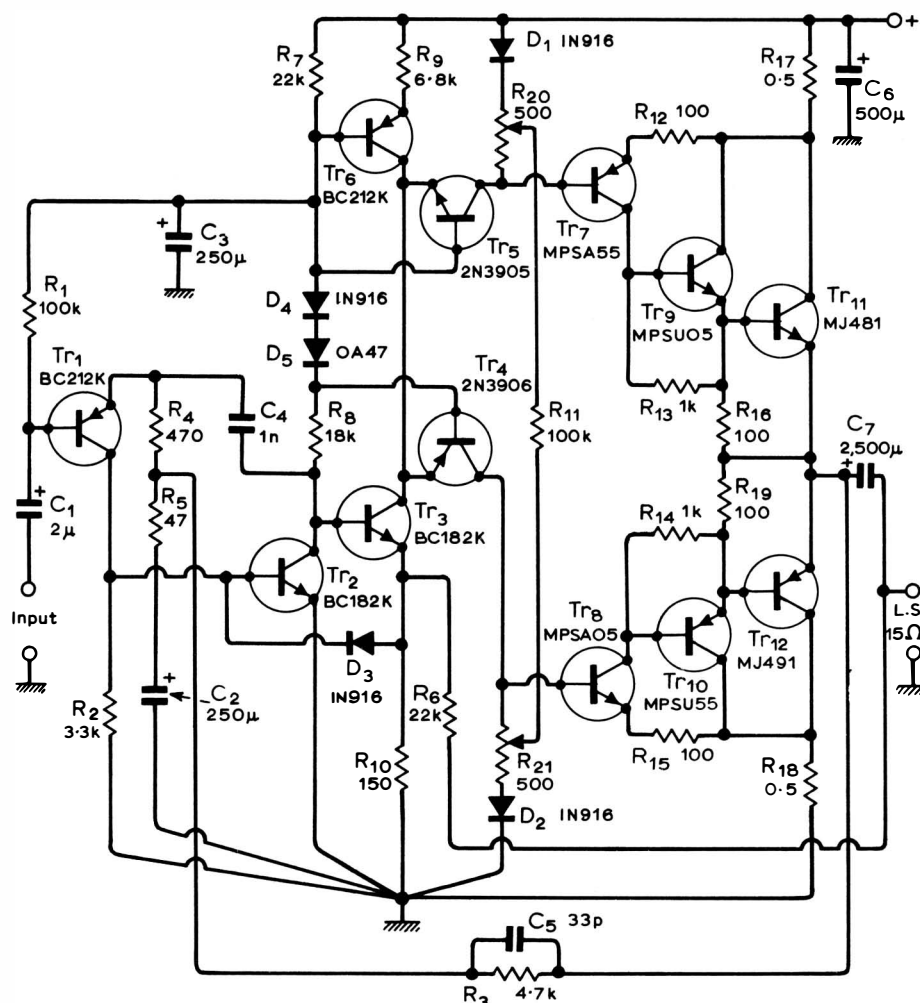


Fig. 1. Complete power amplifier circuit using new approach. Design gives harmonic distortion of 0.01% at all power levels and intermodulation distortion of 0.003%.

\*Allen Clarke Research Laboratory (Plessey), Towcester, Northants.