NECX & NESX Single-Ended to Balanced Converter

XEN Audio

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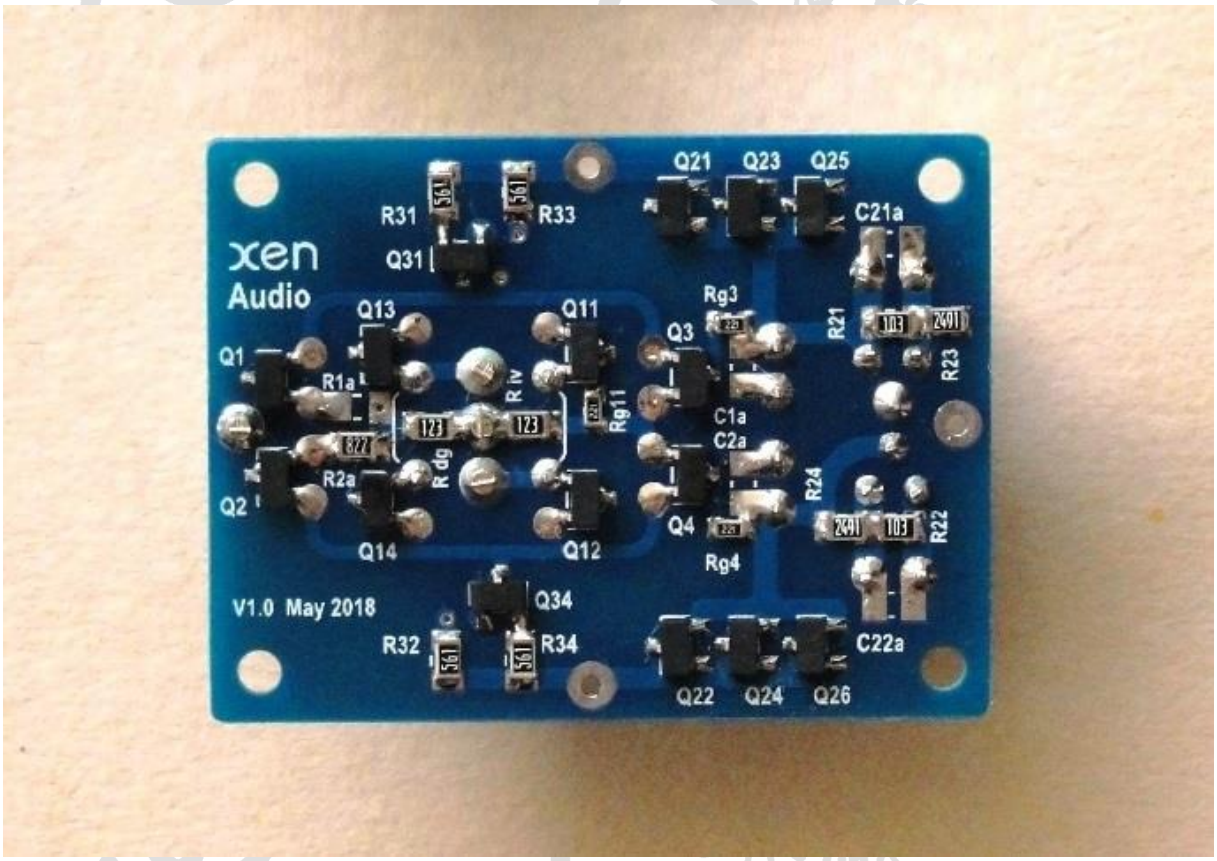


Background

When I first started DIY, I was already building balanced circuits right from the beginning. As then not all my signal sources had balanced output, there was already a need for a single-ended to balanced converter,

The first of such converter that I built was a John Linsley Hood phase splitter (PS) [1]. Could not be simpler with 1 BJT, 4 resistors, and 3 caps. All fine for testing purposes, but not really as permanent solution, with no PSRR on the negative phase, and coupling caps on both outputs.

Some years ago, I made an attempt to design a Gnd referenced phase shifter to eliminate the coupling caps [2]. One can imagine this as the JLH PS with a folded cascode. But I was not totally happy with the design, and it was shelfed for quite a few years. Until recently, the success of the NEXEN and the Pioneer Super Linear Circuit [3] re-ignited the interest to make another serious attempt.

Circuit Description

The best way to explain the Phase Splitter in [2] is to start with a modified SEN IV [4]. Take a standard SEN IV, and connect its current input to Gnd via a resistor R_dg. Then connect the gate of the top N-

JFET to Vin. The N-JFET pair now functions as a JFET follower, loaded by R_dg. Let's call this the SEN PS (Phase Splitter).

Again, applying Kirchhoff's Law as in the SEN_IV, and assuming gate current is negligible, the current flowing through Rdg has to be accompanied by an equal and opposite current through R_iv. If R_dg is large enough in value, the follower output is much the same as the input, so +Vin ~ Out+. In case R_dg = R_iv, and since the current is equal and opposite, so is Out- to Out+. And we have converted a single ended signal to balanced.

It was already mentioned above that R_dg and R_iv cannot be too small or distortion will go up. Typically, they should be around 10k. While the Out+ connection sees the Zout of the top JFET, Zout at the Out- connection is R_iv. In order to be able to drive proper loads, it is sensible to add a low Zout buffer at Out+ and Out-. A matched pair each of 2SK170s or 2SK117s would do nicely.

The distortion of Out- is essentially the same as that of Out+, i.e. no even harmonics cancellation as in some other balanced circuits, such as the NEXEN. This is, however, almost purely 2nd harmonics. So one can now go to a CEN PS, using 2SK246 / 2SJ103 complementary pair in push-pull. It would be even better using 2SK163 / 2SJ44 or 2SK170 / 2SJ74, if you can find them. Note that this problem with the distortion does not occur in the SEN IV, as the top JFET there is used as a cascode for the DAC current output pin, whereas here it is used to convert voltage to current, hence the dominant 2nd harmonics.

The output followers work better with fixed rails. So it would be nice if the CEN PS can also work with fixed rails. We can simply take the original circuit in [2], and mirror it about the Gnd level with complementary devices, as shown in the simplified schematics below. The essential element of the CEN PS is that the top and bottom current sources are absolutely identical at all times. Theoretically, they do not have to be constant or noise free, but only identical. And as long as that is the case, the sum of current around the middle loop has to be zero as well. And since all gate currents are negligible, the only current that can escape the loop are those through R_dg and R_iv. And since their sum has to be zero, R_iv = - R_dg, as before in the SEN PS.

The two additional JFETs on the RHS are necessary to serve as cascodes for the input JFET drains, so that the drain voltages are defined. It is more important that they have low capacitances than high Yfs, especially when the input JFETs have low or negligible Early effect (or more precisely channel-length modulation).

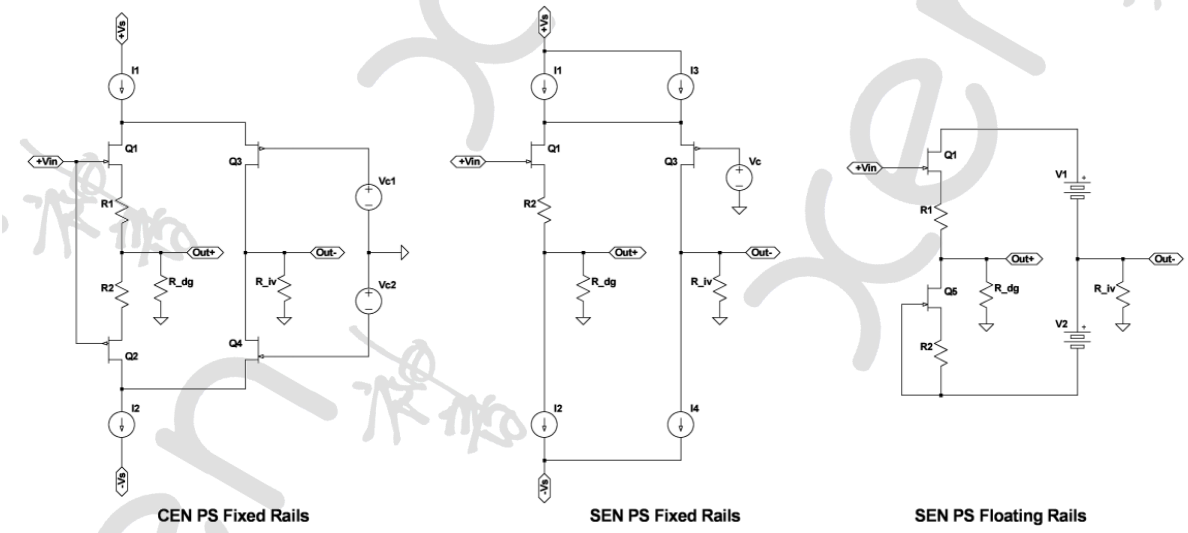


Fig. 1 Phase Splitter Topologies

As already mentioned, the first and most important task is a pair of self-tracking current sources at both rails. Rather than relying on thermal coupling of two independent CCS, it proves to be better to employ a pair of current mirrors at the top and bottom rails, both biased by a common JFET CCS. Especially when the current mirrors are well constructed, the tracking is excellent, as proven in the CCS biasing circuit of our Pioneer Super Linear Headphone Amplifier [3].

If we can make a complementary source follower and current conveyor, we can also make a single-ended one with N-JFET only, as in [1]. All is needed is to disconnect Q2 from the input and replace it with a CCS equal to Idss of Q1. That means in practice a pair of matched N-JFETs, with the lower one configured as a CCS. To make up for the loss in push-pull current sharing, a N-JFET with higher transconductance will be of benefit. Examples are 2SK170, 2SK117, 2SK209, etc.

Actually, the topology of the CEN PS looks essentially the same as Chris Hornbeck's JFET phase shifter [5]. Chris actually posted his circuit before my original, single-ended version. But I was not paying attention to the tube forums.

In Practice

We call our implementation of the CEN PS circuit NECX, as a reverse of the XCEN Balanced to Single-Ended Converter published in 2012 [6]. This time round, we have chosen to use 2SK246 / 2SJ103 Y-grade for the JFETs. There are a couple of reasons why the 2SK246 / 2SJ103 are chosen :

1) They are less of a unobtanium than 2SK170 / 2SJ74.
2) They can be found in Y grade, which allows low bias current to compensate for their low Yfs.
3) Low bias also reduces thermal drift.
4) Importantly, they are less sensitive to Vds (low Early Effect), especially at low current and at Vds above 3V.
5) They have much lower capacitances, thus lower gate-current induced distortion in current conveyor circuits.
6) Their somewhat higher noise is not critical for line level applications at unity gain.

The circuit is also very easy on power supply requirements. For the phase splitter itself, it is constant current and isolated by 2 CCS's. So PSRR is good by design. The Cascode setting voltages want to be reasonable stable and low noise, but this is also great help by the low Early Effect of the chosen devices. The 2 balanced output source followers together also draw (largely) constant current when equally loaded. They can share the same voltage as the cascode JFET gates, and thus can be supplied by a common dual-rail supply. Because of the relatively low current involved, a pair of CCS fed shunt regulators (e.g. TL431's from On Semi) would do very nicely.

We of course also want to try out the single-ended version, which will be called NESX. In this case, Q1,2 are matched 2SK117's for their higher transconductance. But since there is no complementary device to 2SK117, we have to stick to 2SK246 / 2SJ103 for Q3,4.

The final circuit can look something like the schematics in Fig. 2 & 3. Although we built our prototypes with only SMD devices, their TO92 equivalents can be used without any downside whatsoever, though 2SA970 / 2SC2240 might also be difficult to get these days. For lowest DC drift, thermal coupling is important for the current mirrors, the input JFET pair, and the source followers.

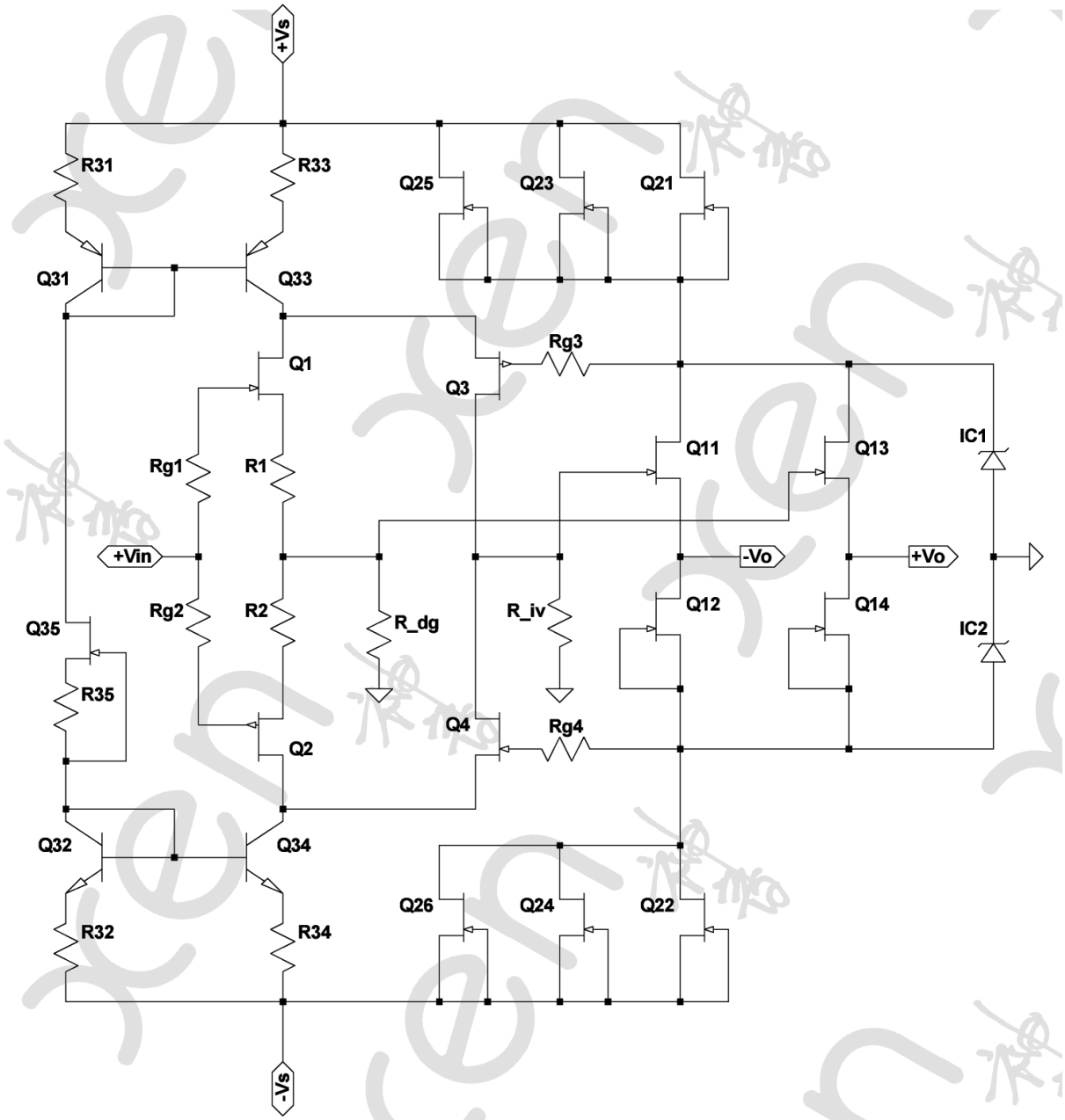


Fig. 2 Schematics of the NECX Single-Ended to Balanced Converter

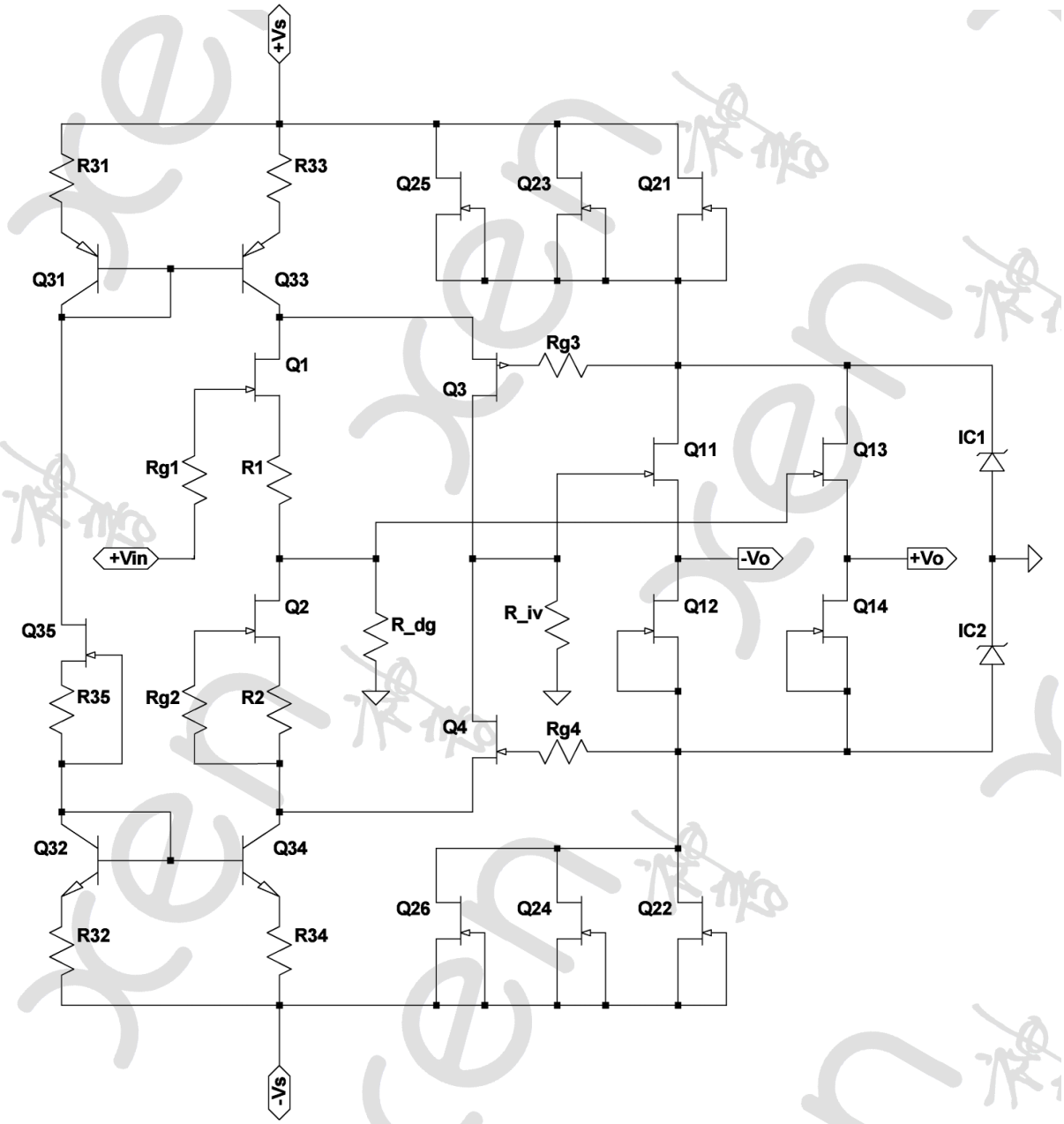
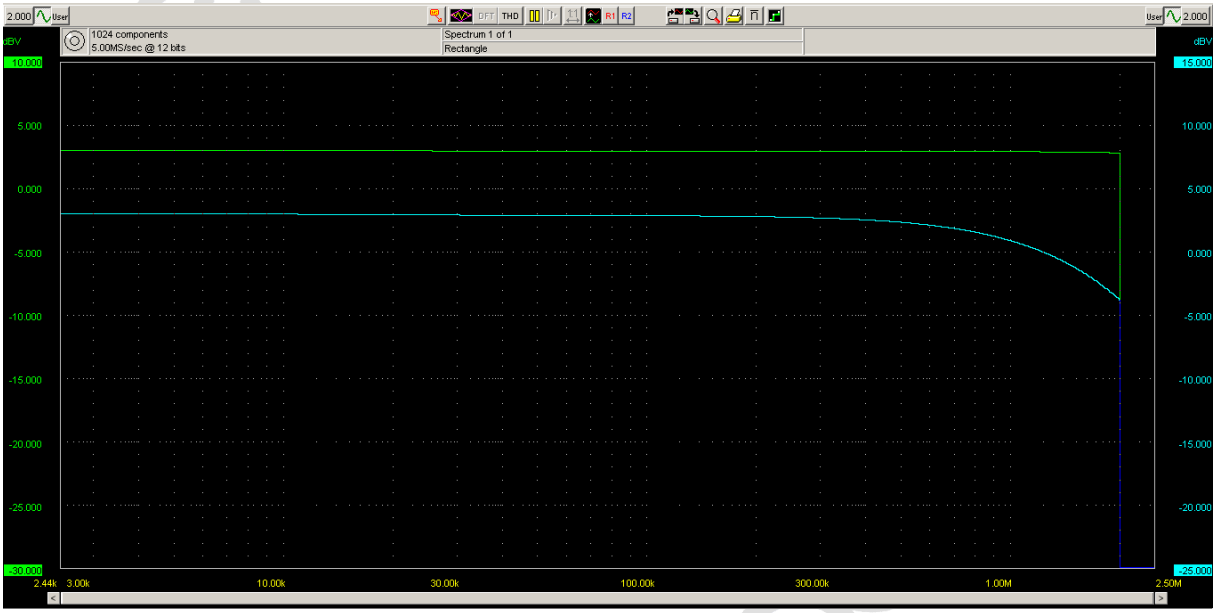


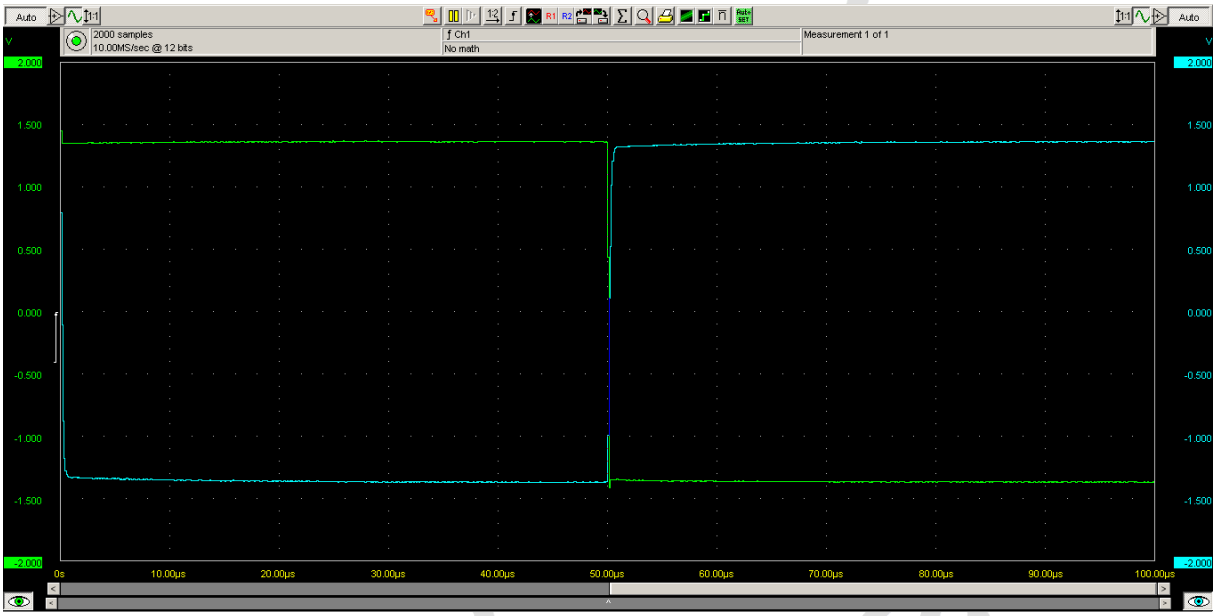
Fig. 3 Schematics of the NESX Single-Ended to Balanced Converter

Prototype Measurements

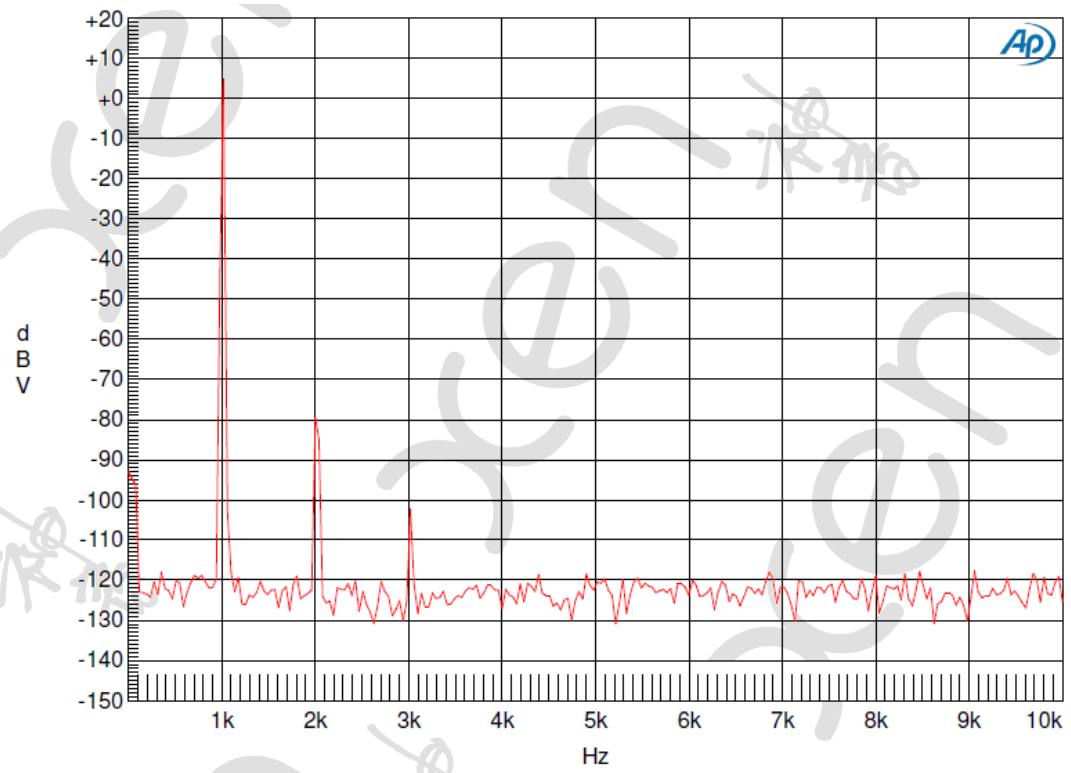
We built a pair of both circuits in full SMD. It is not really essential to thermally couple all the devices, as dissipation is low, in the order of 10~20mW per device. One can, if so wish, mount the PCB against an aluminium plate or heatsink, with flexible thermal pads in between. Without thermal coupling, the DC offsets of both phases were stable to < +/-2mV over 30 minutes after 2 minutes warm-up.

AC gain at 1kHz is 0.97 for both output phases. Bandwidth for the positive phase was larger than 2MHz (limited by test equipment). That for the negative phase was 1.1MHz at -3dB. At high frequencies, the gates of both JFET followers start to draw current, thus reducing the amplitude of the negative phase over R_iv. 10kHz square waves were copybook perfect.





The biggest question is whether the single-ended NESX with higher transconductance JFETs will have lower distortion than push-pull with lower transconductance. Both circuits were measured with an Audio Precision 2722 Analyser. Input signal was 1Vrms at 1kHz, single ended. And output was measured differentially across +Vo and -Vo. The surprise was how close the results were, with NECX having a second harmonics at -86dB, and third at -109dB. The NESX almost gave identical values at -88dB and -106dB respectively. Noise floor in both cases were around -120dBV. So there is really nothing to choose from between the two. The only major difference is the lower front-end bias and drift of the NECX.



Another successful conclusion to a year-long unfinished circuit.

References

1. John Linsley Hood Simple Class A Amplifier, A Postscript
   Wireless World, October 1969, Fig. 4

2. http://www.diyaudio.com/forums/solid-state/200325-fet-based-phase-splitter-2.html#post2814583

3. http://www.diyaudio.com/forums/headphone-systems/313163-pioneer-super-linear-circuit.html

4. http://www.diyaudio.com/forums/digital-line-level/195483-zen-cen-sen-evolution-minimalistic-iv-converter.html

5. http://www.diyaudio.com/forums/tubes-valves/189153-phase-splitter-issue-3.html#post2802454

6. http://www.diyaudio.com/forums/analog-line-level/216557-xcen-balanced-single-converter.html

Appendix 1 Bill of Materials for NECX
Per Channel (+/-18V rails)

Quantity	Designation	Description	Alternative
1	Q1	2SK246-Y, Idss ~ 2mA	2SK208-Y
1	Q2	2SJ103-Y, Idss ~ 2mA	2SJ106-Y
1	Q3	2SJ103-Y, Idss > 2mA	2SJ106-Y
1	Q4	2SK246-Y, Idss > 2mA	2SK208-Y
4	Q11 ~ 14	2SK117-GR, matched Idss	2SK209-GR
6	Q21 ~ 26	2SK209-GR, Idss matched to 10%	
2	Q31, 33	2SA1312-BL, matched hfe	
2	Q32, 34	2SC3324-BL, matched hfe	
1	Q35	2SK209-GR, Idss > 2mA	
2	IC21, 22	TL431 TO-92 On Semi	
1+1	R1, 1a	Susumu 0805 0.5%, trim Q1 to 1mA	
1+1	R2, 2a	Susumu 0805 0.5%, trim Q2 to 1mA	
2	R21, 22	Susumu 0805 10k 0.5%	
2	R23, 24	Susumu 0805 2.49k 0.5%	
4	R31 ~ 34	Susumu 0805 499R 0.5%	
2	R33a, 34a	Susumu 0805 0.5%, trim -Vo DC	
1	R35	Susumu 0805 0.5%, trim Q35 to 2mA	
2	R_dg, R_iv	Susumu 0805 12k 0.5%	
6	Rg1 ~ 4, 11, 13	Susumu 0603 100R 0.5%	
2	C1, 2	Nichicon KA 47µ 25V	
2	C21, 22	Nichicon KA 100µ 16V	
2	C21a, 22a	Panasonic 0805 ECPU 16V 100n	

Appendix 1 Bill of Materials for NESX
Per Channel (+/-18V rails)

Quantity	Designation	Description	Alternative
1	Q1	2SK117-GR	2SK209-GR
1	Q2	2SJ117-GR, Idss matched to Q1	2SK209-GR
1	Q3	2SJ103-Y, Idss > 2mA	2SJ106-Y
1	Q4	2SK246-Y, Idss > 2mA	2SK208-Y
4	Q11 ~ 14	2SK117-GR, matched Idss	2SK209-GR
6	Q21 ~ 26	2SK209-GR, Idss matched to 10%	
2	Q31, 33	2SA1312-BL, matched hfe	
2	Q32, 34	2SC3324-BL, matched hfe	
1	Q35	2SK209-GR, Idss > 4mA	
2	IC21, 22	TL431 TO-92 On Semi	
1+1	R1, 1a	Susumu 0805 0.5%, trim Q1 to 2mA	
1+1	R2, 2a	Susumu 0805 0.5%, trim Q2 to 2mA	
2	R21, 22	Susumu 0805 10k 0.5%	
2	R23, 24	Susumu 0805 2.49k 0.5%	
4	R31 ~ 34	Susumu 0805 499R 0.5%	
2	R33a, 34a	Susumu 0805 0.5%, trim -Vo DC	
1	R35	Susumu 0805 0.5%, trim Q35 to 4mA	
2	R_dg, R_iv	Susumu 0805 12k 0.5%	
6	Rg1 ~ 4, 11, 13	Susumu 0603 100R 0.5%	
2	C1, 2	Nichicon KA 47µ 25V	
2	C21, 22	Nichicon KA 100µ 16V	
2	C21a, 22a	Panasonic 0805 ECPU 16V 100n	