LF398 - Monolithic Sample and Hold Circuit

Features

- Operates from ±5V to ±18V supplies
- Less than 10 µs acquisition time
- TTL, PMOS, CMOS compatible logic input
- 0.5 mV typical hold step at C_h = 0.01 µF
- Low input offset
- 0.002% gain accuracy
- Low output noise in hold mode
- Input characteristics do not change during hold mode
- High supply rejection ratio in sample or hold
- Wide bandwidth
- Space qualified, JM38510

Parametric Table

Temperature Min	0 deg C
Temperature Max	70 deg C
Offset Voltage max, 25C	3, 10 mV

Datasheet

RoHS Compliance Information
LF198/LF298/LF398, LF198A/LF398A Monolithic Sample-and-Hold Circuits
LF198/LF298/LF398, LF198A/LF398A Monolithic Sample-and-Hold Circuits (**Japanese**)

Package Availability, Models, Samples & Pricing

Part Number	Package							Factory Lead Time		Models				Std Pack Size	Package Marking Format
	Type	Pins	Spec.	MSL Rating	Peak Reflow	RoHS Report	CAD Symbols	Weeks	Qty						
LF398M	SOIC NARROW	14	STD	1	235	RoHS	N/A	Full production		N/A				rail of 55	NSUZXYTT LF398M
			NOPB	1	260			6 weeks	1000						
LF398MX	SOIC NARROW	14	STD	1	235	RoHS	N/A	Full production		N/A				reel of 2500	NSUZXYTT LF398M
			NOPB	1	260			6 weeks	3000						
LF398AN	MDIP	8	STD	1	NA	RoHS	N/A	Full production		N/A				rail of 40	NSUZXYTT LF 398AN
			NOPB	1	NA			6 weeks	500						

LF398N	MDIP	8	STD NOPB	1 1	NA NA	RoHS	N/A	Full production 8 weeks	1000	N/A				rail of 40	NSUZXYTT LF 398N
LF398AH	TO-99	8	NOPB	1	NA	RoHS	N/A	Obsolete 6 weeks	1000	N/A				box of 500	NSZXYTTE# LF398AH
LF398H	TO-99	8	STD NOPB	1 1	NA NA	RoHS	N/A	Full production 6 weeks	1000	N/A				box of 500	NSZXYTTE# LF398H
LF398 MDC	Unpackaged Die							Custom N/A	N/A	N/A				tray of N/A	-
LF398 MWC	Wafer							Obsolete N/A	40000	N/A				wafer jar of N/A	-

Obsolete Versions

Obsolete Part	Alternate Part or Supplier	Source	Last Time Buy Date
LF398AH	LF198AH	NSC	12/03/2008

General Description

The LF198/LF298/LF398 are monolithic sample-and-hold circuits which utilize BI-FET technology to obtain ultra-high dc accuracy with fast acquisition of signal and low droop rate. Operating as a unity gain follower, dc gain accuracy is 0.002% typical and acquisition time is as low as 6 µs to 0.01%. A bipolar input stage is used to achieve low offset voltage and wide bandwidth. Input offset adjust is accomplished with a single pin, and does not degrade input offset drift. The wide bandwidth allows the LF198 to be included inside the feedback loop of 1 MHz op amps without having stability problems. Input impedance of 10^{10}Ohm allows high source impedances to be used without degrading accuracy.

P-channel junction FET's are combined with bipolar devices in the output amplifier to give droop rates as low as 5 mV/min with a 1 µF hold capacitor. The JFET's have much lower noise than MOS devices used in previous designs and do not exhibit high temperature instabilities. The overall design guarantees no feed-through from input to output in the hold mode, even for input signals equal to the supply voltages.

Reliability Metrics

Part Number	Process	EFR Reject	EFR Sample Size	PPM *	LTA Rejects	LTA Device Hours	FITS	MTTF (Hours)
LF398 MDC	BIFET	0	12335	0	0	975000	4	276658912
LF398 MWC	BIFET	0	12335	0	0	975000	4	276658912
LF398AH	BIFET	0	12335	0	0	975000	4	276658912
LF398AN	BIFET	0	12335	0	0	975000	4	276658912
LF398H	BIFET	0	12335	0	0	975000	4	276658912
LF398M	BIFET	0	12335	0	0	975000	4	276658912
LF398MX	BIFET	0	12335	0	0	975000	4	276658912
LF398N	BIFET	0	12335	0	0	975000	4	276658912

Note: The Early Failure Rates were calculated as point estimates. The Long Term Failure Rates were calculated at 60% confidence using the Arrhenius equation at 0.7eV activation energy and derating the assumed stress temperature of 150°C to an application temperature of 55°C.

National Semiconductor

LF198/LF298/LF398, LF198A/LF398A Monolithic Sample-and-Hold Circuits

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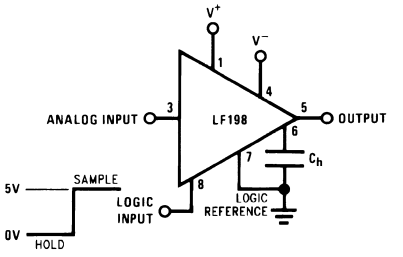
Logic inputs on the LF198 are fully differential with low input current, allowing direct connection to TTL, PMOS, and CMOS. Differential threshold is 1.4V. The LF198 will operate from ±5V to ±18V supplies.

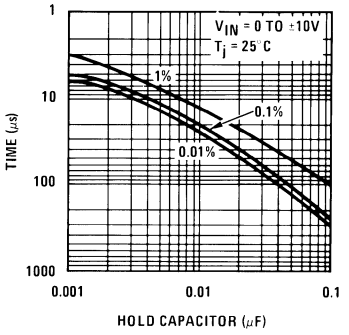
An "A" version is available with tightened electrical specifications.

Typical Connection and Performance Curve



DS005692-32

Acquisition Time



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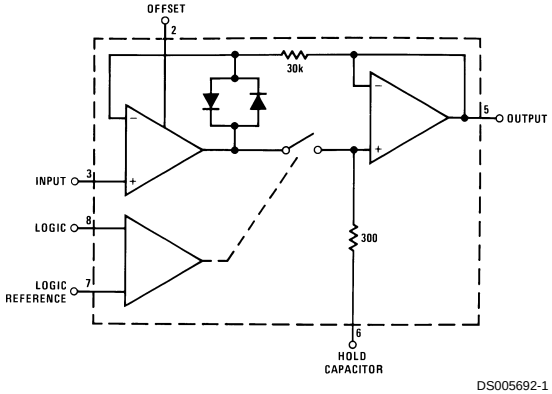
Functional Diagram



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	±18V
Power Dissipation (Package Limitation) (Note 2)	500 mW
Operating Ambient Temperature Range	
LF198/LF198A	−55˚C to +125˚C
LF298	−25˚C to +85˚C
LF398/LF398A	0˚C to +70˚C
Storage Temperature Range	−65˚C to +150˚C
Input Voltage	Equal to Supply Voltage
Logic To Logic Reference Differential Voltage (Note 3)	+7V, −30V
Output Short Circuit Duration	Indefinite
Hold Capacitor Short Circuit Duration	10 sec
Lead Temperature (Note 4)	
H package (Soldering, 10 sec.)	260˚C
N package (Soldering, 10 sec.)	260˚C
M package:	
Vapor Phase (60 sec.)	215˚C
Infrared (15 sec.)	220˚C
Thermal Resistance (θ_{JA}) (typicals)	
H package	215˚C/W (Board mount in still air)
	85˚C/W (Board mount in 400LF/min air flow)
N package	115˚C/W
M package	106˚C/W
θ_{JC} (H package, typical)	20˚C/W

Electrical Characteristics

The following specifcations apply for $-V_S + 3.5V \le V_{IN} \le +V_S - 3.5V$, $+V_S = +15V$, $-V_S = -15V$, $T_A = T_j = 25˚C$, $C_h = 0.01\ \mu F$, $R_L = 10\ k\Omega$, LOGIC REFERENCE = 0V, LOGIC HIGH = 2.5V, LOGIC LOW = 0V unless otherwise specified.

Parameter	Conditions	LF198/LF298			LF398			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage, (Note 5)	$T_j = 25˚C$		1	3		2	7	mV
	Full Temperature Range			5			10	mV
Input Bias Current, (Note 5)	$T_j = 25˚C$		5	25		10	50	nA
	Full Temperature Range			75			100	nA
Input Impedance	$T_j = 25˚C$		10^{10}			10^{10}		Ω
Gain Error	$T_j = 25˚C$, $R_L = 10k$		0.002	0.005		0.004	0.01	%
	Full Temperature Range			0.02			0.02	%
Feedthrough Attenuation Ratio at 1 kHz	$T_j = 25˚C$, $C_h = 0.01\ \mu F$	86	96		80	90		dB
Output Impedance	$T_j = 25˚C$, "HOLD" mode		0.5	2		0.5	4	Ω
	Full Temperature Range			4			6	Ω
"HOLD" Step, (Note 6)	$T_j = 25˚C$, $C_h = 0.01\ \mu F$, $V_{OUT} = 0$		0.5	2.0		1.0	2.5	mV
Supply Current, (Note 5)	$T_j \ge 25˚C$		4.5	5.5		4.5	6.5	mA
Logic and Logic Reference Input Current	$T_j = 25˚C$		2	10		2	10	µA
Leakage Current into Hold Capacitor (Note 5)	$T_j = 25˚C$, (Note 7) Hold Mode		30	100		30	200	pA
Acquisition Time to 0.1%	$\Delta V_{OUT} = 10V$, $C_h = 1000\ pF$		4			4		µs
	$C_h = 0.01\ \mu F$		20			20		µs
Hold Capacitor Charging Current	$V_{IN} - V_{OUT} = 2V$		5			5		mA
Supply Voltage Rejection Ratio	$V_{OUT} = 0$	80	110		80	110		dB
Differential Logic Threshold	$T_j = 25˚C$	0.8	1.4	2.4	0.8	1.4	2.4	V
Input Offset Voltage, (Note 5)	$T_j = 25˚C$		1	1		2	2	mV
	Full Temperature Range			2			3	mV
Input Bias Current, (Note 5)	$T_j = 25˚C$		5	25		10	25	nA
	Full Temperature Range			75			50	nA

Electrical Characteristics

The following specifcations apply for $-V_S + 3.5V \le V_{IN} \le +V_S - 3.5V$, $+V_S = +15V$, $-V_S = -15V$, $T_A = T_j = 25^\circ C$, $C_h = 0.01\ \mu F$, $R_L = 10\ k\Omega$, LOGIC REFERENCE = 0V, LOGIC HIGH = 2.5V, LOGIC LOW = 0V unless otherwise specified.

Parameter	Conditions	LF198A			LF398A			Units
		Min	Typ	Max	Min	Typ	Max	
Input Impedance	$T_j = 25^\circ C$		10^{10}			10^{10}		Ω
Gain Error	$T_j = 25^\circ C$, $R_L = 10k$		0.002	0.005		0.004	0.005	%
	Full Temperature Range			0.01			0.01	%
Feedthrough Attenuation Ratio at 1 kHz	$T_j = 25^\circ C$, $C_h = 0.01\ \mu F$	86	96		86	90		dB
Output Impedance	$T_j = 25^\circ C$, "HOLD" mode		0.5	1		0.5	1	Ω
	Full Temperature Range			4			6	Ω
"HOLD" Step, (Note 6)	$T_j = 25^\circ C$, $C_h = 0.01\mu F$, $V_{OUT} = 0$		0.5	1		1.0	1	mV
Supply Current, (Note 5)	$T_j \ge 25^\circ C$		4.5	5.5		4.5	6.5	mA
Logic and Logic Reference Input Current	$T_j = 25^\circ C$		2	10		2	10	µA
Leakage Current into Hold Capacitor (Note 5)	$T_j = 25^\circ C$, (Note 7) Hold Mode		30	100		30	100	pA
Acquisition Time to 0.1%	$\Delta V_{OUT} = 10V$, $C_h = 1000\ pF$		4	6		4	6	µs
	$C_h = 0.01\ \mu F$		20	25		20	25	µs
Hold Capacitor Charging Current	$V_{IN} - V_{OUT} = 2V$		5			5		mA
Supply Voltage Rejection Ratio	$V_{OUT} = 0$	90	110		90	110		dB
Differential Logic Threshold	$T_j = 25^\circ C$	0.8	1.4	2.4	0.8	1.4	2.4	V

Note 1: "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{JMAX} - T_A)/\theta_{JA}$, or the number given in the Absolute Maximum Ratings, whichever is lower. The maximum junction temperature, T_{JMAX}, for the LF198/LF198A is 150°C; for the LF298, 115°C; and for the LF398/LF398A, 100°C.

Note 3: Although the differential voltage may not exceed the limits given, the common-mode voltage on the logic pins may be equal to the supply voltages without causing damage to the circuit. For proper logic operation, however, one of the logic pins must always be at least 2V below the positive supply and 3V above the negative supply.

Note 4: See AN-450 "Surface Mounting Methods and their effects on Product Reliability" for other methods of soldering surface mount devices.

Note 5: These parameters guaranteed over a supply voltage range of ±5 to ±18V, and an input range of $-V_S + 3.5V \le V_{IN} \le +V_S - 3.5V$.

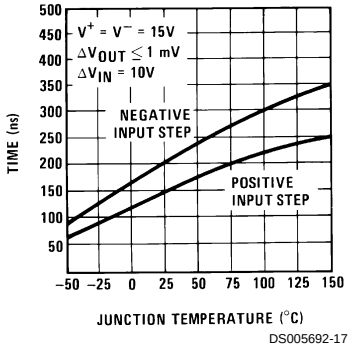
Note 6: Hold step is sensitive to stray capacitive coupling between input logic signals and the hold capacitor. 1 pF, for instance, will create an additional 0.5 mV step with a 5V logic swing and a 0.01µF hold capacitor. Magnitude of the hold step is inversely proportional to hold capacitor value.

Note 7: Leakage current is measured at a junction temperature of 25°C. The effects of junction temperature rise due to power dissipation or elevated ambient can be calculated by doubling the 25°C value for each 11°C increase in chip temperature. Leakage is guaranteed over full input signal range.

Note 8: A military RETS electrical test specification is available on request. The LF198 may also be procured to Standard Military Drawing #5962-8760801GA or to MIL-STD-38510 part ID JM38510/12501SGA.

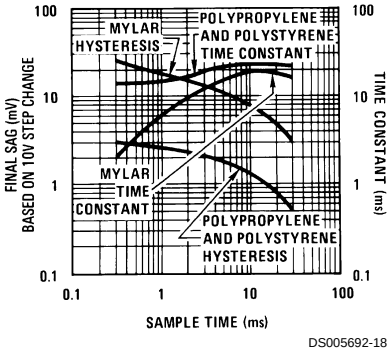
Typical Performance Characteristics

Aperture Time
(Note 9)



DS005692-17

Dielectric Absorption Error in Hold Capacitor



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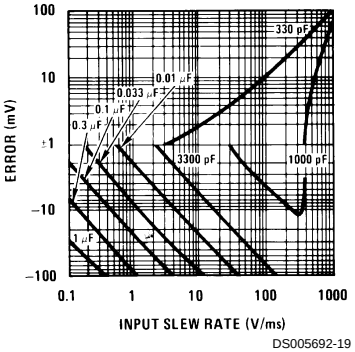
Dynamic Sampling Error



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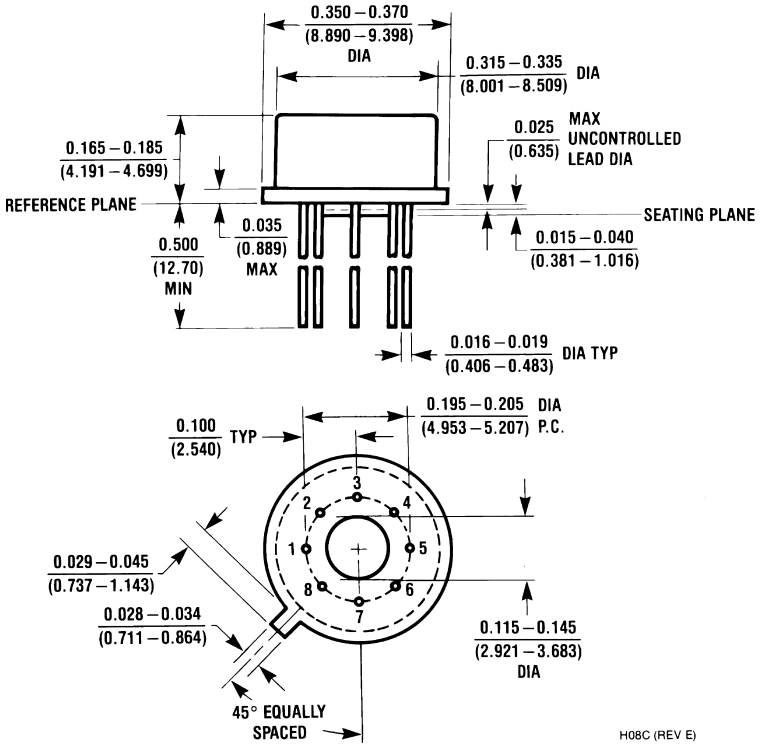
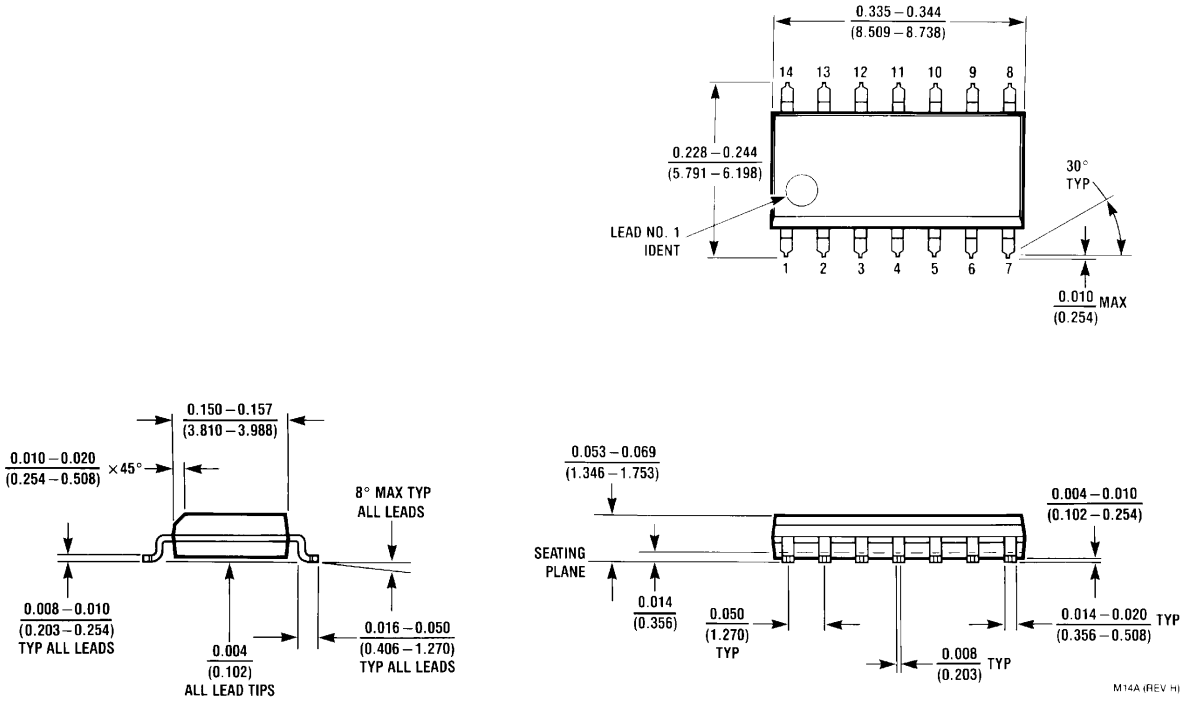
Note 9: See Definition of Terms

Physical Dimensions inches (millimeters) unless otherwise noted

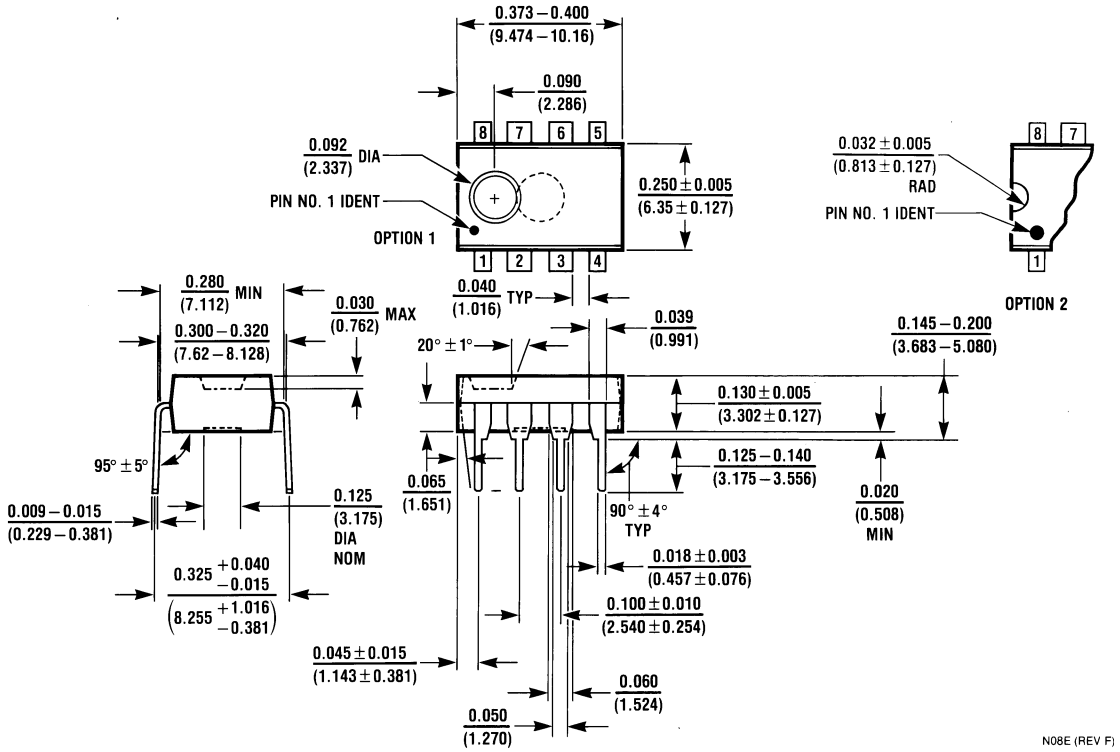


Metal Can Package (H)
Order Number LF198H, LF298H, LF398H, LF198AH or LF398AH
NS Package Number H08C



Molded Small-Outline Package (M)
Order Number LF298M or LF398M
NS Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Molded Dual-In-Line Package (N)
Order Number LF398N or LF398AN
NS Package Number N08E

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.