subsequent cascaded filters cut off at lower frequencies, and the circuit can switch these filters in or out depending on the desired output (**Table 1**). The µC's speed, code efficiency, the number of discrete frequencies to be generated, and the spacing between those frequencies all determine the maximum frequency of operation. The number of loops for one-half cycle of output frequency (50% duty cycle) equals the number of cycles per loop×time/cycle. With a 3.58-MHz crystal, the time per software cycle is 558 nsec. (The 705J1A µC uses one-half of the oscillation frequency for its internal operating frequency.) **Table 1** shows some example frequencies and the corresponding number of loops.

The RC filters have a cutoff frequency, or –3-dB point, at the generated frequency for maximum linearity and minimum distortion. You should note that the output is approximately the same level across all frequencies because the resistors are always in series when driving a high-impedance load. However, because of leakage when a capacitor is active, or grounded, the lowest frequency has a lower output than the highest frequency. You should optimize the R and C values in **Figure 1** for your application, desired output frequencies, and impedance. You can switch the filters on and off sequentially, independently, or in combinations to suit different needs. (DI #2278)

LISTING 1—FREQUENCY-GENERATING SUBROUTINE

```
fgen    sta templ               ;store accumulator in a temp variable
        lda #04                 ;number of interrupts for 250mS (5*65mS)
timer   bset 2,tscr             ;clear real time interrupt flag
innr3   bset 4,output           ;turn on oscillator output
        ldx frec                ;number for one half cycle
innr1   decx                    ;count down for half cycle
        bne innr1               ;if not finished, keep counting
        bclr 4,output           ;turn off oscillator output
        ldx frec                ;number for other half of cycle
innr2   decx                    ;count down for half cycle
        bne innr2               ;if not finished, keep counting
        brclr 6,tscr,innr3      ;if 65mS not passed (see timer/counter
section of docs) do another cycle
        deca                    ;subtract from the five  65mS for 250mS
total
        bne timer               ;have 250mS gone by? If not go back and
repeat all
        lda templ               ;restore accumulator
        rts                     ;
```

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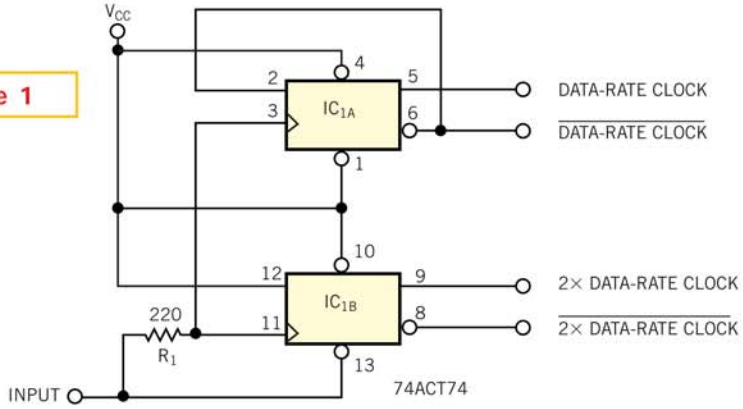
74ACT74 makes low-skew clock divider

Tom Napier, Consultant, North Wales, PA

Serial-data systems often generate an internal clock at twice the data rate for mid-bit sampling or for generating bi-phase codes. External equipment and some internal processes require a clock that runs at the data rate. Simply dividing the twice-rate clock with a flip-flop generates a data-rate clock that is skewed by one logic delay with respect to the input. This delay can be a significant fraction of the bit period. You can use specialized PLL-based low-skew divider chips to deal with this problem, but these chips have a limited frequency range and are not designed to follow rapid changes in the data rate.

Figure 1



The 74ACT74 dual flip-flop generates two clock rates with negligible skew.

The circuit in **Figure 1** uses a dual flip-flop, the 74ACT74, to generate both clock rates as well as both clock polarities with negligible skew. One half of the chip, IC$_{1A}$, acts as a normal divide-by-two circuit. The other half, IC$_{1B}$, tracks the input clock because the input's leading edge triggers IC$_{1B}$ high and the input's trailing edge resets IC$_{1B}$. The divider transitions are synchronous within a few hundred picoseconds with the positive transitions of the twice-rate clock that the chip's other half generates. This circuit works with inputs from a few hertz to more than 100 MHz.

Without R$_1$, the input removes the reset from the twice-rate flip-flop at the same moment as the input clocks this flip-flop on. Theoretically, this setup is allowable because the 74ACT74's reset-recovery time is specified as 0 nsec. In practice, a resistor in the 100 to 500V region, in conjunction with the chip's input capacitance, delays the clock inputs slightly and adds a useful safety margin. (DI #2282)

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